RF MICRO·DEVICES

RF2464

VHF QUADRATURE MODULATOR

Typical Applications

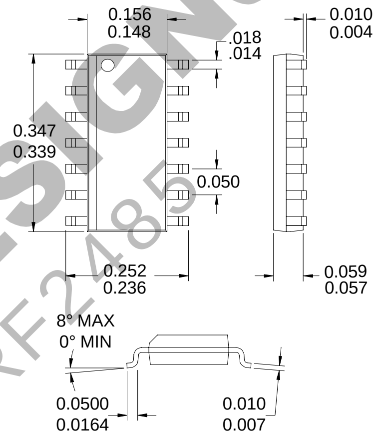
- Digital and Spread-Spectrum Systems
- GMSK, QPSK, DQPSK, QAM Modulation
- Private Mobile Radio and TETRA systems
- AM, SSB, DSB Modulation
- Image-Reject Upconverters

Product Description

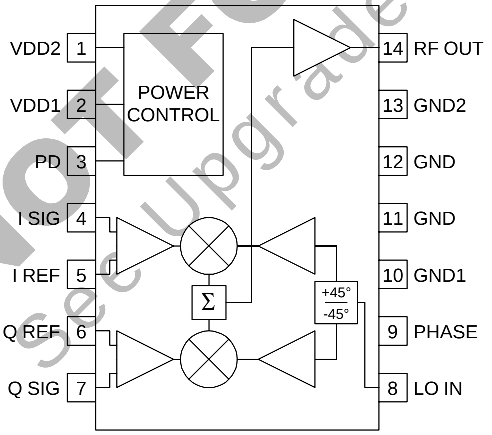
The RF2464 is a monolithic integrated universal modulation system capable of generating modulated AM, PM, or compound carriers in the VHF and UHF frequency range. The IC contains all of the required components to implement the modulation function including differential amplifiers for the baseband inputs, a 90° hybrid phase splitter, limiting LO amplifiers, two balanced mixers, a combining amplifier, and an output RF amplifier which will drive a 50Ω load. Component matching, which can only be accomplished with monolithic construction, is used to full advantage to obtain excellent amplitude balance and high phase accuracy. The unit features low power consumption, single power supply operation and adjustment free operation with no external parts required to operate the part as specified.

Optimum Technology Matching® Applied

☐ Si BJT ☐ GaAs HBT ☑ GaAs MESFET
☐ Si Bi-CMOS ☐ SiGe HBT ☐ Si CMOS



Package Style: SOIC-14



Functional Block Diagram

Features

- Single 3V to 5V Power Supply
- Low Power and Small Size
- CMOS Compatible Power Down Control
- Excellent Amplitude and Phase Balance
- Low Broadband Noise Floor
- 200MHz to 600MHz Operation

Ordering Information

RF2464	VHF Quadrature Modulator
RF2464 PCBA	Fully Assembled Evaluation Board

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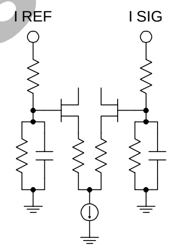
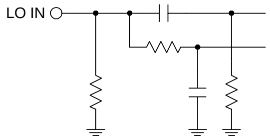
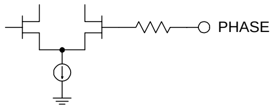
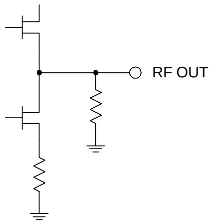
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V_{DC}
Power Down Voltage	-0.5 to V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

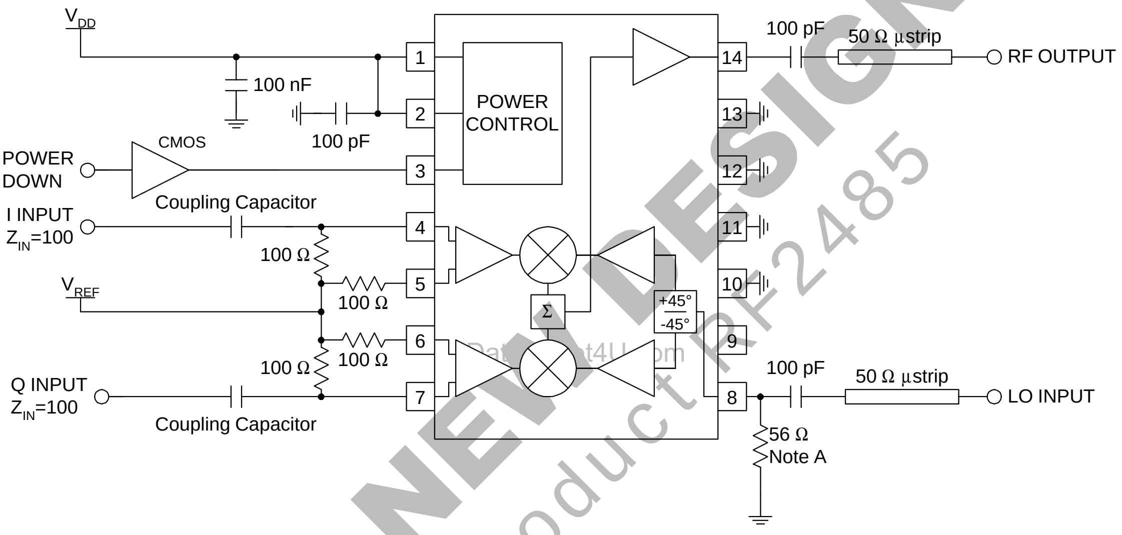
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LO Input					T=25°C, V_{DD}=5V_{DC}, I&Q inputs=2V_{PP}
Frequency Range		200 to 600		MHz	
Power Level		-3 to +6		dBm	
Input VSWR		1.2:1			With external 50Ω termination; see application schematic, note A.
Input Impedance		94-j264		Ω	At 200MHz, without external 50Ω termination.
		79-j158			At 400MHz, without external 50Ω termination.
		67-j117			At 600MHz, without external 50Ω termination.
Modulation Input					
Frequency Range		DC to 100		MHz	
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Modulation (I&Q)		V_{REF}±0.7		V	I & Q signals for 0dBm output power.
Modulation (I&Q)		V_{REF}±1.5		V	I & Q signals for +5dBm output power.
Maximum Modulation (I&Q)		V_{REF}±2.5		V	In-phase and quadrature signals.
Input Resistance		3000		Ω	
DC Offset		50	150	mV	I_{SIG}-I_{REF} and Q_{SIG}-Q_{REF}; to achieve maximum carrier suppression.
Amplitude Error (I/Q)		0.2		dB	
Quadrature Phase Error		±1	±3	°	From 350MHz to 450MHz.
RF Output					V_{DD}=5V, LO Power=0dBm, LO Freq=400MHz, SSB, I&Q input=0.7V_P
Output Power	-1	+1	+3	dBm	
Output Impedance		50			
Output VSWR		1.5:1			
Broadband Noise Floor		-143		dBm/Hz	At 20MHz offset
Sideband Suppression		25	>40	dB	
Carrier Suppression	18	25	>40	dB	Modulation DC offset can be externally adjusted for optimum suppression. Suppression is typically better than 25dB without adjustment.
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>1		MΩ	
Power Down "ON"		V_{CC}		V	Threshold voltage
Power Down "OFF"		0		V	Threshold voltage
Power Supply					
Voltage		5		V	Specifications
		3 to 5.5		V	Operating Limits
Current		28	39	mA	Operating
		0.5	2	mA	Power Down

Pin	Function	Description	Interface Schematic
1	VDD2	Power supply for the RF Output amplifier. An external RF bypass capacitor is needed. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the capacitor should connect immediately to the ground plane.	
2	VDD1	Power supply for all other circuits. An external RF bypass capacitor is needed.	
3	PD	Power Down control. When this pin is 0V all circuits are turned off, and when +5V all circuits are operating. This is a high impedance input, internally connected to the gates of a few FETs. To minimize current consumption in power down mode, this pin should be as close to 0V as possible. In order to maximize output power this pin should be as close to +5V as possible during normal operation.	
4	I SIG	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be 2.5±0.5V. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, the Q SIG and Q REF also need to be swapped to maintain the correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain.	
5	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 40dB it may be tuned ±0.15V (relative to the I SIG DC voltage). Without tuning, it will typically be better than 25dB.	See pin 4.
6	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 40dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, it will typically be better than 25dB. The SIG and REF inputs are inputs of a differential amplifier. Therefore the REF and SIG inputs are interchangeable. If swapping the I SIG and I REF pins, Q SIG and Q REF also need to be swapped to maintain correct phase. It is also possible to drive the SIG and REF inputs in a balanced mode. This will increase the gain.	Same as pin 3.
7	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be 2.5±0.5V.	Same as pin 4.
8	LO IN	The input of the phase shifting network. This high impedance input can be matched with an external 56Ω termination resistor. This pin is internally connected to ground through a 4kΩ resistor. Putting a DC voltage on this pin is not recommended. However, connecting this pin to ground, e.g., through a shunt inductor, is allowed.	
9	PHASE	This pin allows to adjust the phase of the I/Q signals. However, the control is very sensitive and hard to control. Control voltage change for a few degrees adjustment is in the order of 10mV. Device to device and temperature variation are not characterized. Therefore it is not recommended to use this pin; leave it not connected. Do NOT connect to ground.For compensating large errors in the I/Q signals supplied to the device or in control loops this pin may prove useful.	
10	GND1	Ground connection of the LO phase shift network. This pin should be connected directly to the ground plane.	
11	GND	Ground connection for other circuits. Keep traces short and connect to ground plane immediately.	
12	GND	Same as pin 11.	
13	GND2	Ground connection for the RF output stage. A good ground connection is especially important at this pin to avoid interference with other circuits.	

Pin	Function	Description	Interface Schematic
14	RF OUT	50Ω output. This pin carries a DC voltage, and an external blocking capacitor is recommended.	

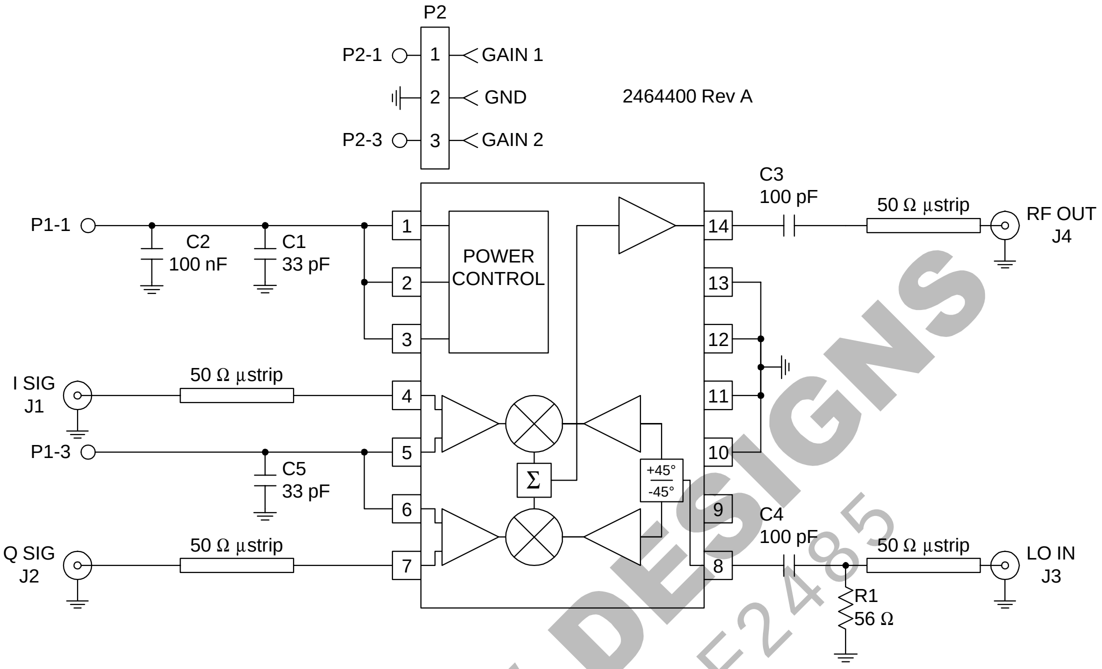
Application Schematic



NOTE A: Optional; input impedance is about 79-J158 Ω at 400 MHz without resistor. SMD resistor mounted adjacent to package pin, grounded through a via to the ground plane.

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
2” x 2”