RF2643

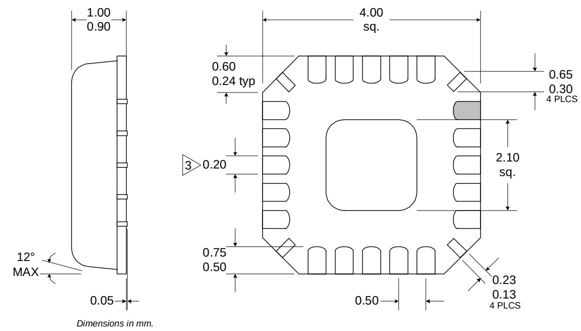
3V DUAL-BAND UPCONVERTER AND DRIVER AMPLIFIER

Typical Applications

- TDMA/AMPS Cellular Systems
- CDMA/AMPS Cellular Systems
- PCS Systems
- Portable Battery-Powered Equipment

Product Description

The RF2643 is a complete upconverter, dual-power amplifier driver and attenuator designed for Cellular and PCS systems. It is designed to upconverter and amplifies RF signals while providing 22dB of linear gain control range. It features digital control for the mixer and drivers. The device features balanced IF inputs, single-ended LO input and dual RF output for Cellular and PCS Systems respectively. The IC is manufactured on an advanced Silicon Bi-CMOS process and packaged in a 20-pin, 4mmx4mm, leadless chip carrier with an exposed die flag.

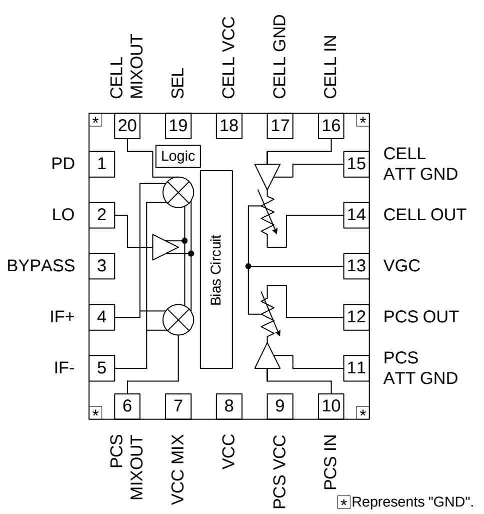


NOTES:
1 Shaded lead is Pin 1.
2 Pin 1 identifier must exist on top surface of package by identification mark or feature on the package body. Exact shape and size is optional.
3 Dimension applies to plated terminal: to be measured between 0.02 mm and 0.25 mm from terminal end.
4 Package Warpage: 0.05 mm max.
5 Die Thickness Allowable: 0.305 mm max.

Package Style: LCC, 20-Pin, 4x4

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single Supply 3.0V Operation
- Power Down Control
- Gain Control Range of 22dB
- Driver Amplifier Select Pin (RF Output Select)
- High Linearity in Mixer and Driver Amp

Ordering Information

RF2643	3V Dual-Band Upconverter and Driver Amplifier
RF2643 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

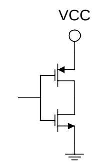
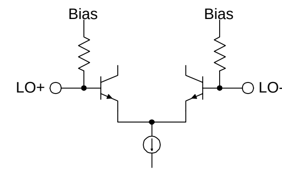
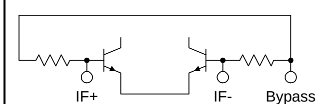
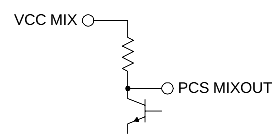
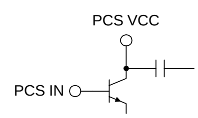
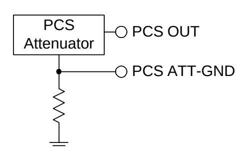
Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Input RF Power	+3	dBm
Operating Ambient Temperature	-30 to +80	°C
Storage Temperature	-30 to +150	°C

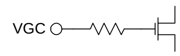
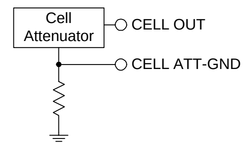
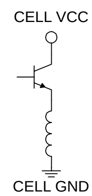
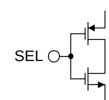
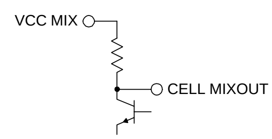
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Upconverter					
Both Bands					Unless stated otherwise, all data in this section is for both Cellular and PCS bands. T=25°C, V_{CC}=2.75V.
IF Frequency Range	100		250	MHz	
LO Input Level	-9	-6	-2	dBm	
RF to LO Isolation	20	30		dBm	
IF to RF Isolation	40			dBm	
IF to LO Isolation	34			dBm	
IF Input Impedance Differential		260		Ω	
IF Input Return Loss Differential	10			dB	
LO Input Impedance Single-Ended		50		Ω	
LO Input Return Loss Single-Ended	10			dB	
RF Output Impedance Single-Ended		50		Ω	
RF Output Return Loss Single-Ended	10			dB	
Cellular Band					RF=835MHz, LO=990MHz@-3dBm
RF Output Frequency	824		849	MHz	
LO Frequency Range	909		1099	MHz	
IF-RF Conversion Gain	-2	0	2	dB	
Noise Figure		12	13	dB	Room Temp.
		13	14		Over Temp.
Output IP3 (Linearity)	10.5	13.0		dBm	See Note 1 (end of parameter table).
Output P1dB	-3	-1		dBm	
LO to RF Output Leakage		-30		dBm	
PCS Band					RF=1880MHz, LO=2030MHz@-3dBm
RF Output Frequency	1850		1910	MHz	
LO Frequency Range	1950		2160	MHz	
IF-RF Conversion Gain	-2	0	2	dB	
Noise Figure		14.0	14.5	dB	Room Temp.
		15.0	16.5		Over Temp.
Output IP3 (Linearity)	8.5	12.0		dBm	See Note 1 (end of parameter table).
Output P1dB	-4	-2		dBm	
LO to RF Output Leakage		-17		dBm	

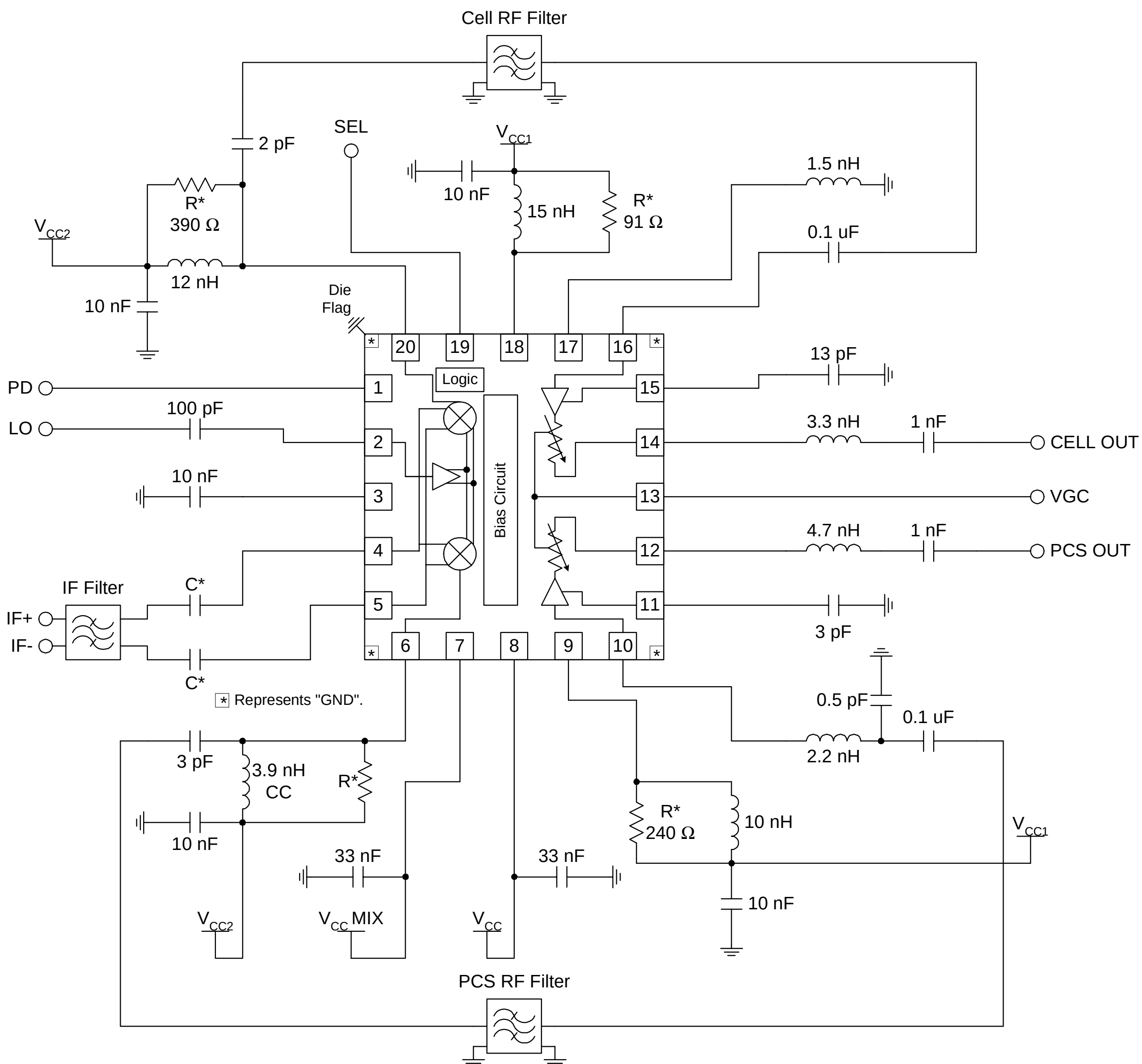
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Amplifiers/Attenuators					
Both Bands					Unless stated otherwise, all data in this section is for both Cellular and PCS bands. T=25°C, V_{CC}=2.75V.
Gain Control Range	17	20		dB	
Gain Control Voltage	0.8		1.9	V	
Gain Control Slope		15	35	dB/V	
Input Impedance Single-Ended		50		Ω	
Input Return Loss Single-Ended	10			dB	
Output Impedance Single-Ended		50		Ω	
Output Return Loss Single-Ended	10			dB	
RF Output Collector Current Consumption		10		mA	
Upconverter Output to Amplifier Input	35	40		dB	Any load.
Cellular Band					
RF Frequency Range	824		849	MHz	
Maximum Gain	5	7	9	dB	Amplifier + Attenuator
Noise Figure at Maximum Gain			2.5	dB	Amplifier + Attenuator
Noise Figure Increase with Attenuation			0.75	dB/dB	
Input IP3 (Linearity)	-1	1		dBm	@ all gain levels See Note 1 (end of parameter table).
PCS Band					
RF Frequency Range	1850		1910	MHz	
Maximum Gain	4	6	8	dB	Amplifier + Attenuator
Noise Figure at Maximum Gain			3.5	dB	Amplifier + Attenuator
Noise Figure Increase with Attenuation			0.75	dB/dB	
Input IP3 (Linearity)	-1	0		dBm	See Cellular Band Input IP3 Conditions.
Control and Power Consumption					Unless otherwise stated, all data in this section is for both Cellular and PCS bands.
Operating Voltage	2.7		3.0	V	
Power Down Control					
	2.1			V	HIGH (Device ON)
			0.5	V	LOW (Device OFF)
Power Down Pin Impedance	20			kΩ	
Band-Select Control (BS)	2.1			V	PCS (HIGH)
			0.5	V	Cellular (LOW)
Band Select Pin Impedance	20			kΩ	
Device OFF Current			10	uA	PD=LOW
Total Current (PD=HIGH)		30	37	mA	Cellular, BS=LOW
		33	42	mA	PCS, BS=HIGH

NOTE 1: OIP3 was measured using a two-tone test. Each injected tone had an input power (at the RF output of the upconverter) of -18dBm with a frequency spacing of 100kHz.

Pin	Function	Description	Interface Schematic
1	PD	Power Down Control. When Logic “high” (greater than 2.1V) the device is active and all circuits are operating. When logic “low” (less than 0.5V) the device is inactive and all circuits are turned off.	
2	LO	Single-ended LO input pin. This pin is internally DC biased and should be DC blocked if it is connected to a device with a DC level present. The single-ended input impedance is 50Ω.	
3	BYPASS	Bypass pin for internal bias circuitry. Bypass with 10nF capacitor.	
4	IF+	Balanced IF input pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. The differential input impedance is 260Ω. For single ended input operation, one pin is used as an input and the other IF input is AC coupled to ground.	
5	IF-	Same as pin 4, except complementary input.	
6	PCS MIXOUT	RF mixer output pin for the PCS system. PCS Mixout output impedance depends on the LC match and it is influenced by the bypass capacitor at VCC2.	
7	VCC MIX	Supply voltage pin for the mixer. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	VCC	Supply voltage pin for all the control and bias circuitry. A bias choke inductor and RF bypass capacitor is required.	
9	PCS VCC	Supply voltage pin for the PCS driver. This pin is an open collector and it will need a bias choke inductor and RF bypass. A parallel resistor to the inductor improves stability of the driver amplifier.	
10	PCS IN	Single-ended input for the PCS driver and attenuator. External matching is required. This pin is internally DC biased and should be DC blocked if it is connected to a device with a DC level present.	
11	PCS ATT GND	PCS attenuator ground pin. This pin should be AC ground. The trace length between the pin and the bypass capacitors should be minimized. The value of the capacitor is chosen to resonate in the PCS band.	
12	PCS OUT	PCS RF output pin. External matching is required. This pin is internally DC biased and should be DC blocked if it is connected to a device with a DC level present.	

Pin	Function	Description	Interface Schematic
13	**VGC**	Analog gain control for the driver amplifier. Valid control voltage ranges from 0.8V_{DC} to 1.9V_{DC}.	
14	**CELL OUT**	Cellular RF output pin. External matching is required. External matching is required. This pin is internally DC biased and should be DC blocked if it is connected to a device with a DC level present.	
15	**CELL ATT GND**	Cell attenuator ground pin. This pin should be AC ground. The trace length between the pin and the bypass capacitors should be minimized. The value of the capacitor is chosen to resonate in the PCS band.	
16	**CELL IN**	Singled end input for the cellular driver and attenuator. External matching is required. This pin is internally DC biased and should be DC blocked if it is connected to a device with a DC level present.	
17	**CELL GND**	This pin should be choke to ground. The inductor is used to adjust the linearity of the cellular driver.	
18	**CELL VCC**	Supply voltage pin for the cell driver. This pin is an open collector and it will need a bias choke inductor and RF bypass. A parallel resistor to the inductor improves stability of the driver amplifier.	
19	**SEL**	Band select control pin for the drivers. When Logic "high" (greater than 2.1V) the PCS band is active. When logic "low" (less than 0.5V) the Cellular Band is active.	
20	**CELL MIXOUT**	RF mixer output pin for the PCS system. PCS Mixout output impedance depends on the LC match and it is influenced by the bypass capacitor at VCC2.	
Pkg Base	**GND**	Ground connection. The backside of the package should be soldered to a top side ground pad, which is connected to the ground plane. Additional ground connections are offered at each corner of the package for flexibility in layout design.	

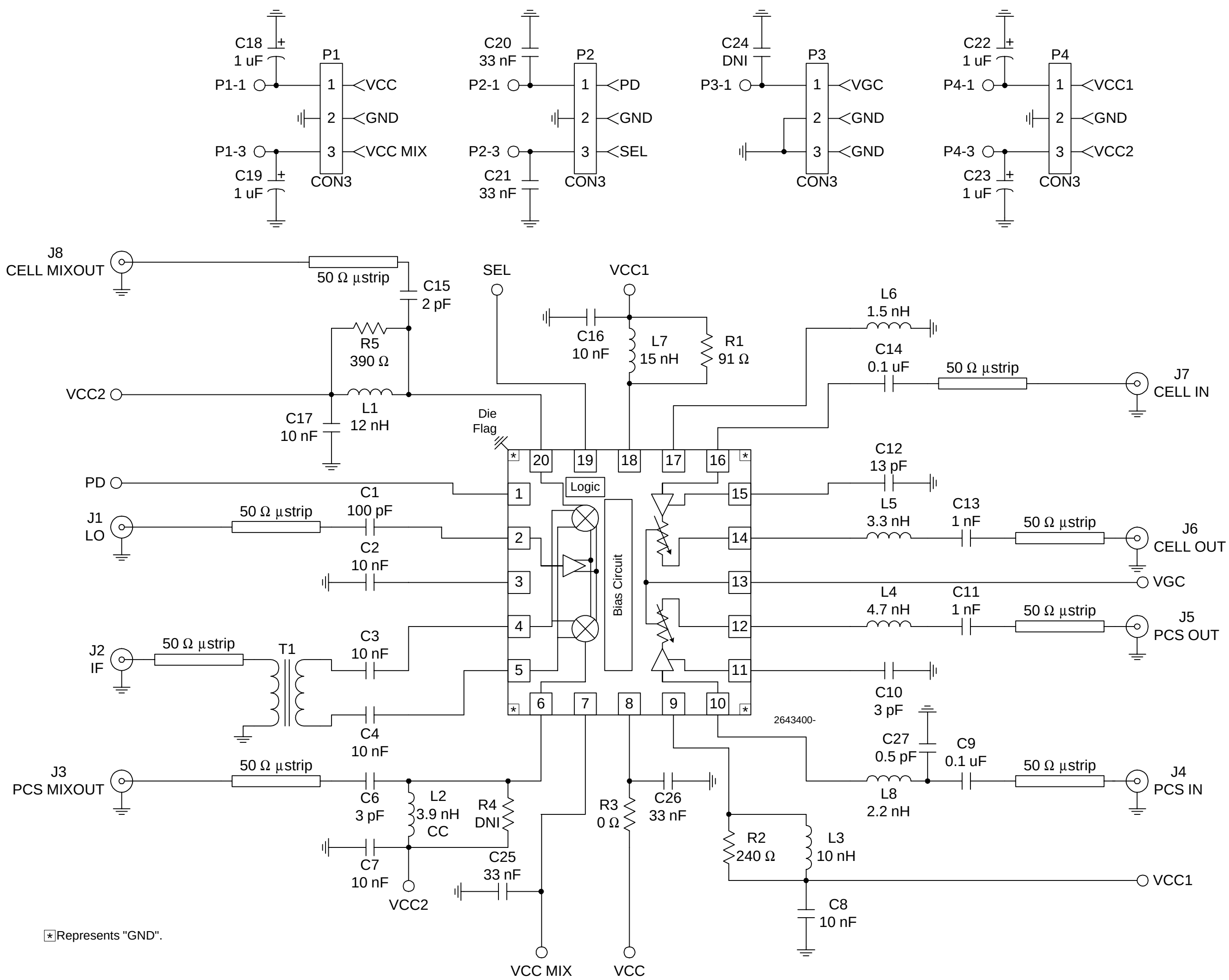
Application Schematic



NOTES:
1. All components marked with "R*" are De-Q resistors.
2. All components marked with "C*" should be present, if IF SAW filter has a direct path to ground.

Evaluation Board Schematic
IF=155 MHz

(Download Bill of Materials from www.rfmd.com.)

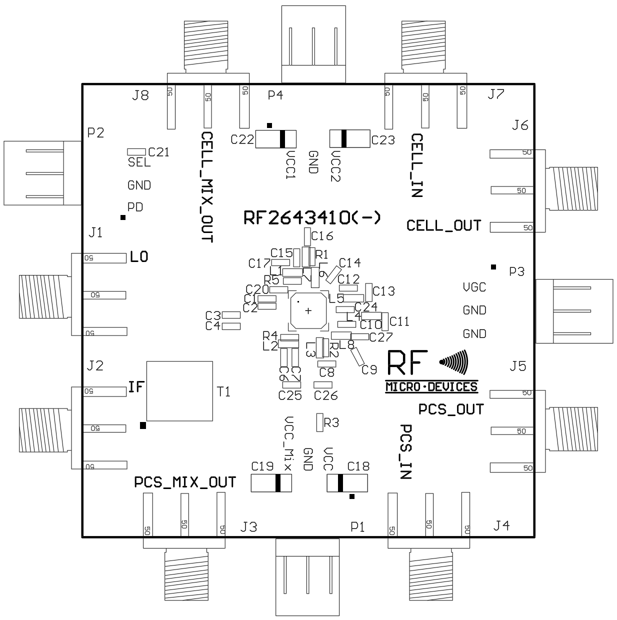


*Represents "GND".

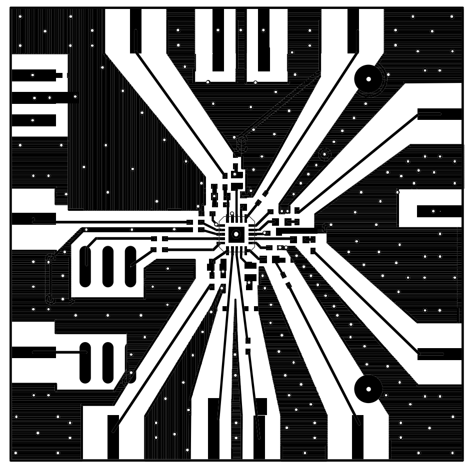
Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.064”, Board Material FR-4, Multi-Layer

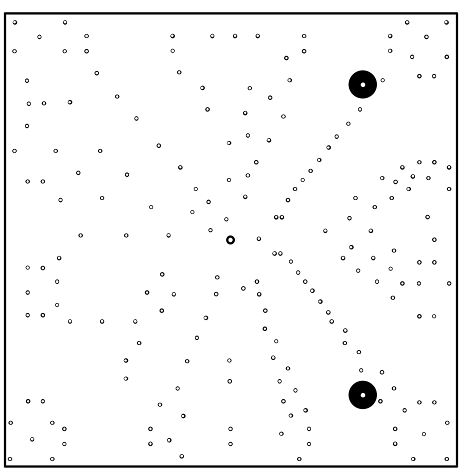
Assembly



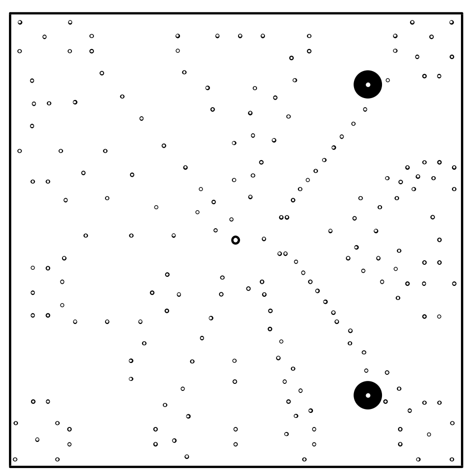
Top



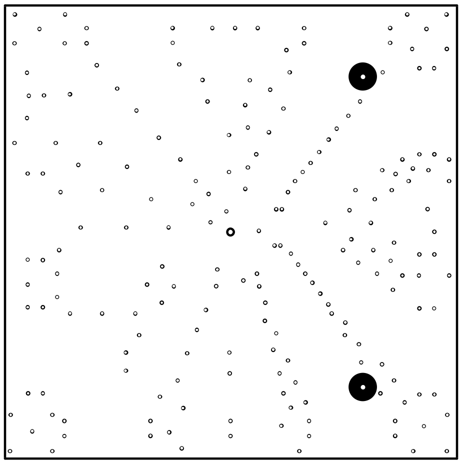
Inner 1 - Ground Plane 1



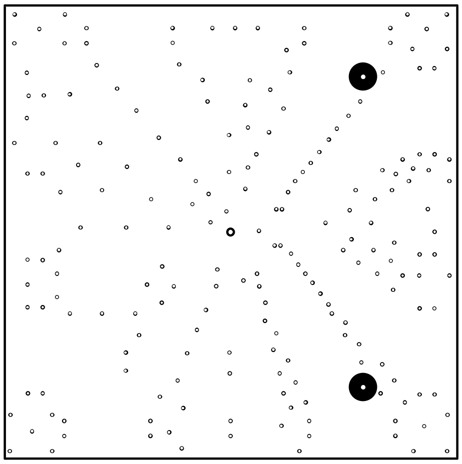
Inner 2 - Power Plane 1



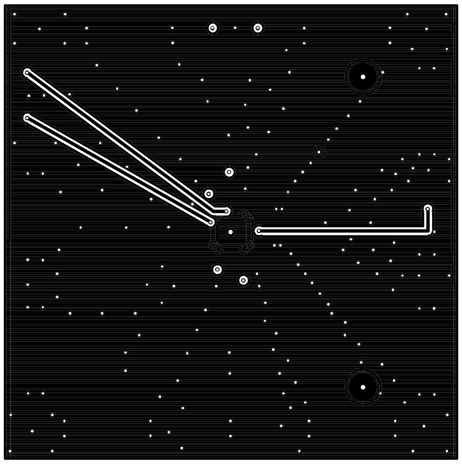
Inner 3 - Ground Plane 2



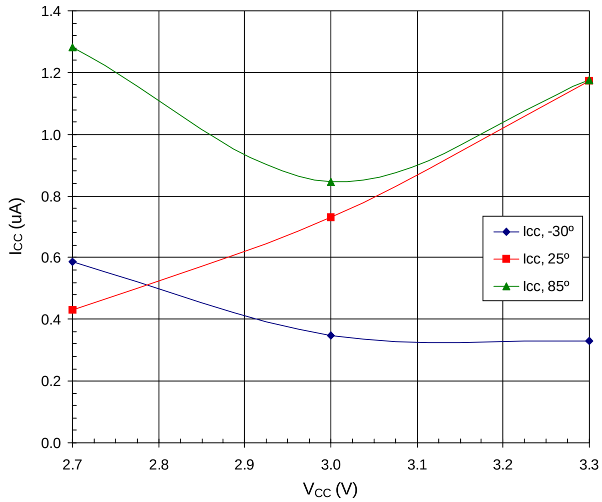
Inner 4 - Power Plane 2



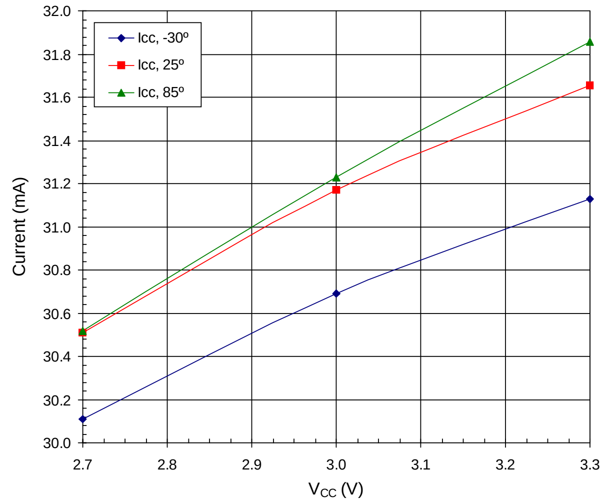
Back



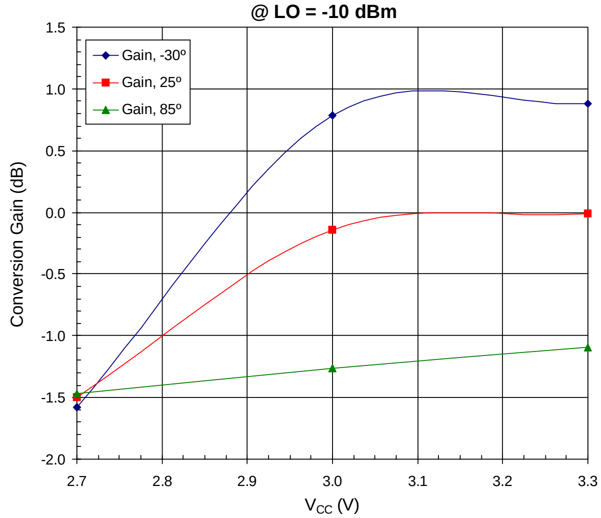
Power Down Current



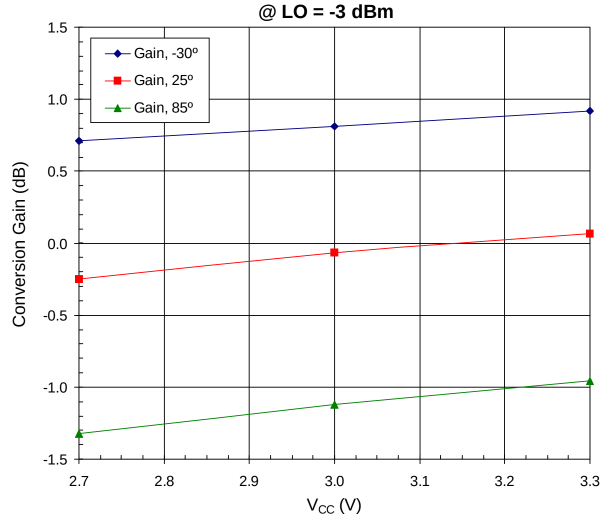
Cellular Current



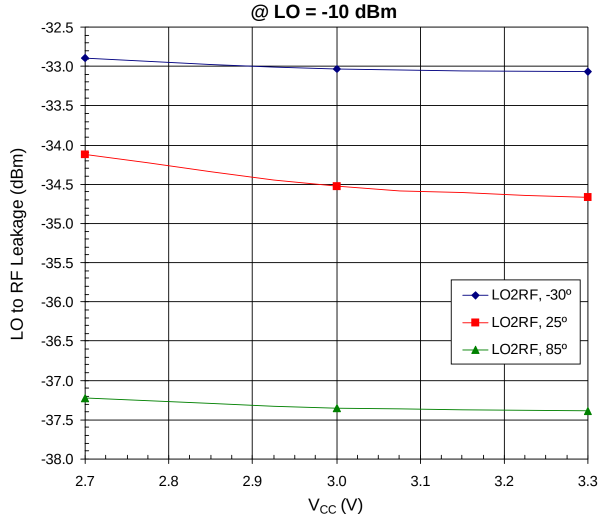
Cellular Mixer Conversion Gain @ LO = -10 dBm



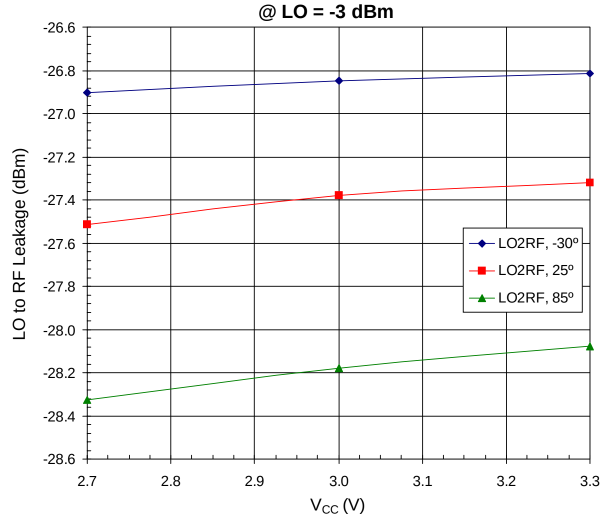
Cellular Mixer Conversion Gain @ LO = -3 dBm



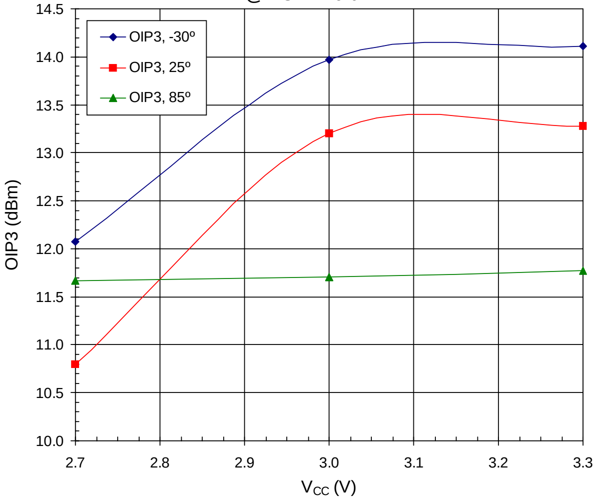
Cellular LO to RF Leakage @ LO = -10 dBm



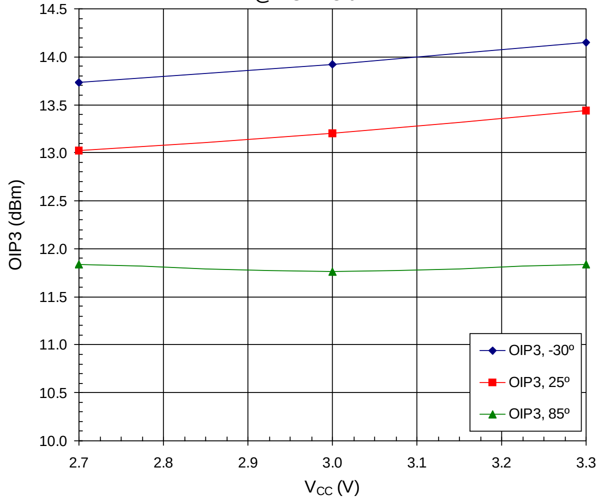
Cellular LO to RF Leakage @ LO = -3 dBm



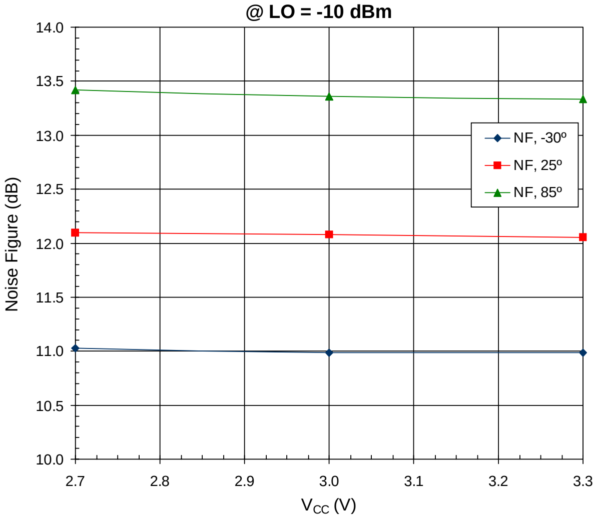
Cellular Mixer OIP3 @ LO = -10 dBm



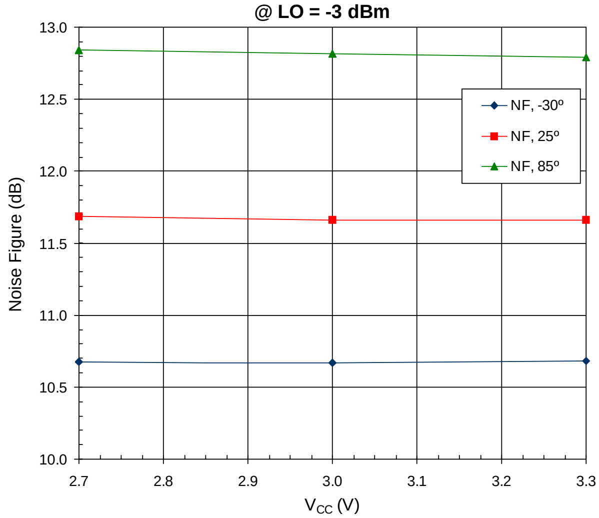
Cellular Mixer OIP3 @ LO = -3 dBm



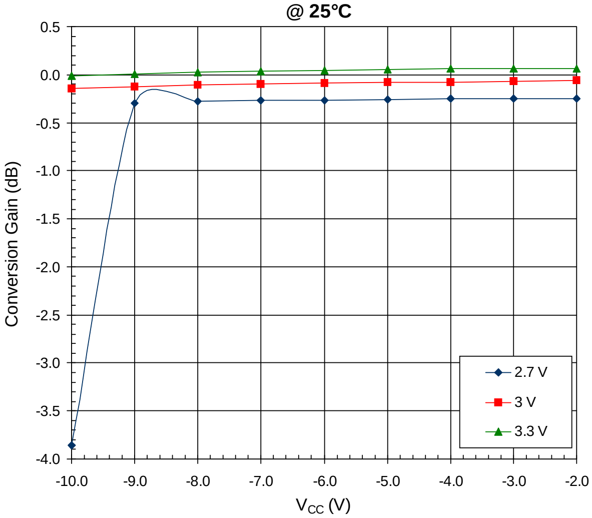
Cellular Mixer Noise Figure @ LO = -10 dBm



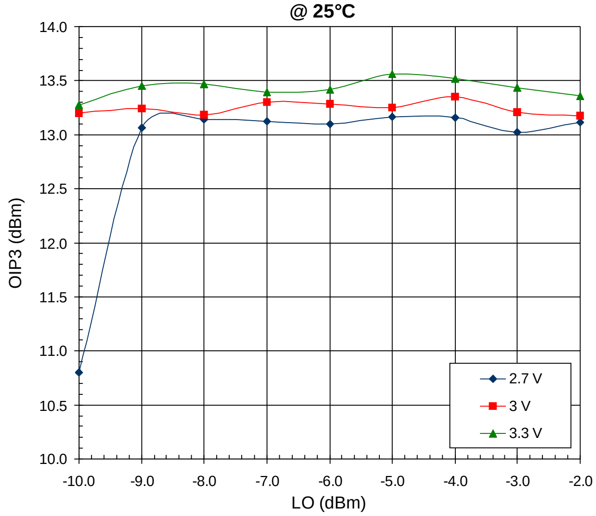
Cellular Mixer Noise Figure @ LO = -3 dBm



Cellular Mixer Gain @ 25°C

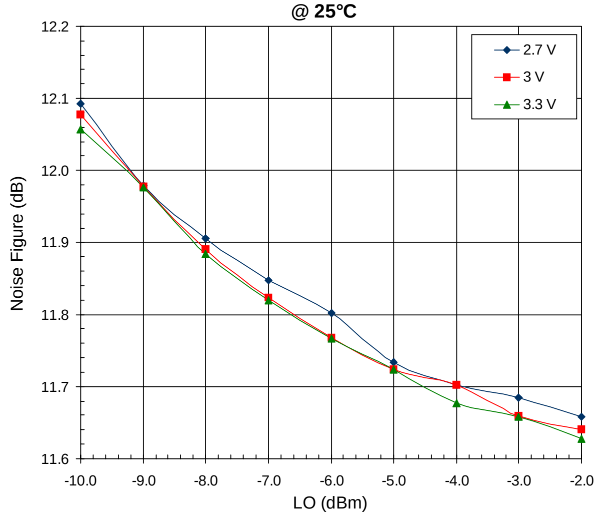


Cellular Mixer OIP3 @ 25°C

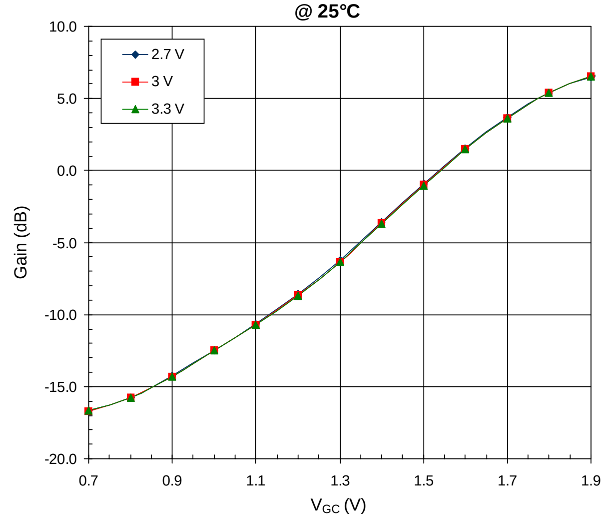


6 MIXERS

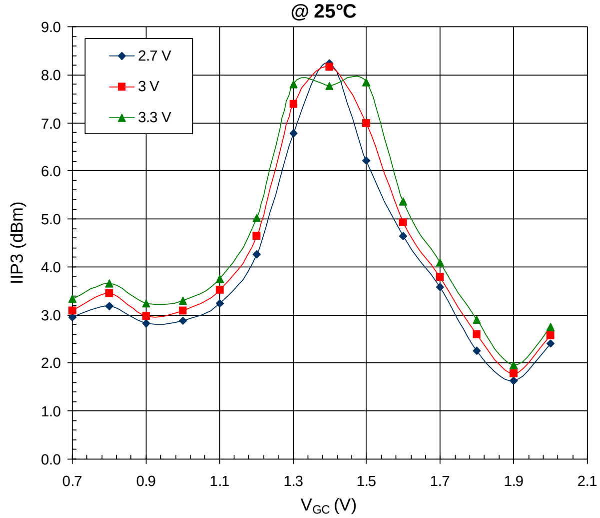
Cellular Mixer Noise Figure @ 25°C



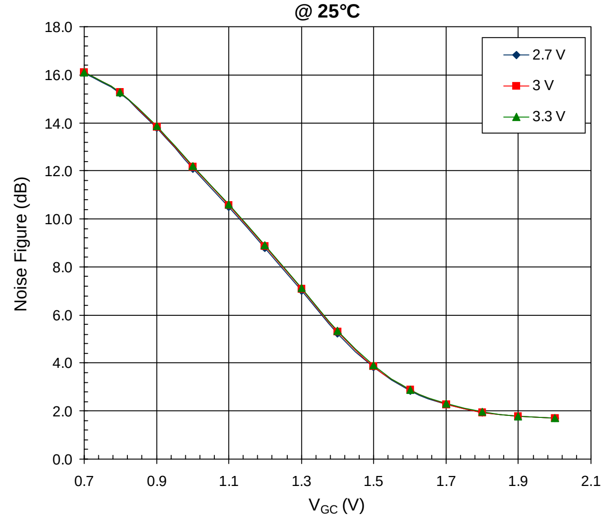
Cellular Gain Driver @ 25°C



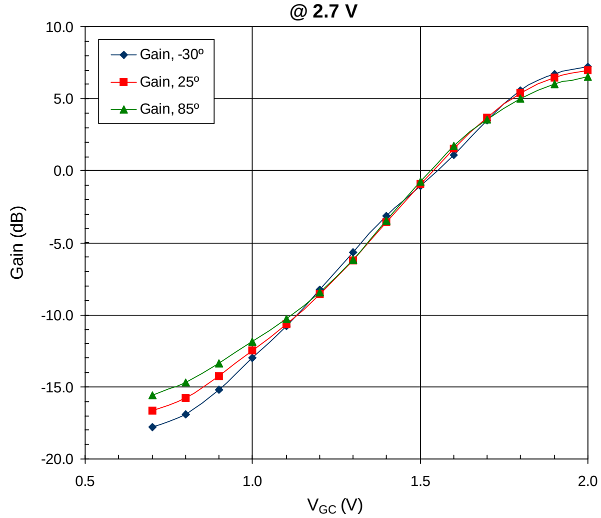
Cellular Driver IIP3 @ 25°C



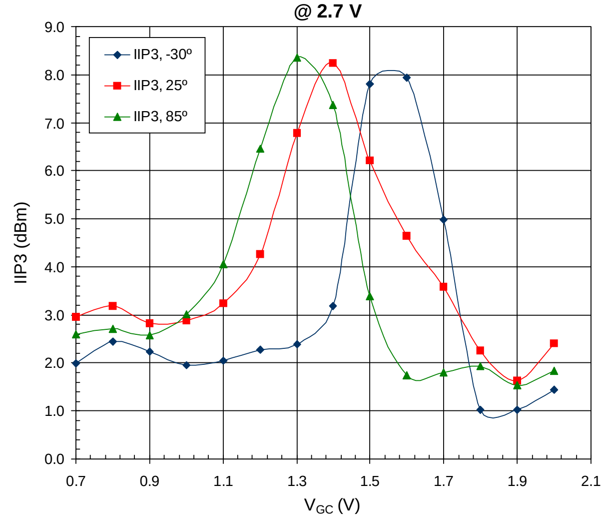
Cellular Noise Figure Driver @ 25°C

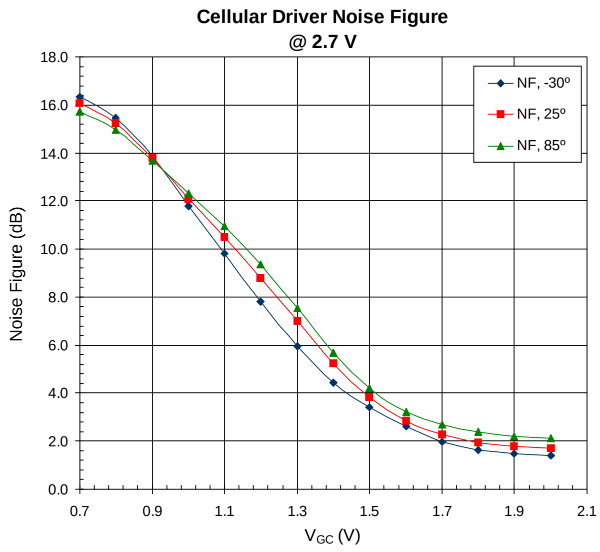


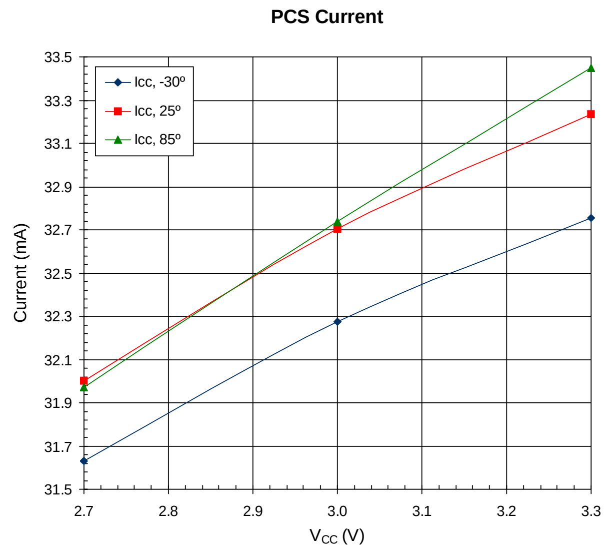
Cellular Gain Driver @ 2.7 V

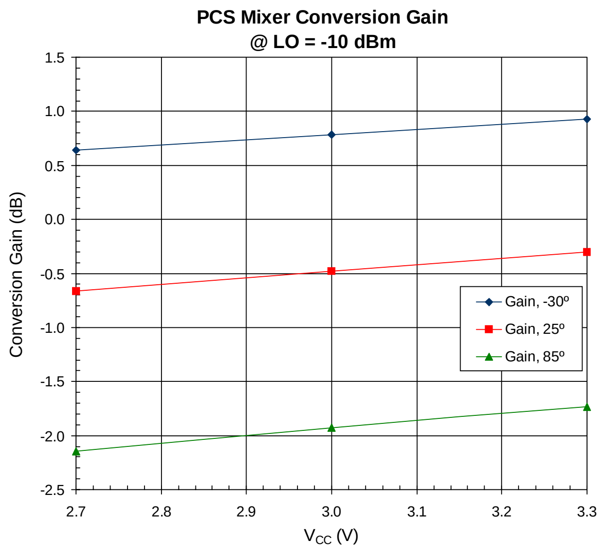


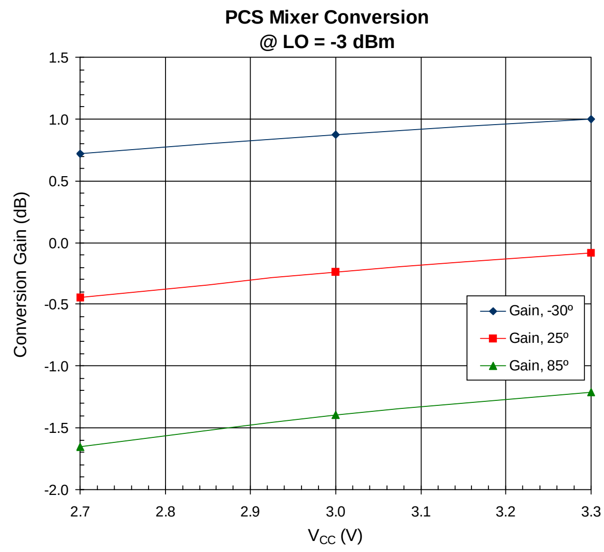
Cellular Driver IIP3 @ 2.7 V

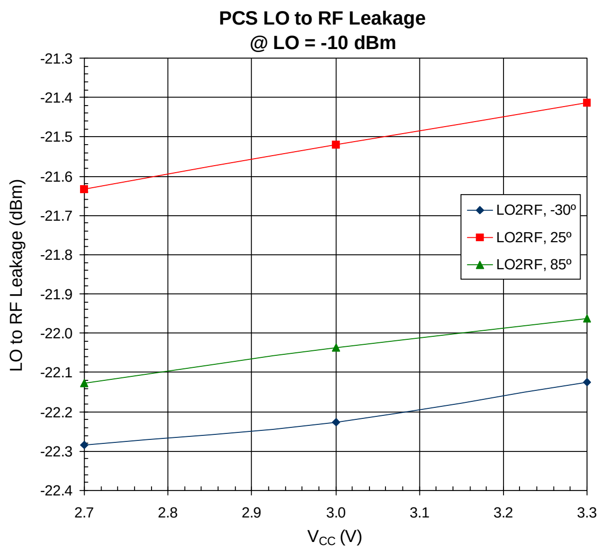


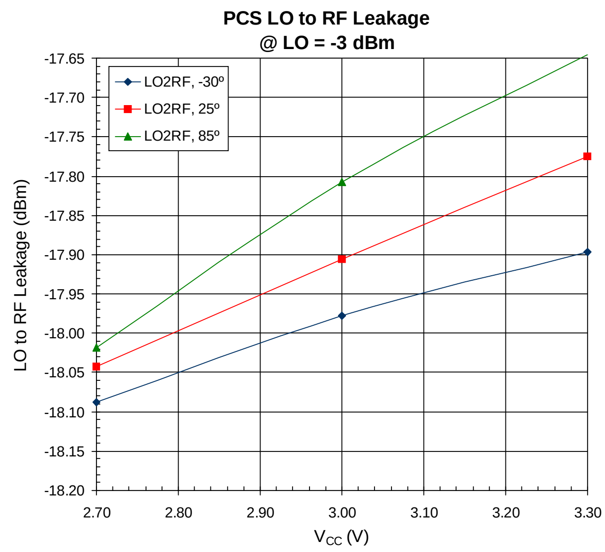

Cellular Driver Noise Figure
@ 2.7 V
Noise Figure (dB)
V_{GC} (V)
NF, -30º
NF, 25º
NF, 85º


PCS Current
Current (mA)
V_{CC} (V)
Icc, -30º
Icc, 25º
Icc, 85º


PCS Mixer Conversion Gain
@ LO = -10 dBm
Conversion Gain (dB)
V_{CC} (V)
Gain, -30º
Gain, 25º
Gain, 85º

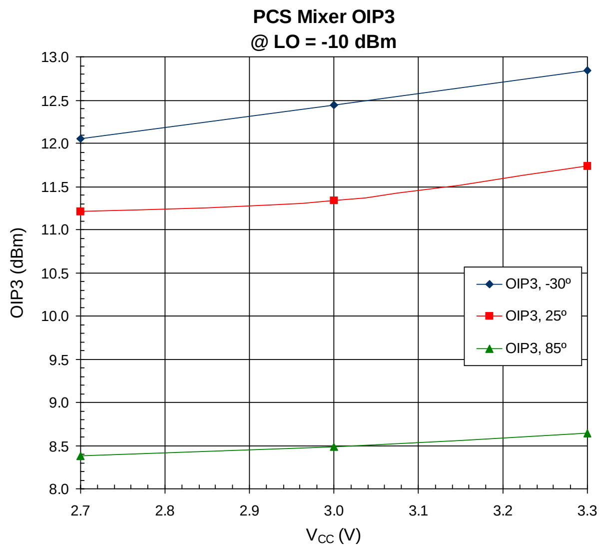

PCS Mixer Conversion
@ LO = -3 dBm
Conversion Gain (dB)
V_{CC} (V)
Gain, -30º
Gain, 25º
Gain, 85º

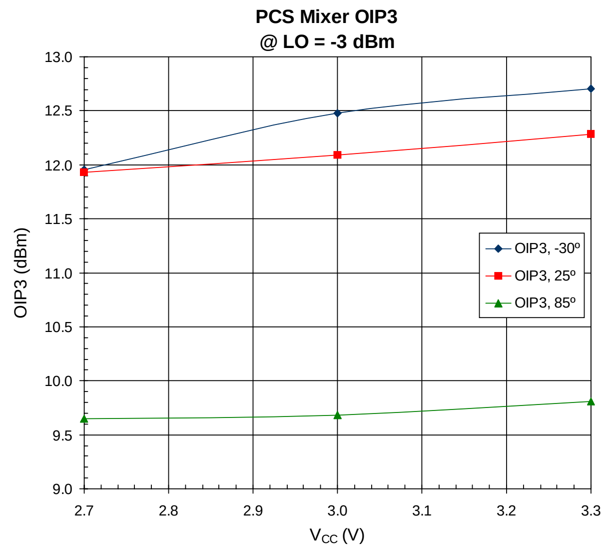

PCS LO to RF Leakage
@ LO = -10 dBm
LO to RF Leakage (dBm)
V_{CC} (V)
LO2RF, -30º
LO2RF, 25º
LO2RF, 85º

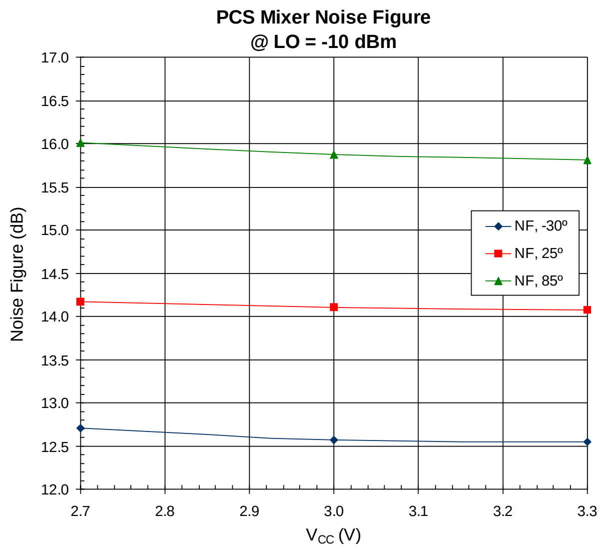

PCS LO to RF Leakage
@ LO = -3 dBm
LO to RF Leakage (dBm)
V_{CC} (V)
LO2RF, -30º
LO2RF, 25º
LO2RF, 85º

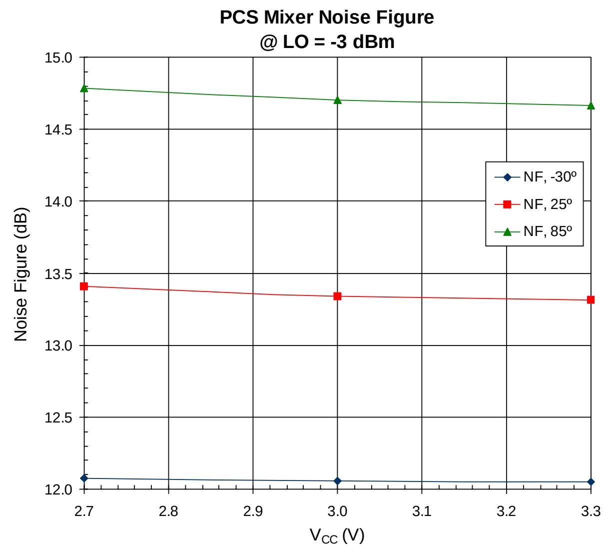
6

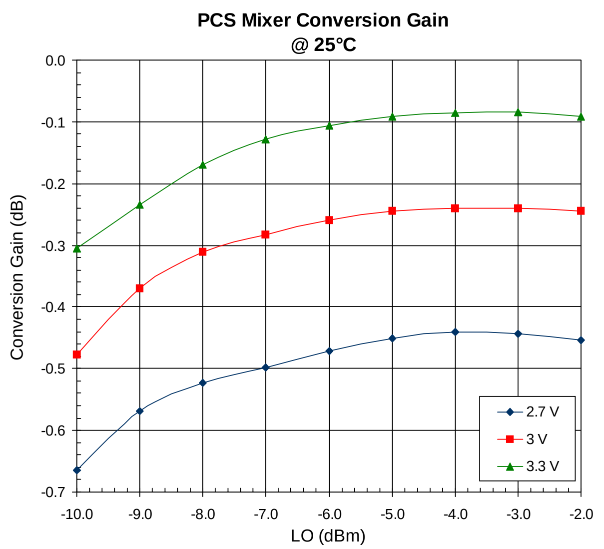
MIXERS

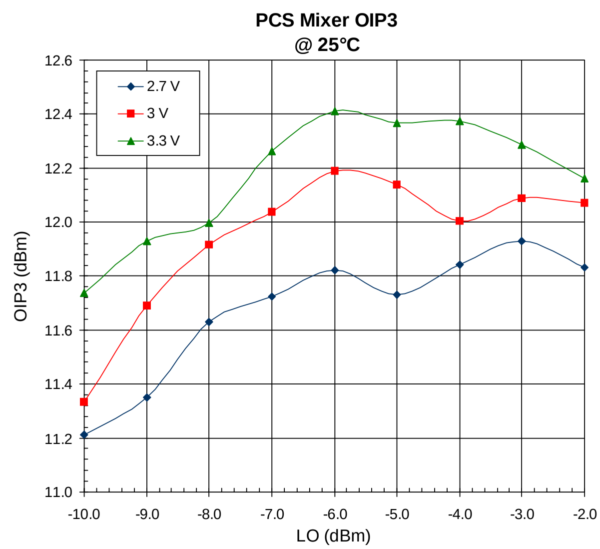

PCS Mixer OIP3
@ LO = -10 dBm
OIP3 (dBm)
VCC (V)
OIP3, -30º
OIP3, 25º
OIP3, 85º


PCS Mixer OIP3
@ LO = -3 dBm
OIP3 (dBm)
VCC (V)
OIP3, -30º
OIP3, 25º
OIP3, 85º

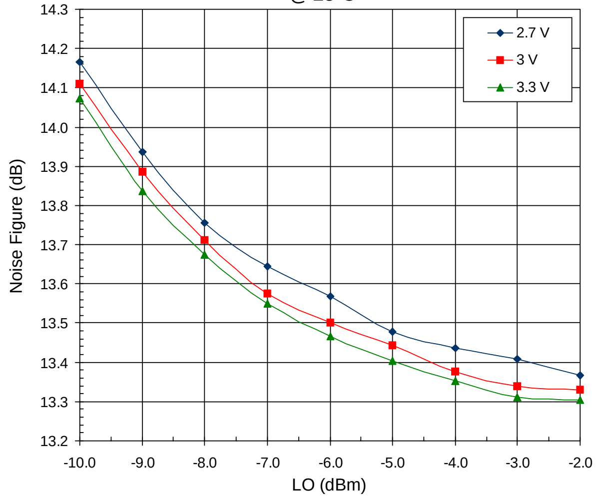

PCS Mixer Noise Figure
@ LO = -10 dBm
Noise Figure (dB)
VCC (V)
NF, -30º
NF, 25º
NF, 85º


PCS Mixer Noise Figure
@ LO = -3 dBm
Noise Figure (dB)
VCC (V)
NF, -30º
NF, 25º
NF, 85º

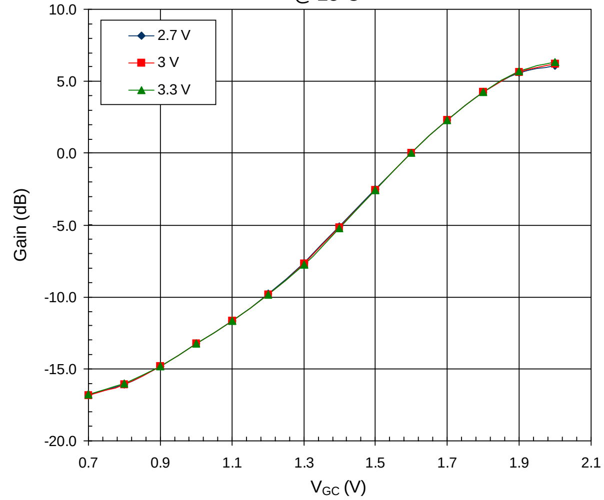

PCS Mixer Conversion Gain
@ 25°C
Conversion Gain (dB)
LO (dBm)
2.7 V
3 V
3.3 V


PCS Mixer OIP3
@ 25°C
OIP3 (dBm)
LO (dBm)
2.7 V
3 V
3.3 V

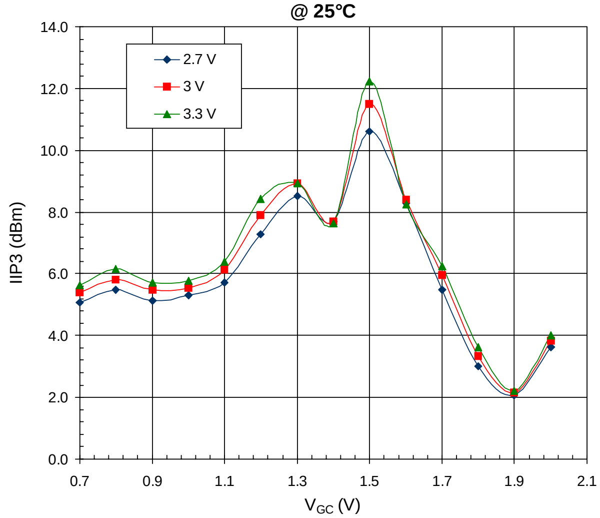
PCS Mixer Noise Figure @ 25°C



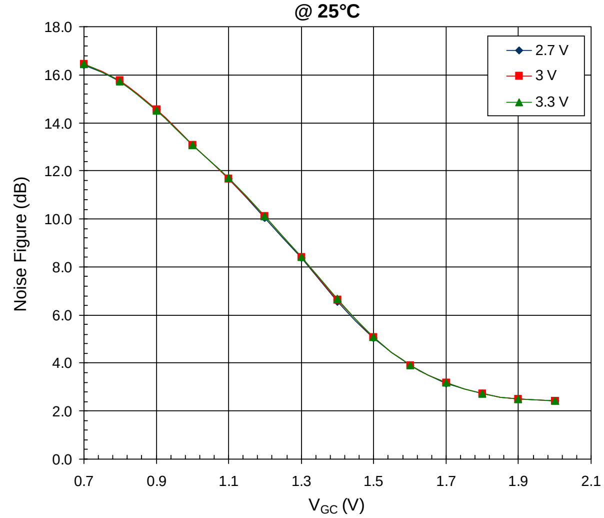
PCS Gain Driver @ 25°C



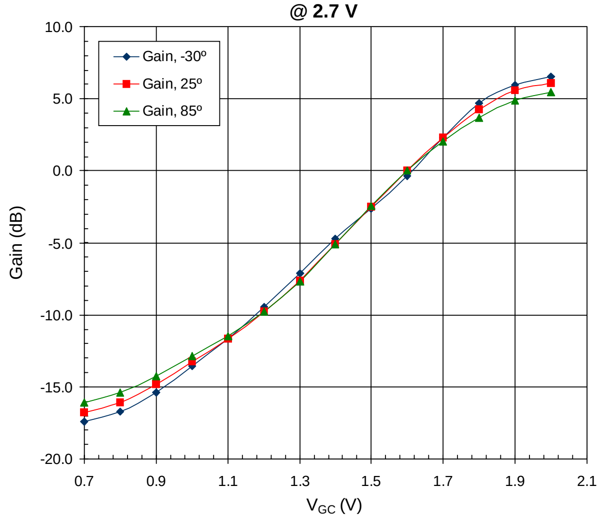
PCS IIP3 Driver @ 25°C



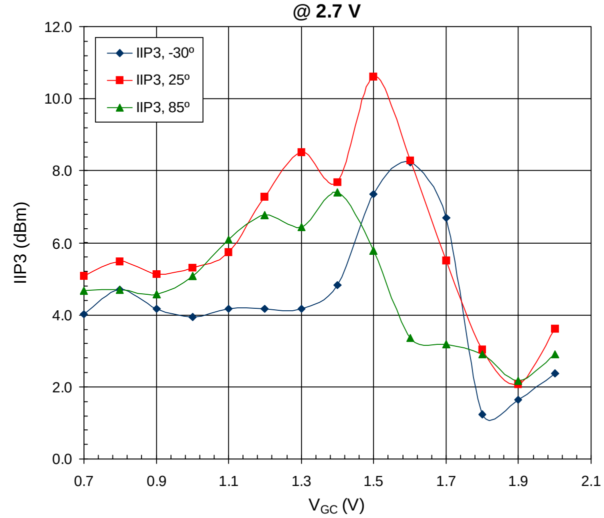
PCS Noise Figure Driver @ 25°C

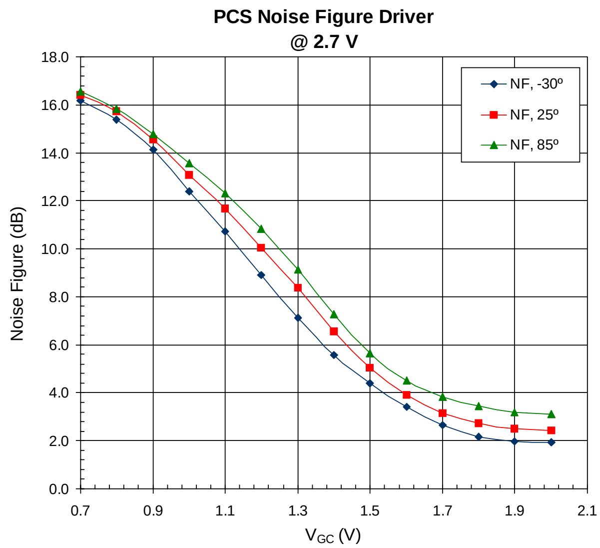


PCS Gain Driver @ 2.7 V



PCS IIP3 Driver @ 2.7 V




PCS Noise Figure Driver
@ 2.7 V
Noise Figure (dB)
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.7
0.9
1.1
1.3
1.5
1.7
1.9
2.1
VGC (V)
NF, -30º
NF, 25º
NF, 85º