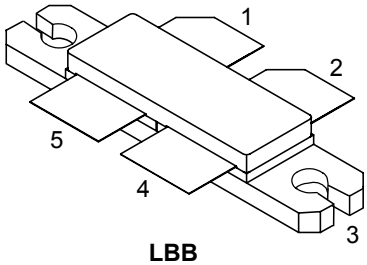
RF2L15200CB4

Datasheet

200 W, 28 V, HF to 1.5 GHz RF power LDMOS transistor



LBB

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF2L15200CB4	860 MHz	28 V	200 W	17.5 dB	72%

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the european directive 2002/95/EC

Applications

- Broadband commercial communications
- TV broadcast
- Avioncs
- Industrial

Description

The RF2L15200CB4 is a 200 W LDMOS FET, designed for wideband communication and ISM applications with frequencies from HF to 1.5 GHz. It can be used in class AB, B or C for all typical modulation formats.

Product status link
RF2L15200CB4

Product summary	
Order code	RF2L15200CB4
Marking	2L15200
Package	LBB
Packing	Tape and reel 13"
Base/bulk quantity	100/100

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C= 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Maximum operating voltage	32	V
T_J	Maximum junction temperature	+200	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC} (1)	Thermal resistance, junction-to-case	0.35	°C/W

1. *T_C = +85 °C , T_J = +200 °C, DC test.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	1C
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

T_C = 25°C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_{DS} = 500 µA	65			V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 28 V			1	µA
		V_{GS} = 0 V, V_{DS} = 50 V				
I_{GSS}	Gate-source leakage current	V_{GS}=-6/10 V, V_{DS}=0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 28 V, I_{DS} = 600 µA	1.75		2.5	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 1 V, I_{DS} = 220 mA	2		4	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_{DS} = 820 mA	50		150	mV
		V_{GS} = 10 V, I_{DS} = 2.5 A	200		365	
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, I_{DS} = 820 mA			1	Ω
		V_{GS} = 10 V, I_{DS} = 2.5 A				
C_{ISS}	Common source input capacitance	V_{GS} = 0 V, V_{DD} = 28 V, f = 1 MHz		92		pF
C_{RSS}	Common source feedback capacitance			1.6		
C_{OSS}	Common source output capacitance			39		

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		-		1500	MHz
P_{OUT}	Output power	f = 860 MHz, at 3dB compression point, CW test signal	-	200		W
G_{PS}	Power gain		-	17.5		dB
η_D	Drain efficiency		-	72		%
VSWR	Load mismatch	At 200 W output power, all phase angles	-		10:1	

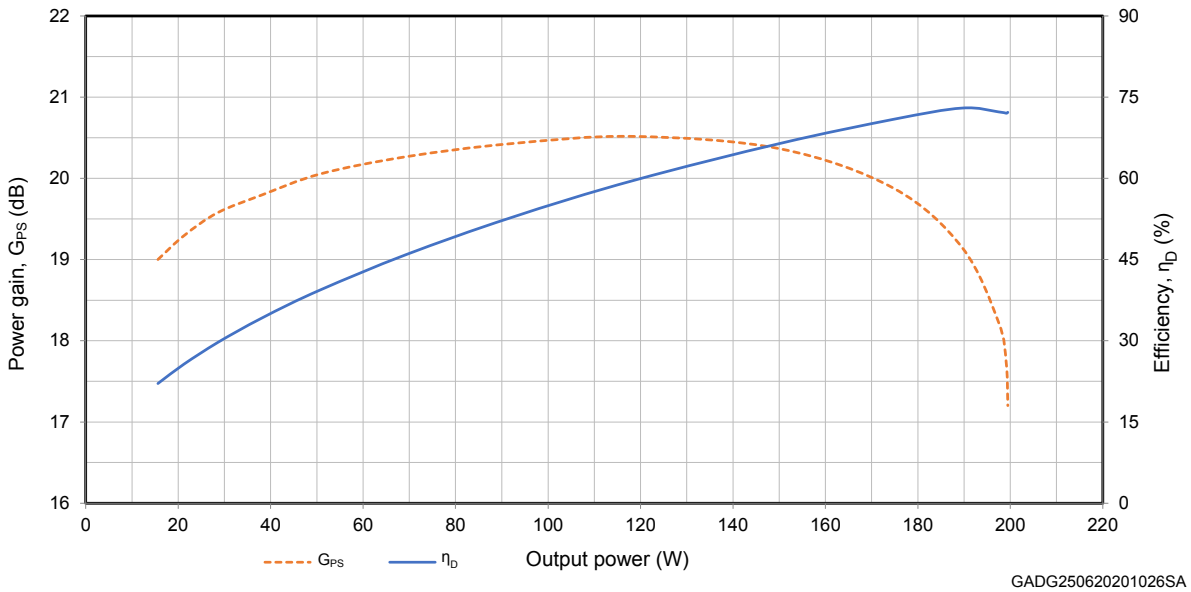
Note: V_{DD} = 28 V, I_{DQ} = 100 mA.

3 Typical performances

Table 6. Output power, power gain and drain efficiency vs input power (f= 860 MHz, CW)

P_{IN} (dBm)	P_{OUT} (dBm)	P_{OUT} (W)	I_{DS} (A)	G_{PS} (dB)	η_D (%)
22.9	41.9	15.6	2.5	19.0	22.1
24.0	43.3	21.2	3.0	19.3	25.7
25.0	44.6	28.5	3.4	19.6	29.7
26.0	45.8	38.1	4.0	19.8	34.2
27.0	47.1	50.8	4.6	20.1	39.4
28.1	48.4	69.3	5.4	20.3	45.9
29.2	49.6	91.7	6.2	20.4	52.7
30.2	50.7	118.6	7.1	20.5	59.6
31.4	51.8	150.3	8.1	20.4	66.5
32.5	52.4	174.8	8.8	19.9	70.9
33.6	52.8	189.5	9.3	19.1	73.0
34.7	53.0	197.4	9.8	18.2	72.3
35.3	53.0	199.1	9.9	17.7	72.0
35.8	53.0	199.4	9.9	17.2	72.2

Figure 1. Power gain and drain efficiency versus output power (f = 860 MHz, CW)

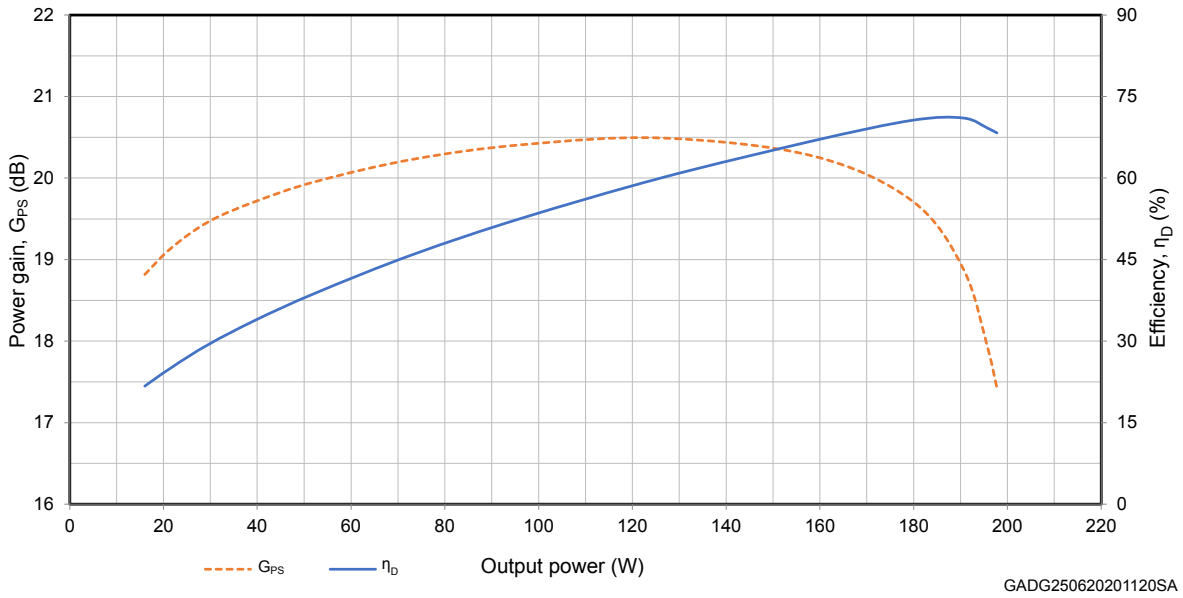


Note: *V_{DD} = 50 V, I_{DQ} =100 mA.*

Table 7. Output power, power gain and drain efficiency vs input power (f= 860 MHz, pulsed CW)

P_{IN} (dBm)	P_{OUT} (dBm)	P_{OUT} (W)	I_{DS} (A)	G_{PS} (dB)	η_D (%)
42.0	34.2	16.0	2.6	18.8	21.7
43.3	34.9	21.6	3.1	19.1	25.1
44.7	35.6	29.5	3.6	19.5	29.4
46.0	36.2	39.5	4.2	19.7	33.8
47.2	36.8	52.5	4.8	20.0	38.9
48.7	37.6	73.5	5.7	20.2	46.0
49.9	38.2	96.6	6.6	20.4	52.7
51.0	38.8	126.3	7.5	20.5	60.1
52.0	39.3	158.5	8.5	20.3	66.8
52.5	39.6	179.8	9.1	19.7	70.6
52.8	39.8	190.6	9.6	18.9	71.1
52.9	40.0	195.7	10.1	17.9	69.2
53.0	40.1	197.8	10.3	17.4	68.3

Figure 2. Power gain and drain efficiency versus output power (f = 860 MHz, pulsed CW)



Note: V_{DD}= 28 V, I_{DQ}= 100 mA pulsed CW; pulse width = 100 µs, duty cycle = 10%.

4 Test circuits

Figure 3. **Test circuit layout (f = 860 MHz)**

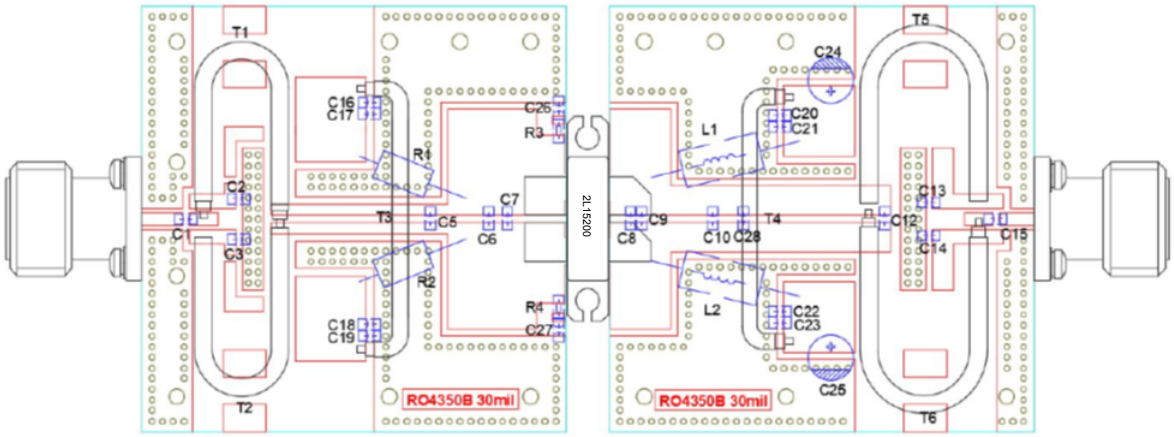


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Figure 4. **Test circuit photo (f = 860 MHz)**

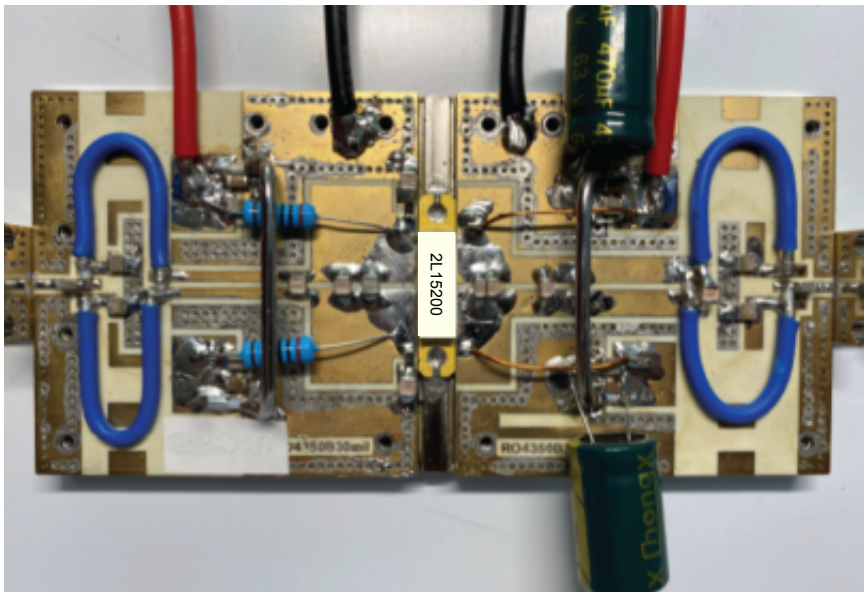

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Table 8. Components list

Component	Value	Reference/suggested manufacturer
C1, C2, C3, C13, C14, C15, C17, C18, C21, C22, C26, C27	120 pF	ATC800B
C5	6.8 pF	ATC800B
C6	5.6 pF	ATC800B
C7	10 pF	ATC800B
C12	3.3 pF	ATC800B
C8, C9, C10, C28	8.2 pF	ATC800B
C16, C19, C20, C23	10 µF	100V, ceramic multilayer capacitor
R1, R2	200 Ω	Metal film resistor
R4, R5	13 Ω	1206 chip resistor
L1, L2		Copper wire, cross section diameter 0.8 mm
C24, C25	470 µF	Electrolytic capacitor, 63 V
PCB	0.762 mm [0.030"] thick, Ɛr= 3.48, Rogers RO4350B, 1 oz. copper	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LBB package information

Figure 5. LBB package outline

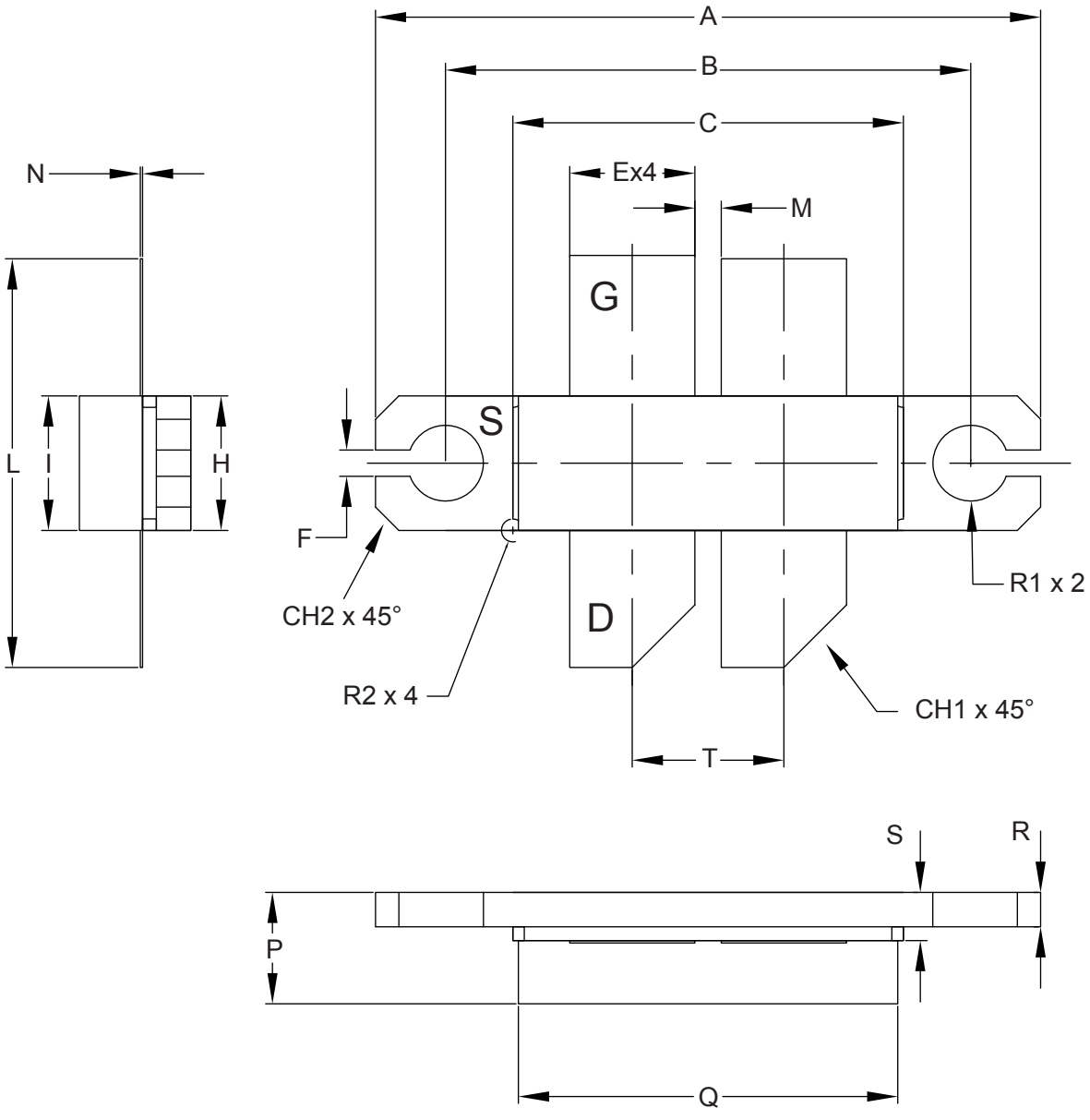
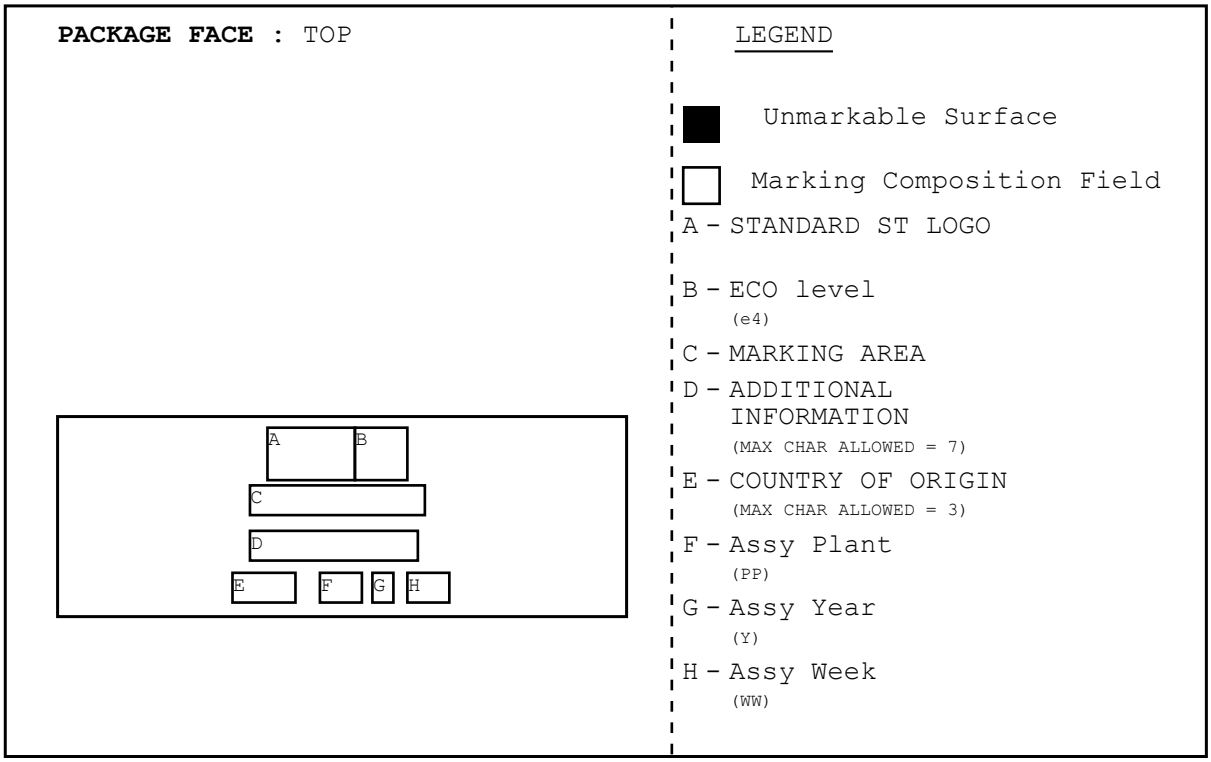


Table 9. **LBB mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A	28.82	28.95	29.08
B	22.73	22.86	22.99
C	16.87	17.00	17.13
E	5.32	5.45	5.58
F	1.01	1.14	1.27
H	5.72	5.85	5.98
I	5.72	5.85	5.98
L	17.65	17.78	17.91
M	1.02	1.15	1.28
N		0.10	
P	4.72	4.85	4.98
Q	16.38	16.51	16.64
R	1.37	1.50	1.63
S	1.97	2.10	2.23
T		6.60	
CH1		2.72	
CH2		1.02	
R1		1.65	
R2		0.50	

6 Marking information

Figure 6. Marking composition



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Revision history

Table 10. **Document revision history**

Date	Version	Changes
01-Jul-2020	1	First release.
15-Apr-2021	2	Modified gain, efficiency and marking values on cover page. Modified Table 1. Absolute maximum ratings (T_C= 25 °C), Table 3. ESD protection, Table 4. Static and Table 5. Dynamic. Modified Figure 1. Power gain and drain efficiency versus output power (f = 860 MHz, CW) and Figure 2. Power gain and drain efficiency versus output power (f = 860 MHz, pulsed CW). Modified the entire Section 4 Test circuits. Added Section 6 Marking information. Minor text changes.

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