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Proposed

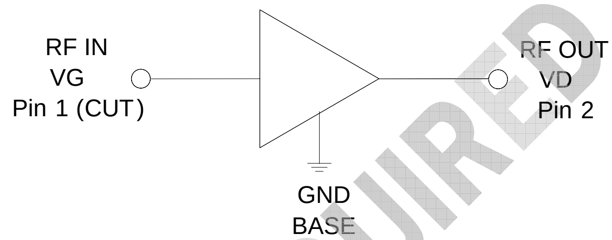
RF3928

300W GaN WIDE-BAND PULSED POWER AMPLIFIER

Package: Flanged Ceramic, 2 pin

Features

- Wideband Operation 2.8GHz to 3.4GHz
- Advanced GaN HEMT Technology
- Advanced Heat-Sink Technology
- Optimized Evaluation Board Layout for 50ohm Operation
- Integrated matching components for high terminal impedances
- 50V Operation Typical Performance
  - Pulsed Output Power 300W
  - Small Signal Gain 11dB
  - Drain Efficiency 50%
  - -40°C to 85°C Operating Temperature



Functional Block Diagram

Applications

- Radar
- Air Traffic Control and Surveillance
- General Purpose Broadband Amplifiers

Product Description

The RF3928 is a 50V 300W high power discrete amplifier designed for S-Band pulsed radar, Air Traffic Control and Surveillance and general purpose broadband amplifier applications. Using an advanced high power density Gallium Nitride (GaN) semiconductor process, these high-performance amplifiers achieve high output power, high efficiency and flat gain over a broad frequency range in a single package. The RF3928 is a matched GaN transistor packaged in a hermetic, flanged ceramic package. This package provides excellent thermal stability through the use of advanced heat sink and power dissipation technologies. Ease of integration is accomplished through the incorporation of simple, optimized matching networks external to the package that provide wideband gain and power performance in a single amplifier

Ordering Information

RF3928	300W GaN Wide-Band Pulsed Power Amplifier
RF3928PCBA-410	Fully Assembled Evaluation Board Optimized for 2.8-3.5GHz; 50V

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☒ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Source Voltage	150	V
Gate Source Voltage	-5 to +2	V
Gate Current (Ig)	155	mA
Operational Voltage	50	V
Ruggedness (VSWR)	3:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_L)	-40 to +85	°C
Operating Junction Temperature (T_J)	200	°C
Human Body Model	Class 1A	
MTTF (T_J < 200 °C)	3.0E + 06	Hours
Thermal Resistance, Rth (junction to case) T_C =85°C, DC bias only T_C =85°C, 100mS pulse, 10% duty cycle	 0.89 0.27	°C/W

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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* MTTF – median time to failure for wear-out failure mode (30% Idss degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT(random) failure rate.

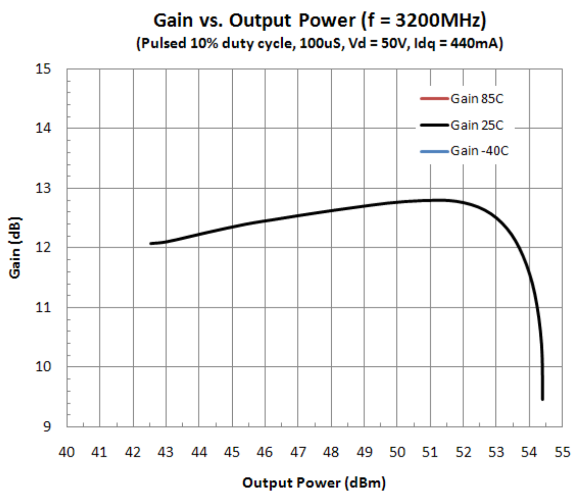
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page two.

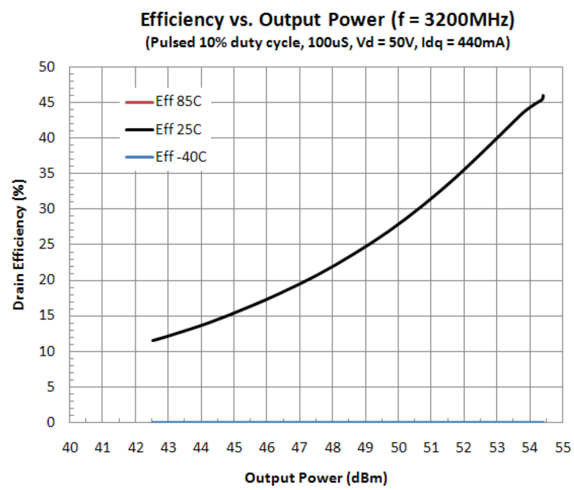
Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J – T_C) / R_{TH}$ J-C and $T_C = T_{CASE}$

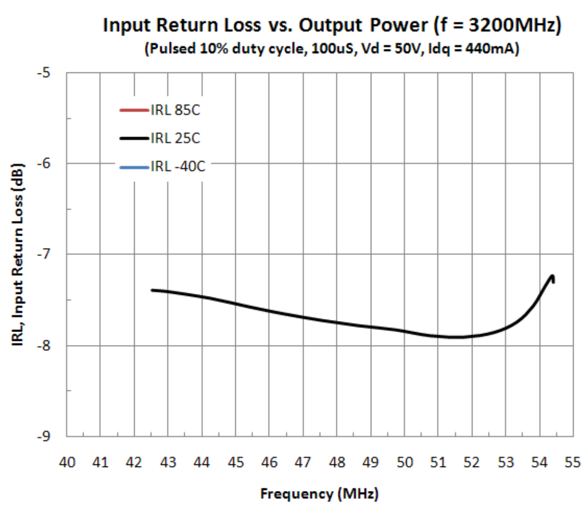
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Drain Voltage (V_{dsq})			50	V	
Gate Voltage (V_{gsq})	-5	-3	-2	V	
Drain Bias Current		440		mA	
Frequency of Operation	2800		3400	MHz	
Capacitance					
Crss		TBD		pF	Vg= -8V, Vd = 0V
Ciss		TBD		pF	Vg= -8V, Vd = 0V
Coss		TBD		pF	Vg= -8V, Vd = 0V
DC Functional Test					
Ig (off) – Gate Leakage			2	mA	Vg = -8V, Vd = 0V
Id (off) – Drain Leakage			2.5	mA	Vg = -8V, Vd = 36V
Vgs (th) – Threshold Voltage		-4.2		V	Vd = 36V, Id = 40mA
Vds (on) – Drain Voltage at high current		0.13		V	Vg = 0V, Id = 1.5A
RF Functional Test					
Small Signal Gain		12		dB	f=2800MHz, Pin = 30dBm [1,2]
Power Gain	9	9.9		dB	f=2800MHz, Pin = 45dBm [1,2]
Input Return Loss			-5.5	dB	f=2800MHz, Pin = 30dBm [1,2]
Output Power	54	54.9		dBm	f=2800MHz, Pin = 45dBm [1,2]
Drain Efficiency	45	53		%	f=2800MHz, Pin = 45dBm [1,2]
Small Signal Gain		12		dB	f=3100MHz, Pin = 30dBm [1,2]
Power Gain	9	9.5		dB	f=3100MHz, Pin = 45dBm [1,2]
Input Return Loss			-5.5	dB	f=3100MHz, Pin = 30dBm [1,2]
Output Power	54	54.5		dBm	f=3100MHz, Pin = 45dBm [1,2]
Drain Efficiency	45	56		%	f=3100MHz, Pin = 45dBm [1,2]
Small Signal Gain		10		dB	f=3400MHz, Pin = 30dBm [1,2]
Power Gain	9	9.3		dB	f=3400MHz, Pin = 45dBm [1,2]
Input Return Loss			-5.5	dB	f=3400MHz, Pin = 30dBm [1,2]
Output Power	54	54.3		dBm	f=3400MHz, Pin = 45dBm [1,2]
Drain Efficiency	45	52		%	f=3400MHz, Pin = 45dBm [1,2]
RF Typical Performance					
Frequency Range	2800		3400	MHz	
Small Signal Gain		11		dB	f=3200MHz, Pin = 30dBm [1,2]
Power Gain		10		dB	Pout = 54.7dBm [1,2]
Gain Variation with Temperature			-0.015	dB/°C	At peak output power [1,2]
Output Power (Psat)		54.7		dBm	Peak output power [1,2]
		300		W	Peak output power [1,2]
Drain Efficiency		48		%	At peak output power [1,2]

[1] Test Conditions: Pulsed Operation, PW=100usec, DC=10%, Vds=50V, Idq=440mA, T=25ºC
[2] Performance in a standard tuned test fixture

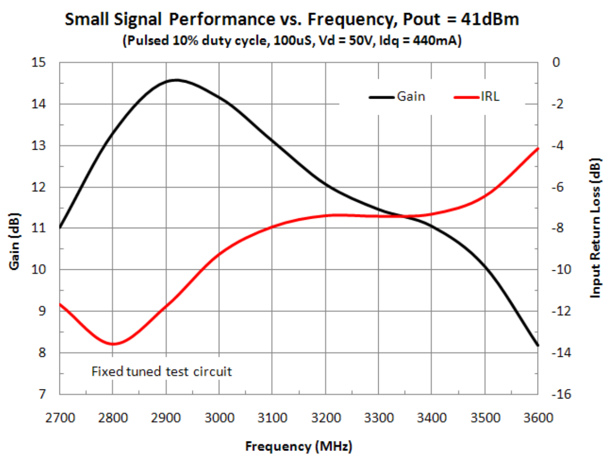
Typical Performance in standard fixed tuned test fixture over temperature (pulsed at center band frequency)

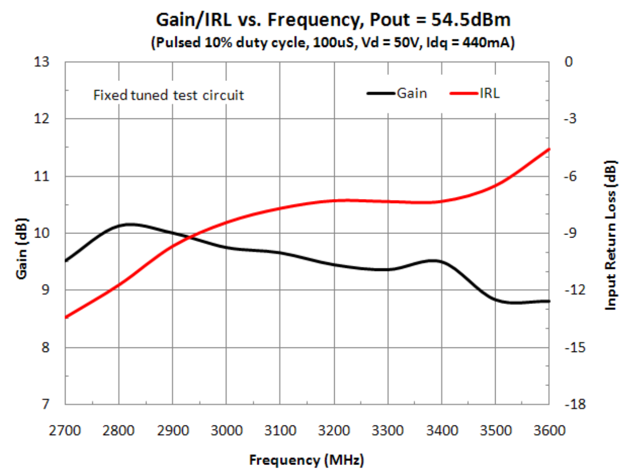


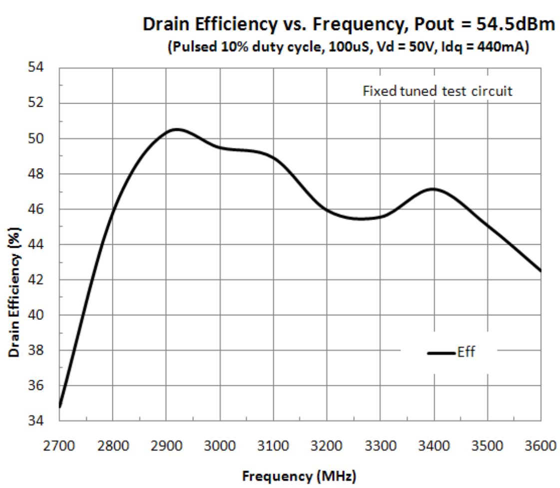


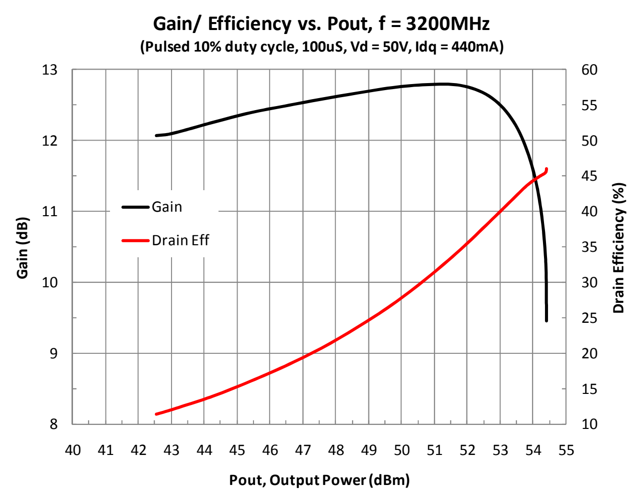


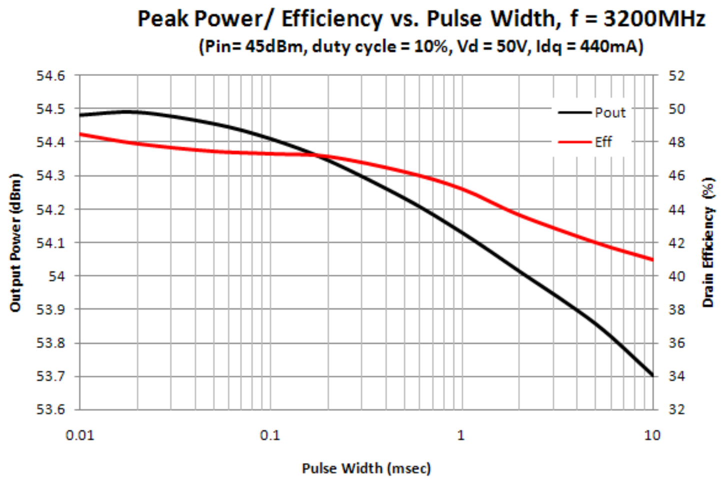
Typical Performance in standard fixed tuned test fixture (T=25°C, unless noted)

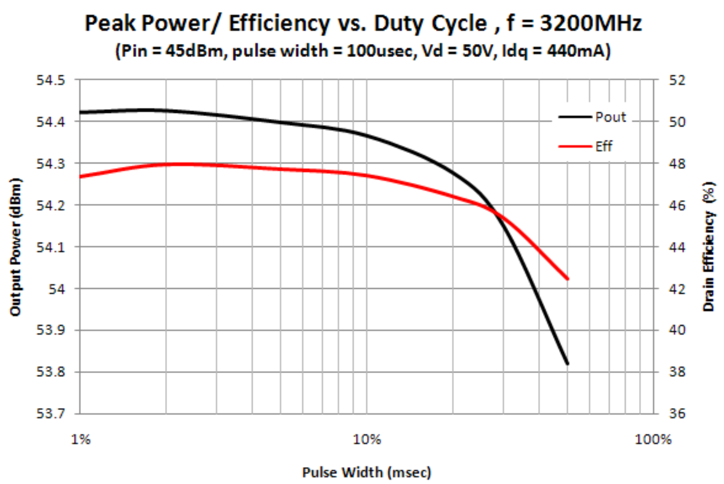






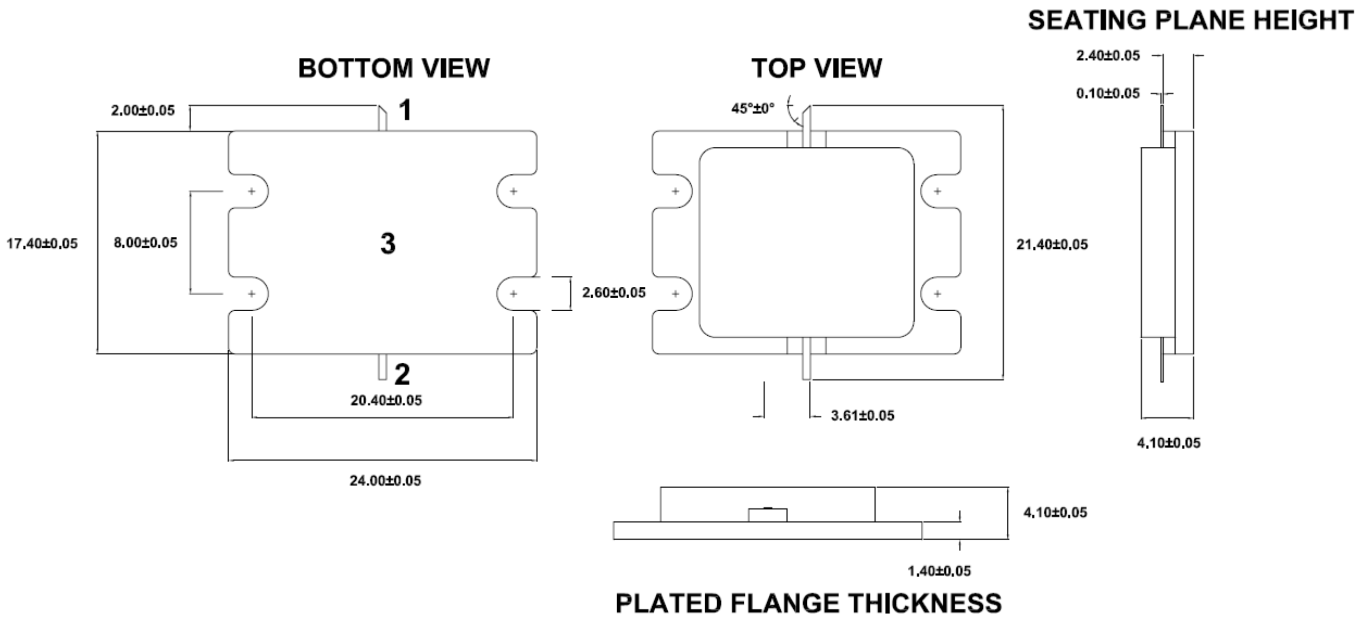



Peak Power/ Efficiency vs. Pulse Width, f = 3200MHz
(Pin= 45dBm, duty cycle = 10%, Vd = 50V, Idq = 440mA)
Output Power (dBm)
Drain Efficiency (%)
Pulse Width (msec)
Pout
Eff
54.6
54.5
54.4
54.3
54.2
54.1
54
53.9
53.8
53.7
53.6
52
50
48
46
44
42
40
38
36
34
32
0.01
0.1
1
10


Peak Power/ Efficiency vs. Duty Cycle , f = 3200MHz
(Pin = 45dBm, pulse width = 100usec, Vd = 50V, Idq = 440mA)
Output Power (dBm)
Drain Efficiency (%)
Pulse Width (msec)
Pout
Eff
54.5
54.4
54.3
54.2
54.1
54
53.9
53.8
53.7
52
50
48
46
44
42
40
38
36
1%
10%
100%

Package Drawing

(All dimensions in mm)



Pin	Function	Description
1	Gate	Gate – VG RF Input
2	Drain	Drain – VD RF Output
3	Source	Source – Ground Base

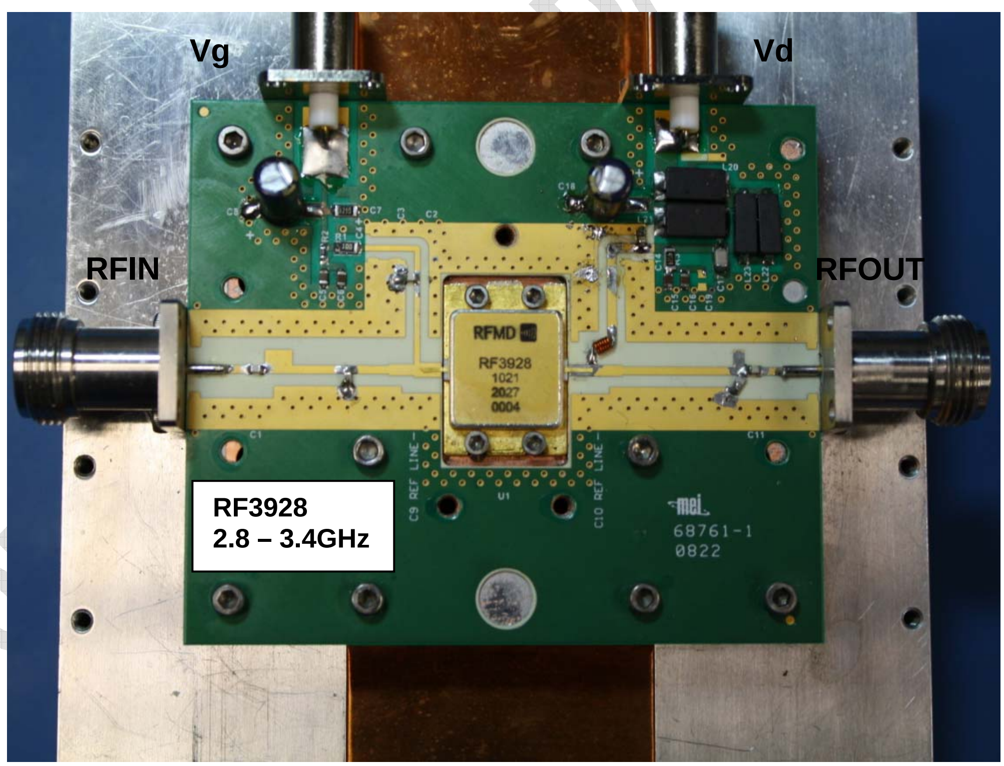
Bias Instruction for RF3928 Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.
Evaluation board requires additional external fan cooling.
Connect all supplies before powering evaluation board.

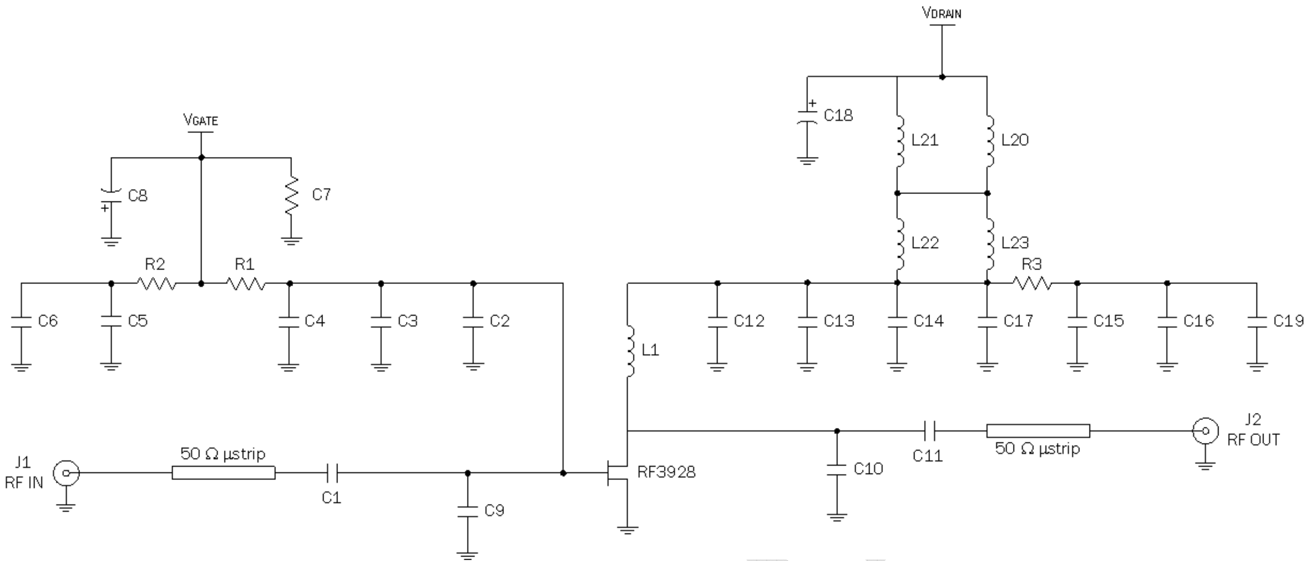
1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the V_G and V_D grounds are also connected to this ground terminal.
3. Apply -6V to Vg.
4. Apply 50V to Vd.
5. Increase Vg until drain current reaches 440mA or desired bias point.
6. Turn on the RF input.

IMPORTANT NOTE: Depletion mode device, when biasing the device VG be applied BEFORE V_D. When removing bias V_D must be removed BEFORE V_G is removed. Failure to follow sequencing will cause the device to fail.

Note: For optimal RF performance, consistent and optimal heat removal from the base of the package is required. A thin layer of thermal grease should be applied to the interface between the base of the package and the equipment chassis. It is recommended a small amount of thermal grease is applied to the underside of the device package. Even application and removal of excess thermal grease can be achieved by spreading the thermal grease using a razor blade. The package should then be bolted to the chassis and input and output leads soldered to the circuit board.



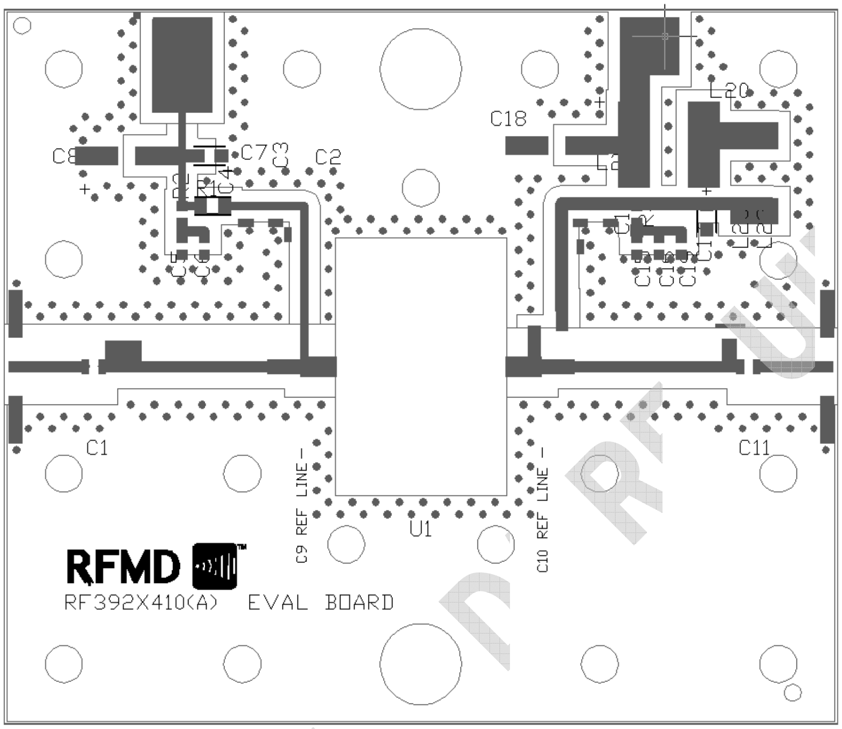
Evaluation Board Schematic



Evaluation Board Bill of Materials

Component	Value	Manufacturer	Part Number
R1	10 ohms	Panasonic	ERJ-8GEYJ100V
R2	0 ohms	Panasonic	ERJ-3GEY0R00
R3	51 ohms	Panasonic	ERJ-8GEYJ510
C1,C11	22pF	ATC	ATC100A220JT
C2, C14	12pF	ATC	ATC100A120JT
C5, C16	1000pF	Panasonic	ECJ-2VB1H102K
C6,C15	10000pF	Panasonic	ECJ-2VB1H103K
C7	120 ohms	Panasonic	ERJ-6GEYJ120V
C8,C18	10uF	Panasonic	ECA-2AM100
C9	0.7pF	ATC	ATC100A0R7BT
C10	0.2pF	ATC	ATC100A0R2BT
C17	62pF	ATC	ATC100B620JT
L1	22nH	Coilcraft	0807SQ-22N_LC
L20,L21	115 ohm, 10A	Steward	28F0181-1SR-10
L22,L23	75 ohm, 10A	Steward	35F0121-1SR-10
C3,C4,C7,C12,C13,C19	NOT POPULATED		

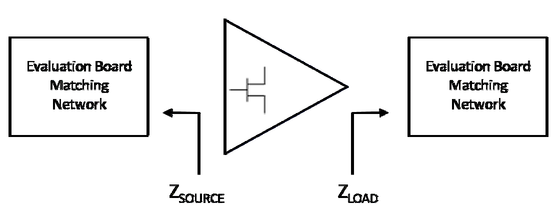
Evaluation Board Layout



Device Impedances

Frequency	Z Source (Ω)	Z Load (Ω)
2800MHz	60.4 – j0.5	42.1 – j 30.5
3000MHz	51.9 – j13.5	33.8 – j 25.7
3200MHz	44.1 – j16.5	29.5 – j 8.9
3400MHz	38.3 – j16.7	17.0 – j9.0

* Device impedances reported are the measured evaluation board impedances chosen for a tradeoff of peak power, peak efficiency and gain performance across the entire frequency bandwidth.



REV	DESCRIPTION OF CHANGE	MODIFIED By	DATE
1	Initial release	MP	3/17/2008
2	Updated package photo and part description	MP	6/7/2010
3	Added new format graphs, source and load impedances Updated evaluation board BOM	MP	6/15/2010
4	Added max gate current limit Updated Rth based on RF pulse measurements Added Output power and drain efficiency graphs detailing the effects of pulse width and duty cycle Updated source and load impedances Updated evaluation board BOM Test limits updated based on completion of validation data	MP	8/27/2010
5	Updated Rth for pulse/DC, Max Vd, Min Eff, Min Pout, package picture size (front page)	DR	9/28/2010.