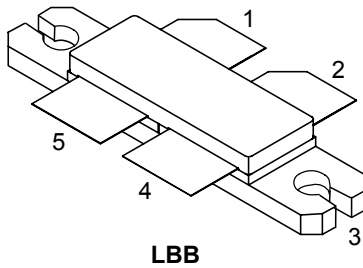


400 W, 28/32 V, HF to 1 GHz RF power LDMOS transistor



| Pin connection | |
|----------------|----------------------|
| Pin | Connection |
| 1 | Drain A |
| 2 | Drain B |
| 3 | Source (bottom side) |
| 4 | Gate B |
| 5 | Gate A |



| Product status link | |
|------------------------------|--|
| RF3L05400CB4 | |

| Product summary | |
|--------------------|-------------------|
| Order code | RF3L05400CB4 |
| Marking | 3L05400 |
| Package | LBB |
| Packing | Tape and reel 13" |
| Base/bulk quantity | 100/100 |

Features

| Order code | Frequency | V _{DD} | P _{OUT} | Gain | Efficiency |
|--------------|-----------|-----------------|------------------|-------|------------|
| RF3L05400CB4 | 108 MHz | 28 V | 400 W | 15 dB | 75% |

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- In compliance with the European directive 2002/95/EC

Applications

- 2-30 MHz HF or short wave communication
- 30-88 MHz ground communication
- 118-140 MHz avionics
- 136-174 MHz commercial ground communication
- 30-512 MHz jammer, ground/air communication
- HF to 1 GHz ISM - instrumentation

Description

The **RF3L05400CB4** is a 400 W, 28/32 V, LDMOS FET designed for wideband communication and ISM applications in the frequency range from HF to 1 GHz. It can be used in class AB, B or C for all typical modulation formats.

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

| Symbol | Parameter | Value | Unit |
|-----------|------------------------------|------------|------|
| V_{DS} | Drain-source voltage | 90 | V |
| V_{GS} | Gate-source voltage | -8 to 10 | V |
| V_{DD} | Maximum operating voltage | 36 | V |
| T_{STG} | Storage temperature range | -65 to 150 | °C |
| T_J | Maximum junction temperature | 200 | °C |

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|------------------|--------------------------------------|-------|------|
| $R_{thJC}^{(1)}$ | Thermal resistance, junction-to-case | 0.3 | °C/W |

1. $T_C = 85\text{ °C}$, $T_J = 200\text{ °C}$, DC test.

Table 3. ESD protection

| Symbol | Test methodology | Class |
|--------|---|-------|
| HBM | Human body model (according to ANSI/ESDA/JEDEC JS001-2017) | 2 |
| CDM | Charge device model (according to ANSI/ESDA/JEDEC JS002-2014) | C3 |

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 4. Static (per side)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|---|---|------|------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 100\text{ }\mu\text{A}$ | 90 | | | V |
| I_{DSS} | Zero gate voltage drain leakage current | $V_{GS} = 0\text{ V}$, $V_{DS} = 28\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 75\text{ V}$ | | | 1 | |
| I_{GSS} | Gate-source leakage current | $V_{GS} = -8/10\text{ V}$, $V_{DS} = 0\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = 28\text{ V}$, $I_D = 600\text{ }\mu\text{A}$ | 1.75 | | 2.50 | V |
| $V_{GS(Q)}$ | Gate quiescent voltage | $V_{DS} = 1\text{ V}$, $I_D = 1\text{ A}$ | 2 | | 4 | V |
| $V_{DS(on)}$ | Static drain-source on-voltage | $V_{GS} = 10\text{ V}$, $I_{DS} = 5\text{ A}$ | | | 800 | mV |
| $I_{DS(on)}$ | Static drain-source on-current | $V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$ | | | 2.5 | A |
| $R_{DS(on)}$ | Drain-source on-state resistance | $V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$ | | | 1 | Ω |
| C_{ISS} | Common source input capacitance | $V_{GS} = 0\text{ V}$, $V_{DD} = 28\text{ V}$, $f = 1\text{ MHz}$ | | 187 | | pF |
| C_{RSS} | Common source feedback capacitance | | | 4.6 | | pF |
| C_{OSS} | Common source output capacitance | | | 79 | | pF |

Table 5. Dynamic

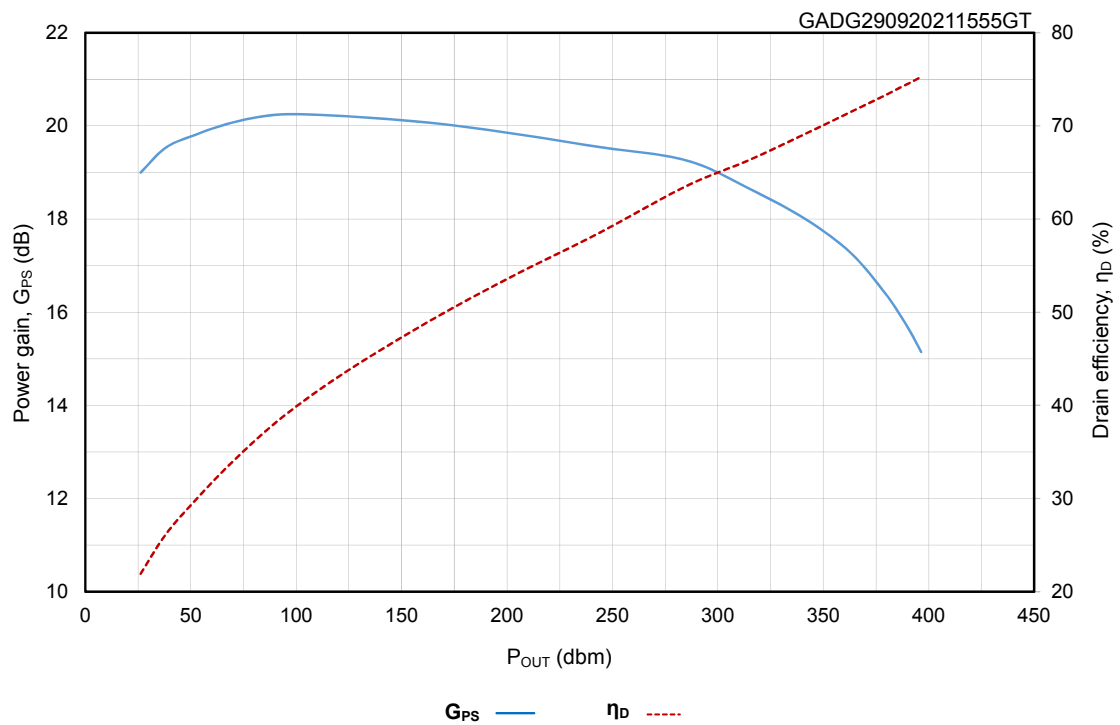
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------|--|------|------|------|------|
| f | Frequency | | | | 1000 | MHz |
| P_{OUT} | Output power | f = 108 MHz, 5 dB compression | | 400 | | W |
| G_{PS} | Power gain | | | 15 | | dB |
| η_D | Drain efficiency | | | 75 | | % |
| VSWR | Load mismatch | $P_{OUT} = 400\text{ W}$, pulsed CW, all phases | | | 10:1 | |

Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$, pulsed CW, pulse width = 100 μs , duty cycle = 10%.

3 Typical performances

Table 6. Output power, power gain and drain efficiency versus input power (f = 108 MHz)

| P_{IN} (dBm) | P_{OUT} (dBm) | P_{OUT} (W) | I_{DS} (A) | G_{PS} (dB) | η_D (%) |
|----------------|-----------------|---------------|--------------|---------------|--------------|
| 29.3 | 49.5 | 90 | 8.4 | 20.2 | 38 |
| 30.3 | 50.5 | 113 | 9.6 | 20.2 | 42 |
| 31.3 | 51.45 | 139.5 | 10.9 | 20.15 | 45.8 |
| 32.3 | 52.35 | 170.7 | 12.2 | 20.03 | 50 |
| 33.3 | 53.1 | 205 | 13.5 | 19.8 | 54.15 |
| 34.3 | 53.8 | 243 | 14.8 | 19.5 | 58.4 |
| 35.3 | 54.6 | 284.7 | 16 | 19.3 | 63.5 |
| 36.3 | 54.6 | 314.5 | 17 | 18.7 | 66.3 |
| 37.3 | 55.3 | 342 | 17.6 | 18 | 69.2 |
| 38.3 | 55.55 | 363.4 | 18.1 | 17.25 | 71.5 |
| 39.3 | 55.7 | 379.1 | 18.5 | 16.4 | 73.25 |
| 39.9 | 55.85 | 385.9 | 18.6 | 15.95 | 74 |
| 40.3 | 55.92 | 391.3 | 18.7 | 15.62 | 74.65 |
| 40.8 | 55.98 | 396.4 | 18.8 | 15.18 | 75.2 |

Figure 1. Power gain and efficiency versus output power (108 MHz)


Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$, pulsed CW, pulse width = 100 μs , duty cycle = 10%

4 Test circuits

Figure 2. Test circuit layout (f = 108 MHz)

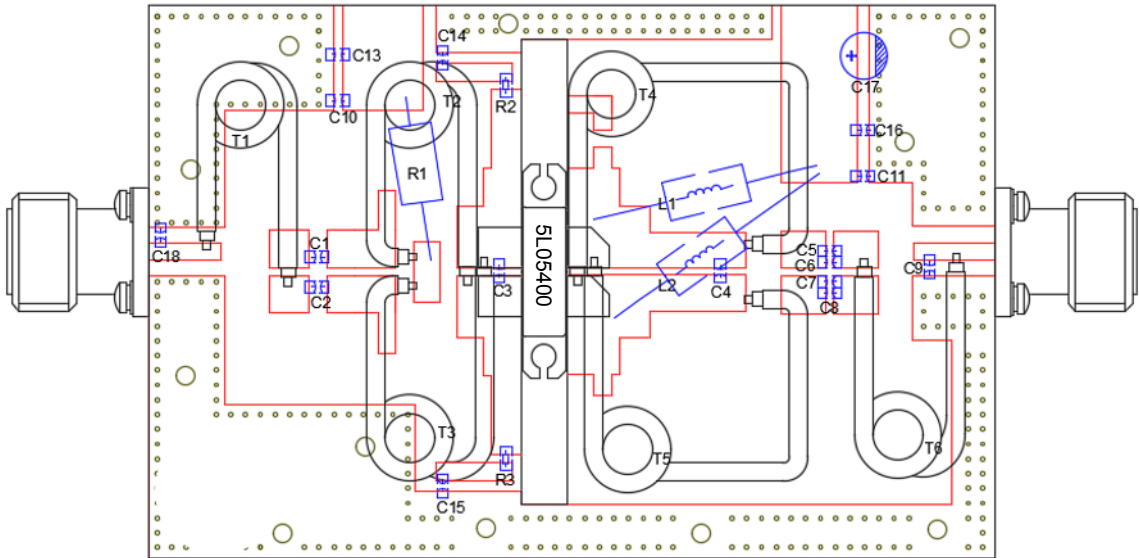


Figure 3. Test circuit photo

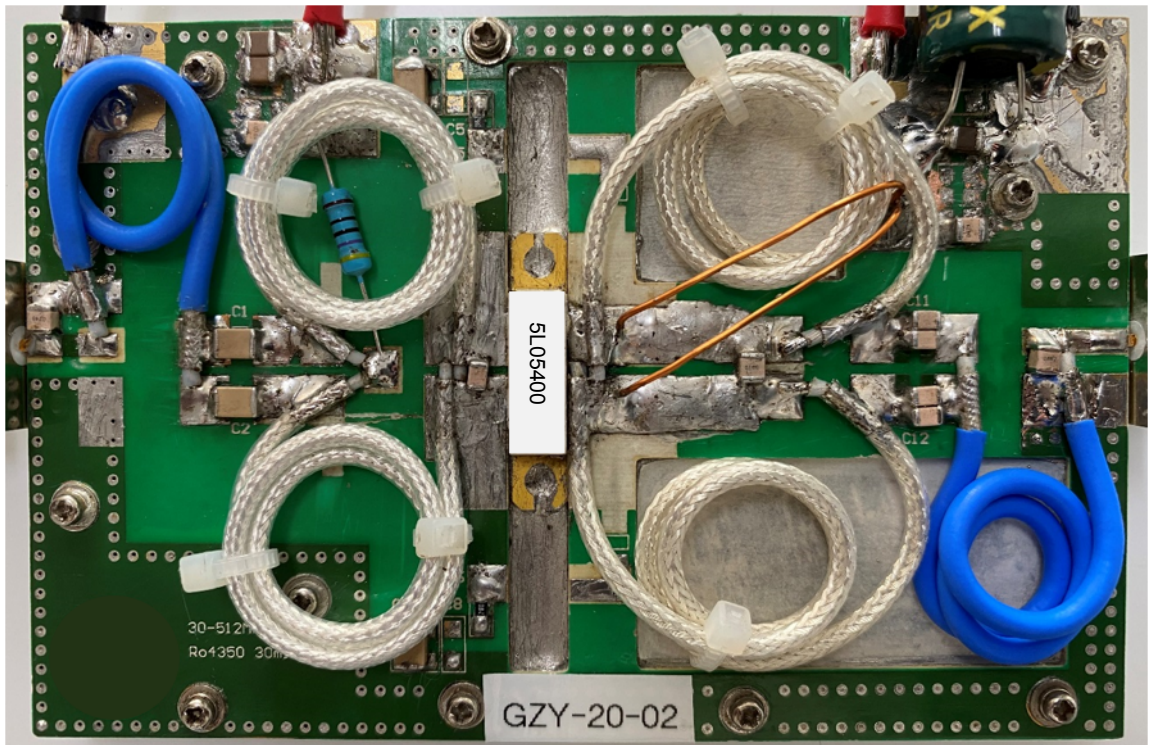


Table 7. Components list

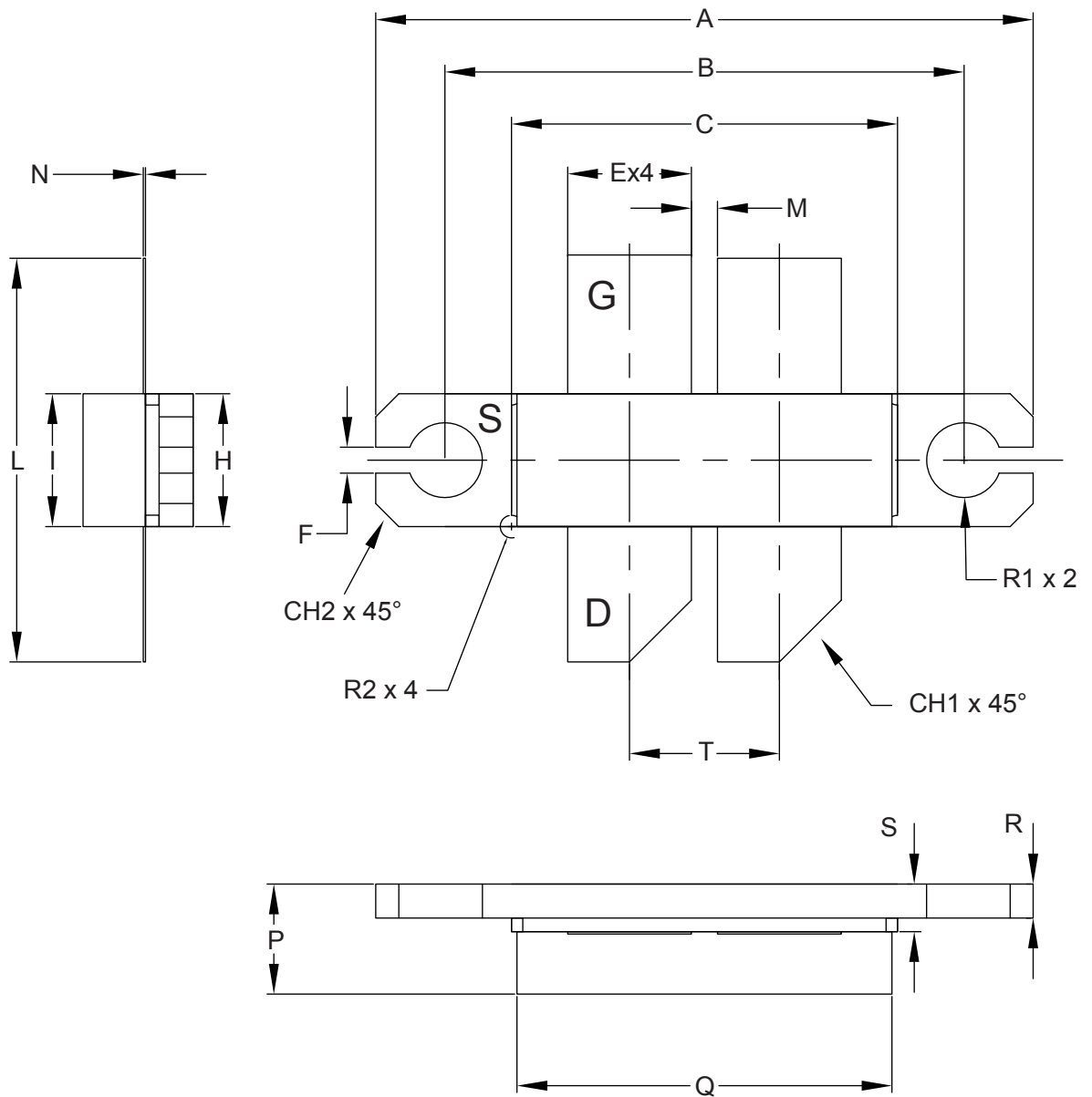
| Component | Value | Reference |
|--------------------------|---|-------------------------------------|
| C5, C6, C7, C8, C10, C11 | 470 pF | ATC800B |
| C3, C18 | 24 pF | ATC800B |
| C4 | 18 pF | ATC800B |
| C9 | 8.2 pF | ATC800B |
| C1, C2, C14, C15 | 10 nF | 100 V ceramic multilayer capacitor, |
| C13, C16 | 10 μ F | 100 V ceramic multilayer capacitor |
| T1 | 50 Ω , ϕ 2.0, line length = 15 cm | Coaxial cable |
| T2, T3 | 25 Ω , ϕ 2.0, line length = 15 cm | Coaxial cable |
| T3, T4 | 12.5 Ω , ϕ 2.0, line length = 20 cm | Coaxial cable |
| T6 | 50 Ω , ϕ 2.0, line length = 18 cm | Coaxial cable |
| R1 | 470 Ω | Metal film resistor |
| R3, R4 | 24 Ω | 0805 chip resistor |
| L1, L2 | Φ 0.8 mm | Copper wire |
| C17 | 470 μ F, 63 V | 63 V electrolytic capacitor |
| PCB | 0.762 mm [0.030"] thick, $\epsilon_r = 3.48$, Rogers RO4350B, 1 oz. copper | |

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LBB package information

Figure 4. LBB package outline



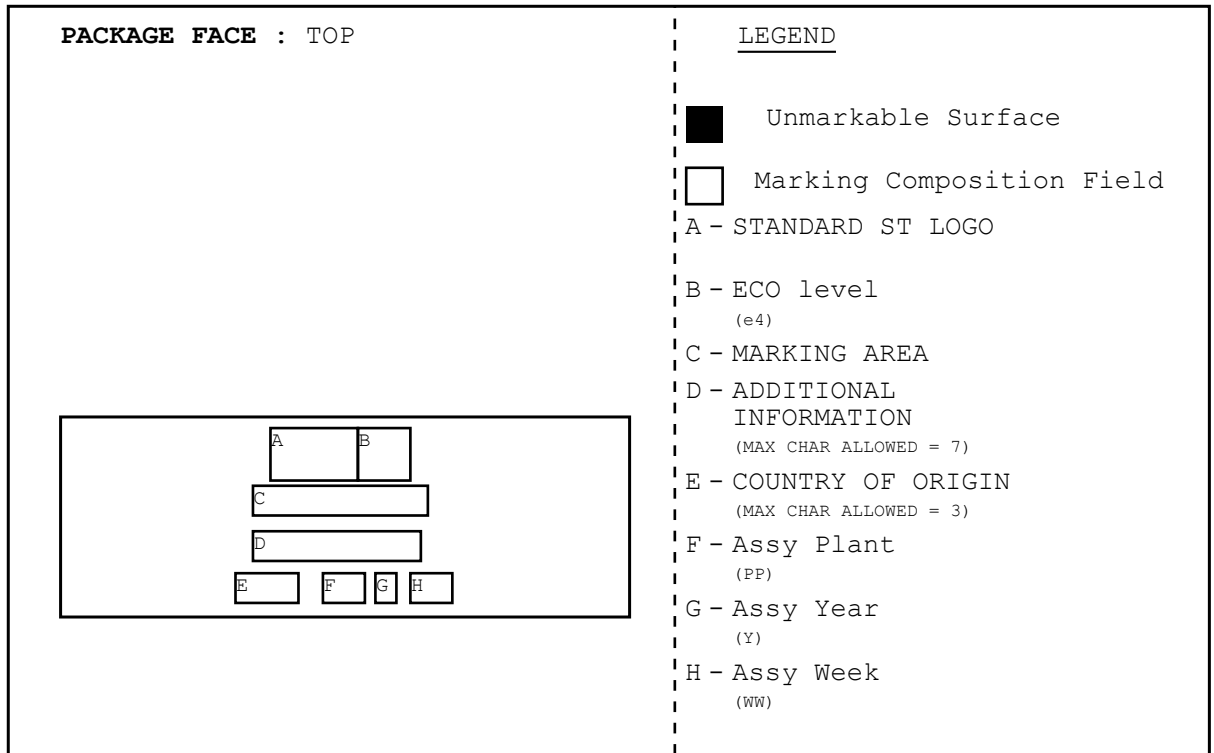
DM00666717_2

Table 8. LBB mechanical data

| Symbol | Millimeters | | |
|--------|-------------|-------|-------|
| | Min. | Typ. | Max. |
| A | 28.82 | 28.95 | 29.08 |
| B | 22.73 | 22.86 | 22.99 |
| C | 16.87 | 17.00 | 17.13 |
| E | 5.32 | 5.45 | 5.58 |
| F | 1.01 | 1.14 | 1.27 |
| H | 5.72 | 5.85 | 5.98 |
| I | 5.72 | 5.85 | 5.98 |
| L | 17.65 | 17.78 | 17.91 |
| M | 1.02 | 1.15 | 1.28 |
| N | | 0.10 | |
| P | 4.72 | 4.85 | 4.98 |
| Q | 16.38 | 16.51 | 16.64 |
| R | 1.37 | 1.50 | 1.63 |
| S | 1.97 | 2.10 | 2.23 |
| T | | 6.60 | |
| CH1 | | 2.72 | |
| CH2 | | 1.02 | |
| R1 | | 1.65 | |
| R2 | | 0.50 | |

5.2 Marking information

Figure 5. Marking composition



GADG040220211644GT

Revision history

Table 9. Document revision history

| Date | Version | Changes |
|-------------|---------|--|
| 08-Jun-2020 | 1 | First release |
| 01-Oct-2021 | 2 | Updated title and Device summary on cover page. Updated Section 1 Electrical ratings. Updated Table 4. Static (per side). Updated Figure 1. Power gain and efficiency versus output power (108 MHz). Updated Section 4 Test circuits. Added Section 5.2 Marking information. Minor text changes. |

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