



# RF5144

DUAL-BAND CDMA 800MHz/1900MHz  
TRI-MODE POWER AMPLIFIER MODULE

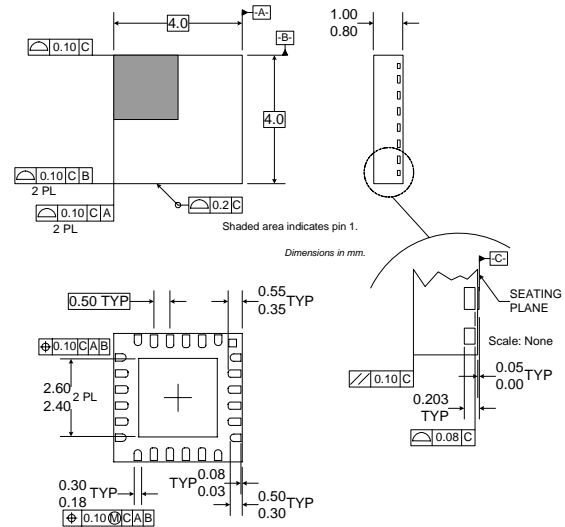
**RoHS Compliant & Pb-Free Product**

### Typical Applications

- 3V CDMA/AMPS Cellular Handset
- 3V CDMA2000/1XRTT Cellular Handset
- 3V CDMA US-PCS Handset
- 3V CDMA2000/1XRTT US-PCS Handset

### Product Description

The RF5144 is a high-power, high-efficiency linear amplifier module specifically designed for 3V handheld systems. The device is manufactured on an advanced third generation GaAs HBT process, and was designed for use as the final RF amplifier in 3V IS-95/CDMA2000 1X/AMPS handheld digital cellular equipment, spread-spectrum systems, and other applications in the 824MHz to 849MHz band and 1850MHz to 1910MHz band. The RF5144 has a digital control line for low power applications to lower quiescent current. The RF5144 is assembled in a 24-pin, 4mmx4mm, QFN package.



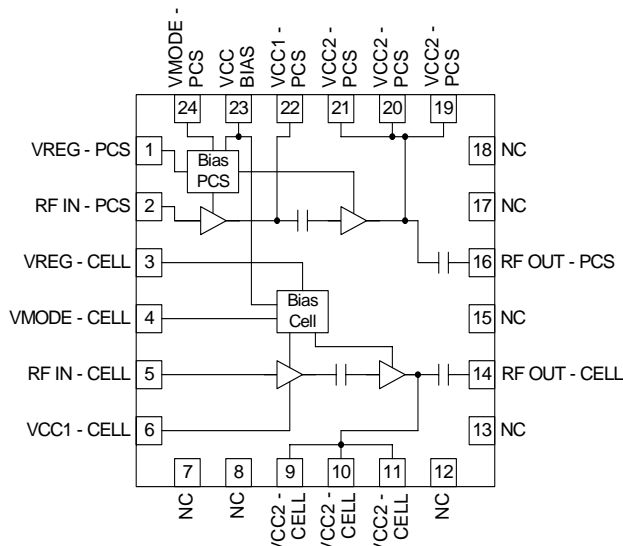
### Optimum Technology Matching® Applied

- |                                     |  |                                       |
|-------------------------------------|--|---------------------------------------|
| <input type="checkbox"/> Si BJT     | <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> GaAs MESFET  |
| <input type="checkbox"/> Si Bi-CMOS | <input type="checkbox"/> SiGe HBT            | <input type="checkbox"/> Si CMOS      |
| <input type="checkbox"/> InGaP/HBT  | <input type="checkbox"/> GaN HEMT            | <input type="checkbox"/> SiGe Bi-CMOS |

Package Style: QFN, 24-Pin, 4 x 4

### Features

- Input/Output Internally Matched @ 50Ω
- 28dBm Output Power
- 41% Peak Linear Efficiency for Cell Band
- -51 dBc ACPR @ 885kHz for Cell Band
- -50dBc ACPR @ 1.25MHz for PCS Band
- 40% Peak Linear Efficiency for PCS Band



Functional Block Diagram

### Ordering Information

RF5144 Dual-Band CDMA 800MHz/1900MHz Tri-Mode Power Amplifier Module  
RF5144PCBA-410 Fully Assembled Evaluation Board

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# RF5144

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V
Supply Voltage ( $P_{OUT} \leq 31$ dBm)	+5.2	V
Control Voltage ( $V_{REG}$ )	+3.9	V
Input RF Power	+10	dBm
Mode Voltage ( $V_{MODE}$ )	+3.9	V
Operating Temperature	-30 to +110	°C
Storage Temperature	-40 to +150	°C



**Caution!** ESD sensitive device.

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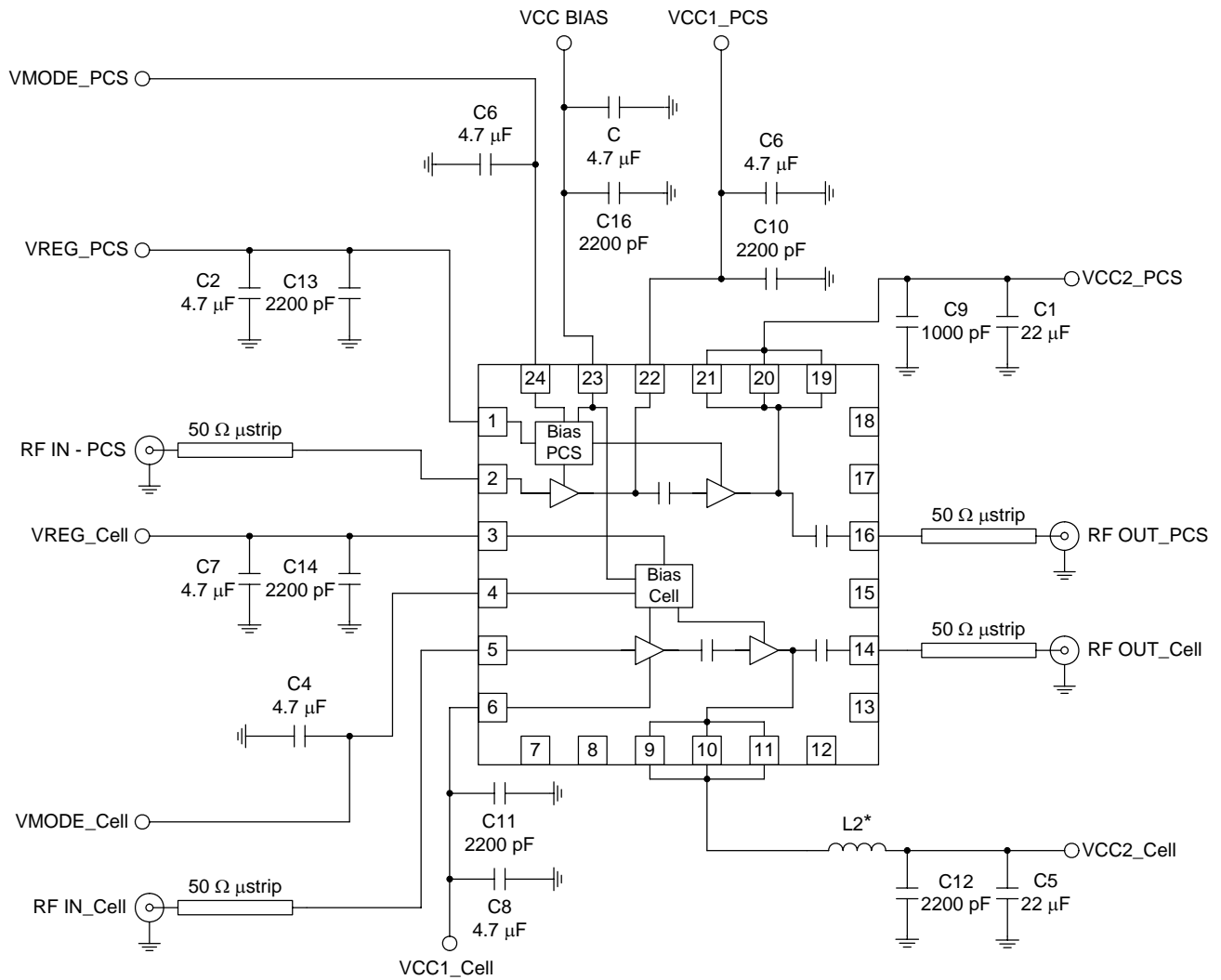
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>High Power Mode - CDMA Cell Band (<math>V_{MODE}</math> Low)</b>					$T=25^{\circ}\text{C}$ Ambient, $V_{CC}=3.4\text{V}$ , $V_{REG}=2.8\text{V}$ , $V_{MODE}=0\text{V}$ , and $P_{OUT}=28\text{dBm}$ for all parameters (unless otherwise specified).
Operating Frequency Range	824		849	MHz	
Linear Gain	26.5	28.5	30.5	dB	
Maximum Linear Output	28			dBm	
Linear Efficiency	37	41	44	%	
Maximum $I_{CC}$	421	455	501	mA	
ACPR @ 885kHz		-51	-46	dBc	
ACPR @ 1.98MHz		-58	-55	dBc	
Input VSWR		2:1			
Stability in Band			6:1		No oscillation > -70dBc
Stability out of Band			10:1		No damage
Noise Power		-133		dBm/Hz	At 45MHz offset.
<b>Low Power Mode - CDMA Cell Band (<math>V_{MODE}</math> High)</b>					$T=25^{\circ}\text{C}$ Ambient, $V_{CC}=3.4\text{V}$ , $V_{REG}=2.8\text{V}$ , $V_{MODE}=2.8\text{V}$ , and $P_{OUT}=16\text{dBm}$ for all parameters (unless otherwise specified).
Operating Frequency Range	824		849	MHz	
Linear Gain	25	27	30	dB	
Maximum Linear Output	16			dBm	
Linear Efficiency	8.1	9.0	9.8	%	
Maximum $I_{CC}$	120	130	145	mA	
ACPR @ 885kHz		-50	-46	dBc	
ACPR @ 1.98MHz		-65	-58	dBc	
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation > -70dBc
			10:1		No damage
<b>FM Mode - Cell Band</b>					$T=25^{\circ}\text{C}$ Ambient, $V_{CC}=3.4\text{V}$ , $V_{REG}=2.8\text{V}$ , $V_{MODE}=0\text{V}$ , and $P_{OUT}=30.5\text{dBm}$ for all parameters (unless otherwise specified).
Operating Frequency Range	824		849	MHz	
AMPS Maximum Output Power	30.5	31.0		dBm	
AMPS Efficiency	45	52	56	%	
AMPS Gain	26	28	30		
AMPS Second Harmonics		-50	-35	dBc	
AMPS Third Harmonics		-60	-35	dBc	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>High Gain Mode - CDMA PCS Band (<math>V_{MODE}</math> Low)</b>					
Operating Frequency Range	1850		1910	MHz	T=25°C Ambient, $V_{CC}$ =3.4V, $V_{REG}$ =2.8V, $V_{MODE}$ =0V, and $P_{OUT}$ =28dBm for all parameters (unless otherwise specified).  No oscillation > -70dBc No damage At 80MHz offset.
Linear Gain	26.0	28.0	30.5	dB	
Second Harmonics		-45	-35	dBc	
Third Harmonics		-60	-35	dBc	
Maximum Linear Output	28			dBm	
Linear Efficiency	37	40	45	%	
Maximum $I_{CC}$	412	465	501	mA	
ACPR @ 1.25MHz		-50	-46	dBc	
ACPR @ 1.98MHz		-54.0	-51.5	dBc	
Input VSWR		2:1			
Output VSWR Stability			6:1 10:1		
Noise Power		-137		dBm/Hz	
<b>Low Gain Mode - CDMA PCS Band (<math>V_{MODE}</math> High)</b>					
Operating Frequency Range	1850		1910	MHz	T=25°C Ambient, $V_{CC}$ =3.4V, $V_{REG}$ =2.8V, $V_{MODE}$ =2.8V, and $P_{OUT}$ =16dBm for all parameters (unless otherwise specified).  No oscillation > -70dBc No damage
Linear Gain	25.0	27.0	29.5	dB	
Maximum Linear Output	16			dBm	
ACPR @ 1.25MHz		-55	-48	dBc	
ACPR @ 1.98MHz		-63	-56	dBc	
Linear Efficiency	7.8	9.0	10.6	%	
Maximum $I_{CC}$	110	130	150	mA	
Input VSWR		2:1			
Output VSWR Stability			6:1 10:1		
<b>Power Supply</b>					
Supply Voltage	3.2	3.4	4.2	V	$V_{REG\_CELL}$ =2.8V $V_{REG\_PCS}$ =2.8V $V_{REG\_PCS}$ =2.8V
High Gain Idle Current - Cell	45	60	75	mA	
Low Gain Idle Current - Cell	34	45	64	mA	
$V_{REG}$ Current - Cell	1.5	2.5	3.0	mA	
High Gain Idle Current - PCS	45	75	95	mA	
Low Gain Idle Current - PCS	40	65	85	mA	
$V_{REG}$ Current - PCS	1.5	2.0	3.0	mA	
$V_{MODE}$ Current - Cell		200	250	uA	
$V_{MODE}$ Current - PCS		150	250	uA	
RF Turn On/Off Time		1.2	6	uS	
DC Turn On/Off Time		2	40	uS	
Total Current (Power Down)		0.2	2.0	uA	
$V_{REG}$ Low Voltage (Power Down)	0		0.5	V	
$V_{REG}$ High Voltage (Recommended)	2.75	2.8	2.95	V	
$V_{REG}$ High Voltage (Operational)	2.7		3.0	V	
$V_{MODE}$ Voltage	0		0.5	V	
$V_{MODE}$ Voltage	2.0		3.0	V	

# RF5144

Pin	Function	Description	Interface Schematic
1	VREG_PCS	Regulated voltage supply for PCS band amplifier bias circuit. In power down mode, both $V_{REG\_PCS}$ and $V_{MODE\_PCS}$ need to be LOW (<0.5V).	
2	RFIN_PCS	PCS band RF input internally matched to 50Ω. This input is internally AC-coupled.	
3	VREG_Cell	Regulated voltage supply for Cell band amplifier bias circuit. In power down mode, both $V_{REG\_Cell}$ and $V_{MODE\_Cell}$ need to be LOW (<0.5V).	
4	VMODE_Cell	Cell band mode control pin. For nominal operation (High Power mode), $V_{MODE\_Cell}$ is set LOW. When set HIGH, devices are biased lower to improve efficiency.	
5	RFIN_Cell	Cell band RF input internally matched to 50Ω. This input is internally AC-coupled.	
6	VCC1_Cell	Cell band first stage collector supply. A 2200uF and a 4.7μF decoupling capacitors are required.	
7	NC	No connection. Do not connect this pin to any external circuit.	
8	NC	No connection. Do not connect this pin to any external circuit.	
9	VCC2_Cell	Cell band output stage collector supply. Please see the schematic for required external components.	
10	VCC2_Cell	Same as Pin 9.	
11	VCC2_Cell	Same as Pin 9.	
12	NC	No connection. Do not connect this pin to any external circuit.	
13	NC	No connection. Do not connect this pin to any external circuit.	
14	RFOUT_Cell	Cell band RF output. Internally AC-coupled.	
15	NC	No connection. Do not connect this pin to any external circuit.	
16	RFOUT_PCS	PCS band RF output. Internally AC-coupled.	
17	NC	No connection. Do not connect this pin to any external circuit.	
18	NC	No connection. Do not connect this pin to any external circuit.	
19	VCC2_PCS	PCS band output stage collector supply. Please see the schematic for required external components.	
20	VCC2_PCS	Same as Pin 19.	
21	VCC2_PCS	Same as Pin 19.	
22	VCC1_PCS	PCS band first stage collector supply. A 4.7μF decoupling capacitor is required.	
23	VCC BIAS	Bias circuit supply voltage.	
24	VMODE_PCS	PCS band mode control pin. For nominal operation (High Power mode), $V_{MODE\_PCS}$ is set Low. When set HIGH, devices are biased lower to improve efficiency.	
Pkg Base	GND	The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

## Evaluation Board Schematic - CDMA



\*The current rating for component L2 needs to be 1A. On the evaluation board, the parasitic inductance of a 0603 0 Ω resistor (Panasonic part #ERJ-3GEY0R00) is used to realize the required inductance. An inductor with value between 1 nH and 1.5 nH can also be used for L2. Different inductance will give slight tradeoff between ACPR and efficiency. The 0 Ω resistor is chosen on the evaluation board for the reason of low BOM cost.

## PCB Design Requirements

### PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

### PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

### PCB Metal Land Pattern

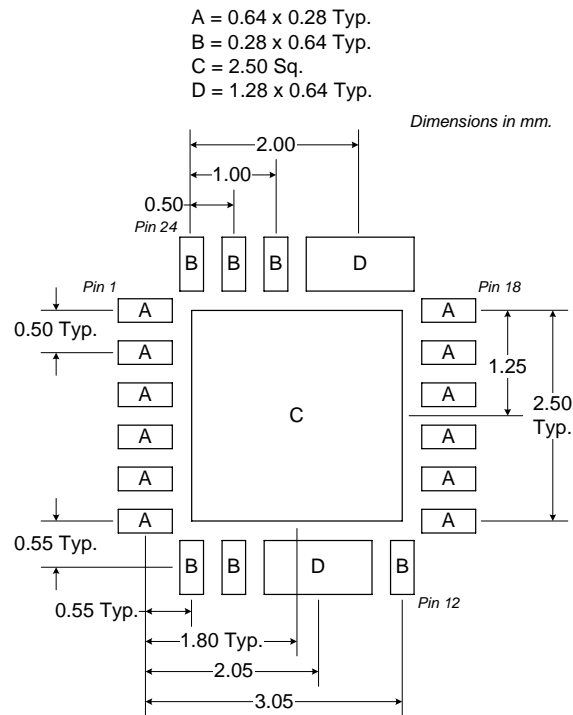
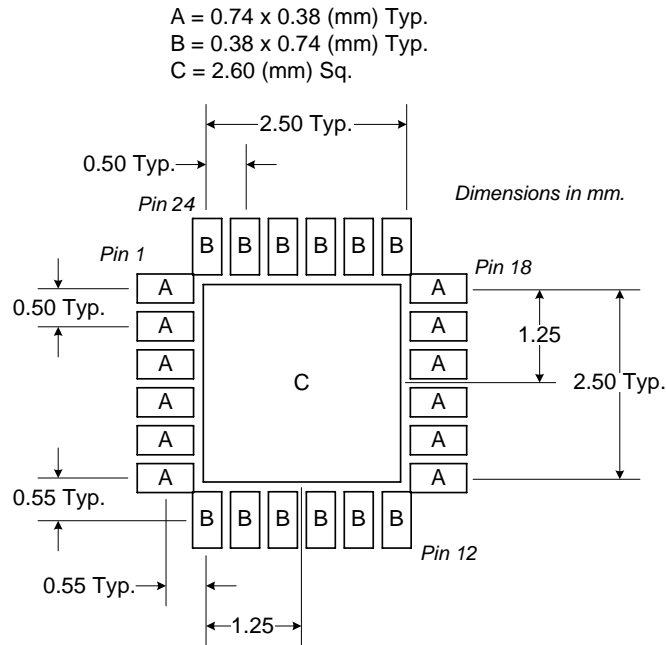


Figure 1. PCB Metal Land Pattern (Top View)

## PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.



**Figure 2. PCB Solder Mask (Top View)**

**RF5144**