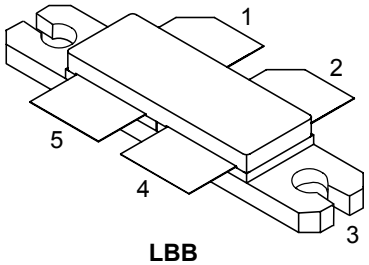
RF5L05500CB4

Datasheet

500 W, 50 V, HF to 500 MHz RF power LDMOS transistor



LBB

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF5L05500CB4	108 MHz	50 V	500 W	19 dB	70%

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- In compliance with the European directive 2002/95/EC

Applications

- 30-88 MHz/136-174 MHz ground communication
- Plasma generator
- Particle accelerator
- FM and VHF TV broadcast

Description

The RF5L05500CB4 is a 500 W, 50 V, high performance LDMOS FET designed for multiple applications in the frequency range from HF to 500 MHz.

Product status link
RF5L05500CB4

Product summary	
Order code	RF5L05500CB4
Marking	5L05500
Package	LBB
Packing	Tape and reel 13"
Base/bulk quantity	100/100

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	95	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	55	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}(1)	Thermal resistance, junction-to-case	0.2	°C/W

1. *T_C = 85 °C , T_J = 200 °C, DC test.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 100 µA	95	-		V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 50 V		-	1	µA
		V_{GS} = 0 V, V_{DS} = 75 V		-	1	
I_{GSS}	Gate-source leakage current	V_{GS} = -8/10 V, V_{DS} = 0 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 50 V, I_D = 600 µA	2.1	-	3.2	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 50 V, I_D = 100 mA	2.3	-	4.3	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_D = 2 A		-	600	mV
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV		-	2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, V_{DS} = 100 mV		-	1	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency				1000	MHz
P_{OUT}	Output power	f = 108 MHz, 2 dB compression, pulsed CW		500		W
G_{PS}	Power gain			19		dB
η_D	Drain efficiency			70		%
VSWR	Load mismatch	P_{OUT} = 500 W, pulsed CW, all phases			10:1	

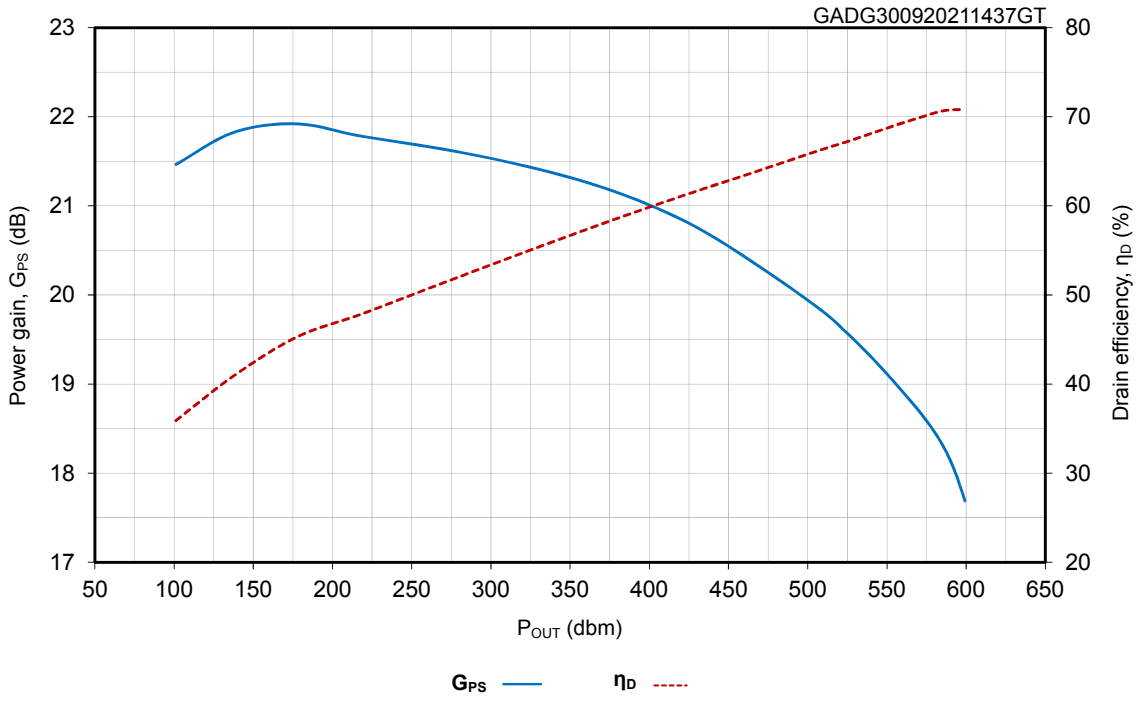
Note: V_{DD} = 50 V, I_{DQ} = 100 mA, pulse width = 100 µs, duty cycle = 10%.

3 Typical performances

Table 6. Output power, power gain and drain efficiency vs input power (f=108 MHz)

P_{IN} (dBm)	P_{OUT} (dBm)	P_{OUT} (W)	I_{DS} (A)	G_{PS} (dB)	η_D (%)
28.6	50.2	103.5	5.7	21.6	36.3
29.6	51.5	140.7	6.8	21.9	41.1
30.6	52.6	180.7	8.0	22.0	45.4
31.6	53.4	220.4	9.2	21.8	47.9
32.6	54.3	267.9	10.5	21.7	51.1
33.6	55.0	319.6	11.7	21.5	54.5
34.5	55.7	374.9	12.9	21.2	58.1
35.4	56.3	425.1	13.9	20.8	61.3
36.3	56.7	465.4	14.6	2.4	63.6
37.2	57.0	505.3	15.3	19.8	66.0
37.7	57.2	524.2	15.6	19.5	67.1
38.1	57.3	540.4	15.9	19.2	68.1
38.5	57.4	555.3	16.1	18.9	69.0

Figure 1. Power gain and drain efficiency versus output power (f = 108 MHz)



Note: V_{DD}= 50 V, I_{DQ}= 100 mA, pulsed CW, pulse width=100 µs, duty cycle=10%.

4 Test circuits

Figure 2. **Test circuit layout (f = 108 MHz)**

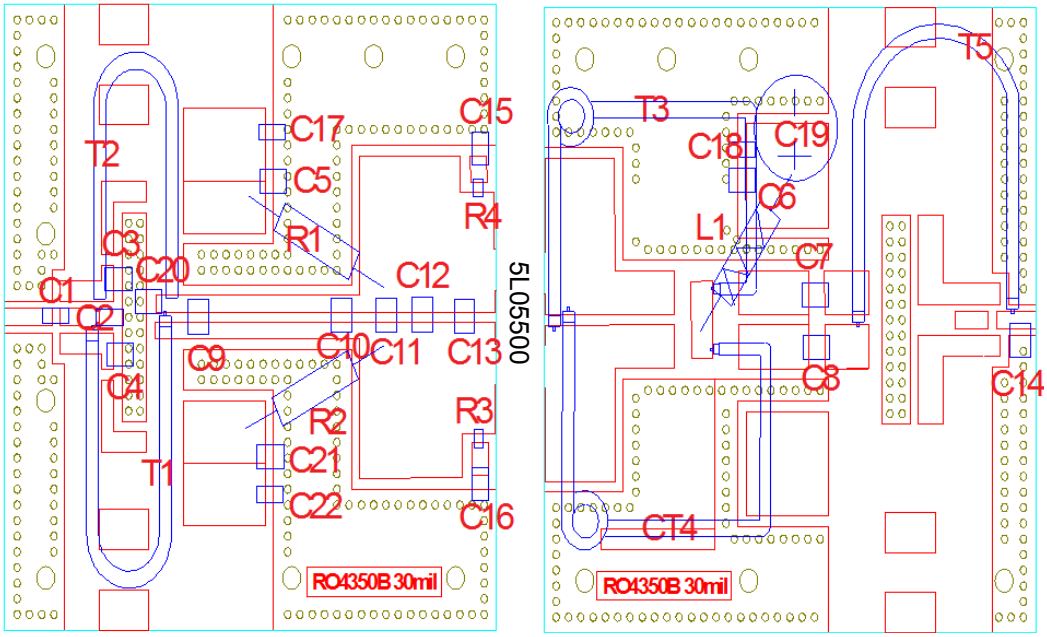


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Figure 3. **Test circuit photo**

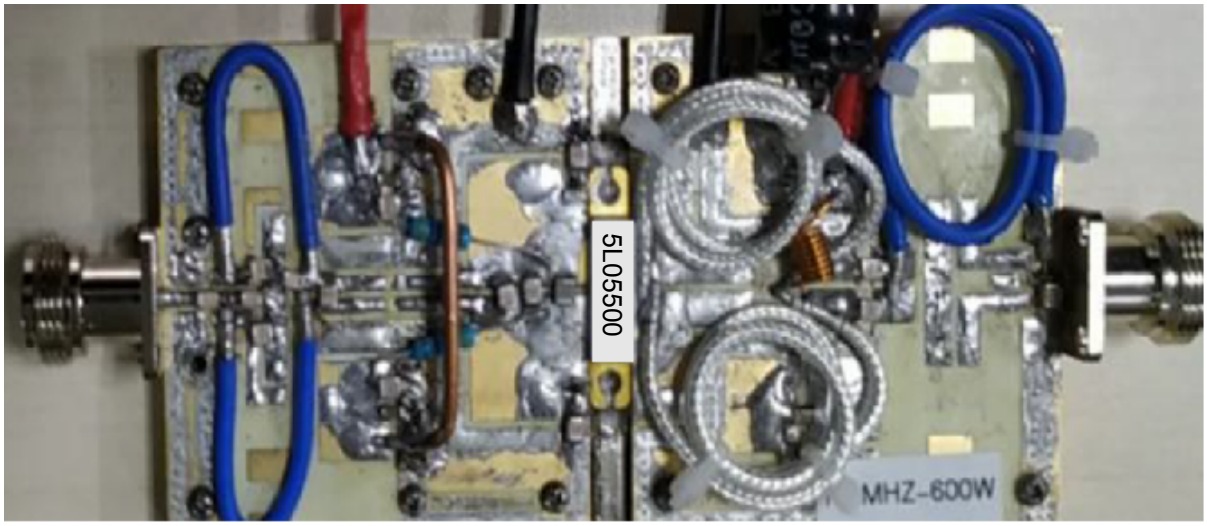

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Table 7. Components list

Component	Value	Reference
C1, C2, C13, C20	100 pF	DLC70B
C3, C4, C5, C6, C7,C8, C15, C16, C21	1000 pF	DLC70B
C9, C10, C11, C12	56 pF	DLC70B
C14	20 pF	DLC70B
C17, C18, C22	10 µF	100 V/10UF
C19	1000 µF	63V/1000UF
C19	5.6 pF	DLC70B
R1, R2	470 Ω	
R3, R4	15 Ω	0805 chip resistor
L1	ϕ 0.5,8	Circle enameled wire
T1	50 Ω, 60 mm	SF-086-1.5
T2	25 Ω, 6,0 mm	SFF-25-1.5
T3, T4	25 Ω, 200 mm	SFF-25-1.5
T5	50 Ω, 160 mm	SF-086-1.5
PCB	0.762 mm (0.030") thick, εr = 3.48, Rogers RO4350B, 1 oz. copper	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LBB package information

Figure 4. LBB package outline

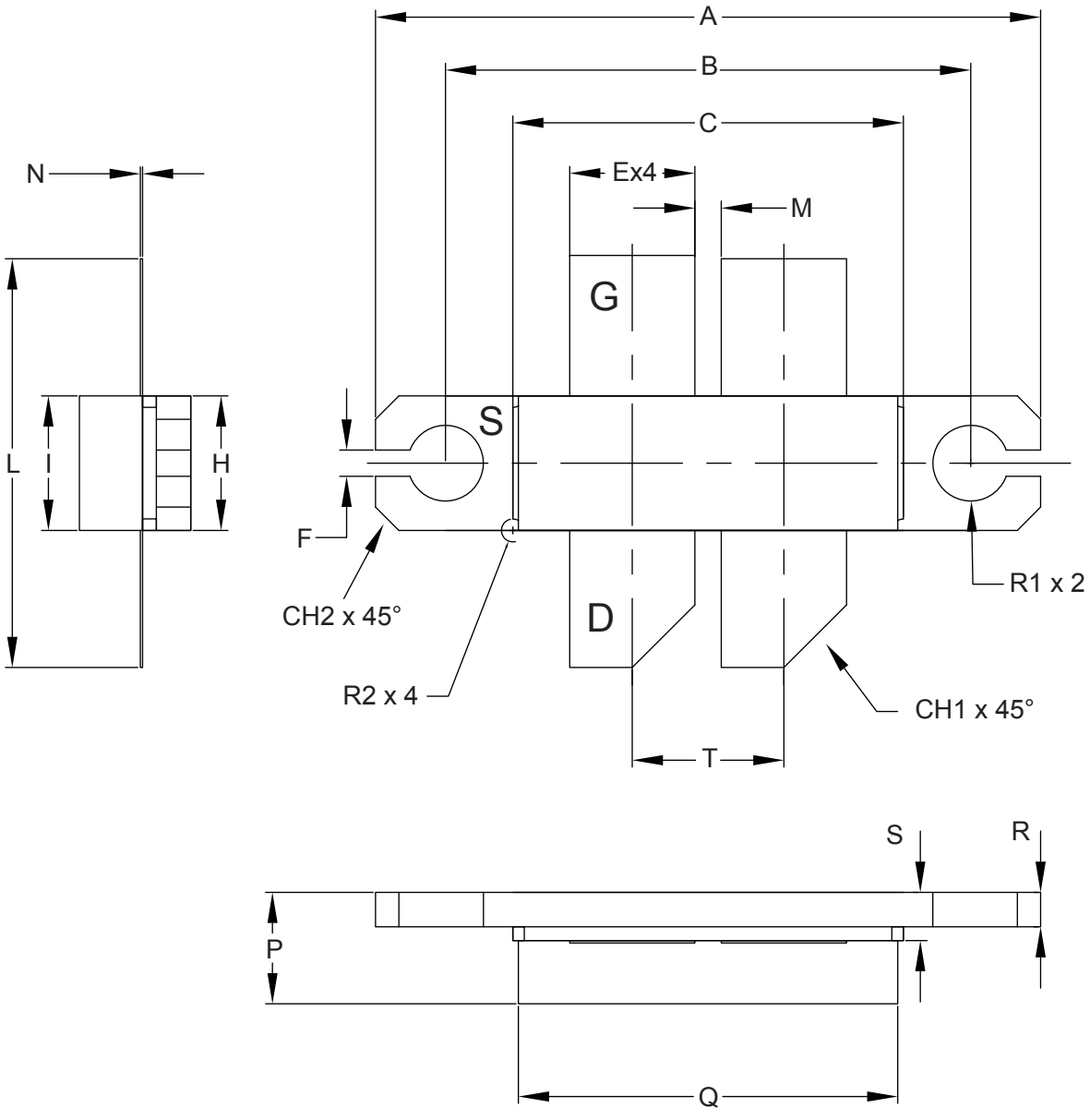

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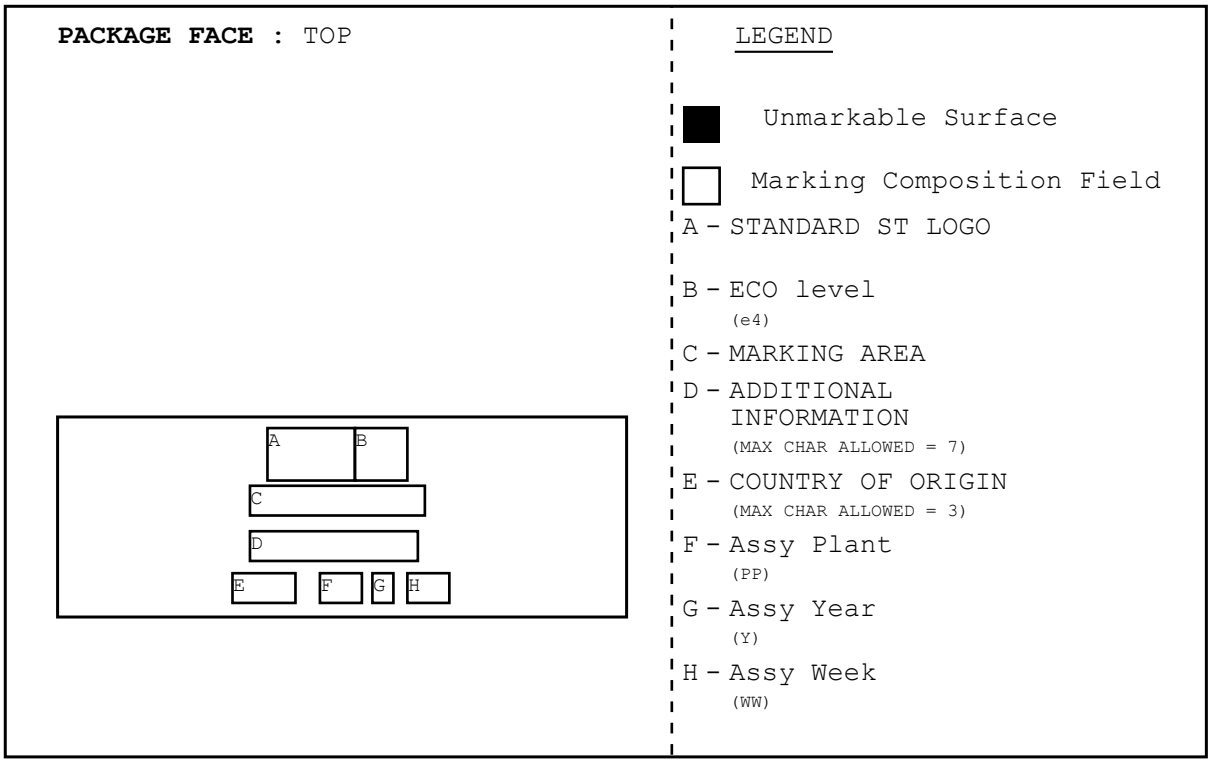
Table 8. **LBB mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A	28.82	28.95	29.08
B	22.73	22.86	22.99
C	16.87	17.00	17.13
E	5.32	5.45	5.58
F	1.01	1.14	1.27
H	5.72	5.85	5.98
I	5.72	5.85	5.98
L	17.65	17.78	17.91
M	1.02	1.15	1.28
N		0.10	
P	4.72	4.85	4.98
Q	16.38	16.51	16.64
R	1.37	1.50	1.63
S	1.97	2.10	2.23
T		6.60	
CH1		2.72	
CH2		1.02	
R1		1.65	
R2		0.50	

5.2 Marking information

Figure 5. **Marking composition**



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Revision history

Table 9. **Document revision history**

Date	Version	Changes
01-Jul-2020	1	First release
04-Oct-2021	2	Updated title and Device summary on cover page. Updated Section 1 Electrical ratings. Updated Section 2 Electrical characteristics. Updated Figure 1. Power gain and drain efficiency versus output power (f = 108 MHz). Updated Section 4 Test circuits. Added Section 5.2 Marking information. Minor text changes.

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