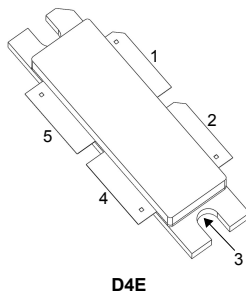


750 W, 50 V, 1200 to 1400 MHz RF power LDMOS transistor



D4E

Pin connection	
Pin	Connection
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
RF5L1214750CB4	1300 MHz	50 V	750 W	15 dB	53%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally matched pair transistors in push-pull configuration
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the European directive 2002/95/EC

Applications

- L-Band radar
- From 1300 to 1500 MHz particle accelerator

Description

The RF5L1214750CB4 is a 750 W, 50V high performance LDMOS FET, designed for L-Band radar and particle accelerator in the frequency range from 1300 to 1500 MHz.



Product status link
RF5L1214750CB4

Product summary	
Order code	RF5L1214750CB4
Marking	5L1214750
Package	D4E
Packing	Tray
Base/bulk quantity	20/100

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	110	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	55	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	0.02	°C/W

1. $T_C = 80\text{ °C}$, $P_{OUT} = 1\text{ kW}$, pulse width = 100 μs , duty cycle = 10%.

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device mode (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_{DS} = 100\ \mu\text{A}$	110	-		V
I_{DSS}	Zero gate voltage drain leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		-	10	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 90\text{ V}$		-		
I_{GSS}	Gate-source leakage current	$V_{GS} = -8/10\text{ V}, V_{DS} = 0\text{ V}$		-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$I_D = 600\ \mu\text{A}$	1	-	3	V
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 1\text{ V}, I_{DS} = 100\text{ mA}$	2	-	5	V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}, I_{DS} = 10\text{ A}$		-	1.2	V
$I_{DS(on)}$	Static drain-source on-current	$V_{GS} = 10\text{ V}, V_{DS} = 100\text{ mV}$		-	2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}, V_{DS} = 100\text{ mV}$		-	1	Ω

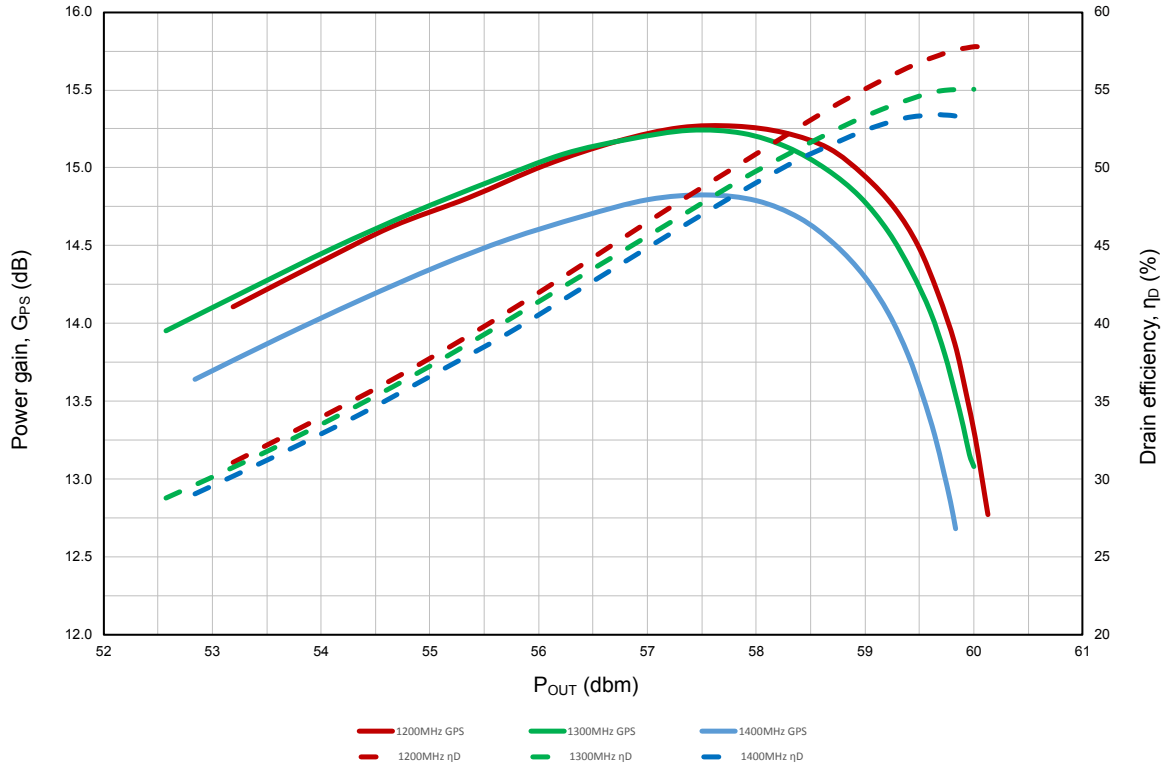
Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	$f = 1300\text{ MHz}$		750		W
G_{PS}	Power gain		-	15		dB
η_D	Drain efficiency		-	53		%
VSWR	Load mismatch	$P_{OUT} = 750\text{ W}, \text{all phases}$	-		10:1	

Note: $V_{DD} = 50\text{ V}, I_{DQ} = 150\text{ mA}, \text{pulse CW} = 100\ \mu\text{s}, \text{duty cycle} = 10\%$.

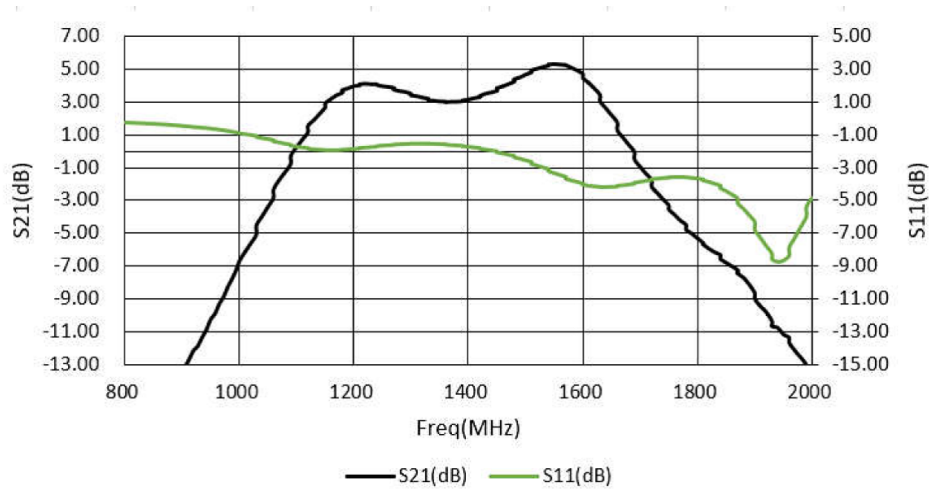
3 Typical performances

Figure 1. Power gain and drain efficiency vs output power (over 1200 - 1400 MHz frequency band)



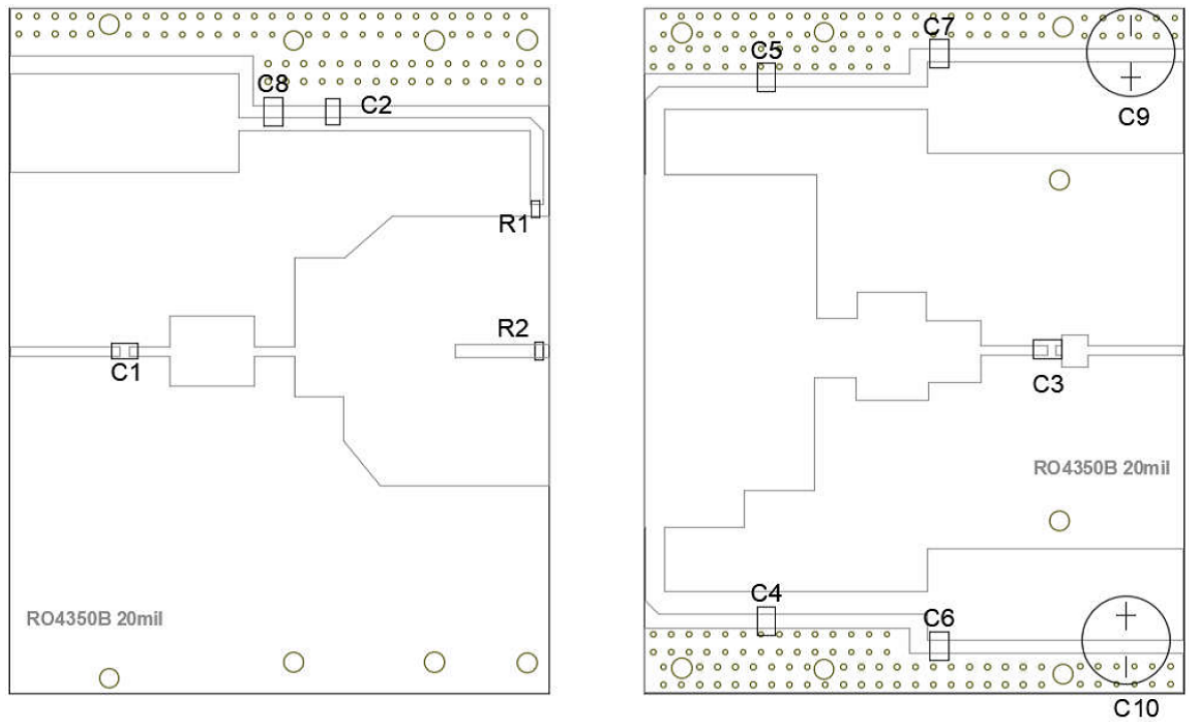
Note: $V_{DD} = 50\text{ V}$, $I_{DQ} = 150\text{ mA}$, pulsed CW, pulse width = 100 μs .

Figure 2. Small signal gain and return loss (S21 and S11)



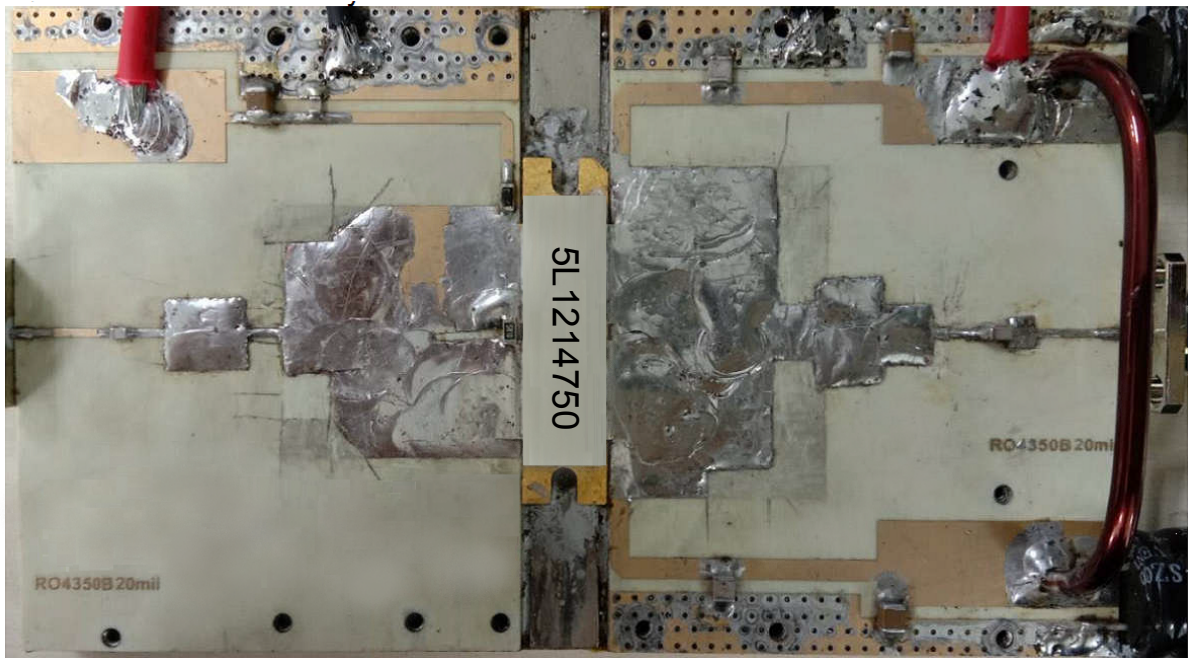
Note: $V_{DD} = 50\text{ V}$, $I_{DQ} = 400\text{ mA}$, $p_{in} = 0\text{ dBm}$.

4 Test circuits

Figure 3. Test circuit layout

Table 6. Components list

Component	Value	Size	Reference
C1, C2	47 pF	0805	ATC600F
C3, C4, C5	47 pF	0805	ATC800B
C6, C7, C8	10 μ F	1210	50 V ceramic multilayer capacitor
C9, C10	1000 μ F		63 V aluminum electrolytic capacitor
R1	15 Ω	0805	
R2	5.1 Ω	0805	
PCB	0.508 mm (0.020") thick, $\epsilon_r = 3.48$, Rogers RO4350B, 1 oz. copper		

Figure 4. Test circuit photo

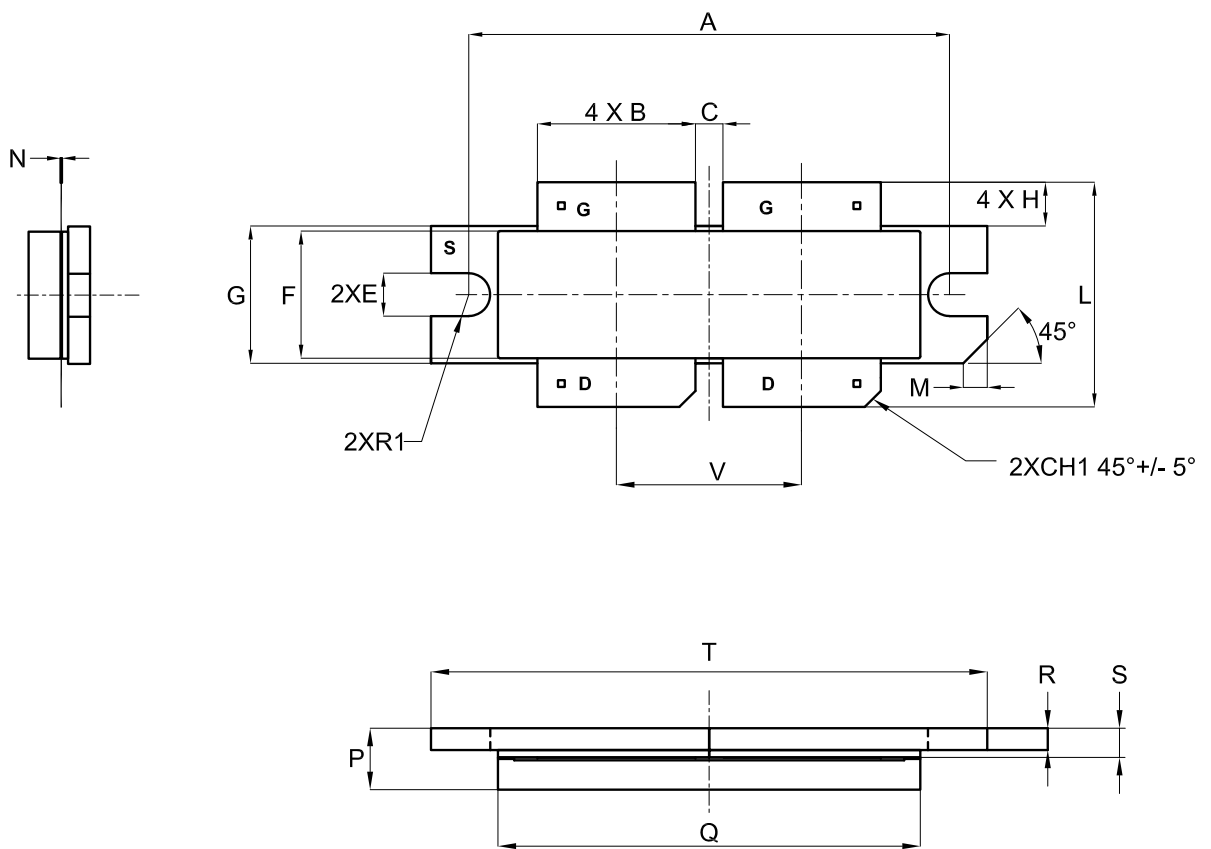


5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 D4E package information

Figure 5. D4E package outline



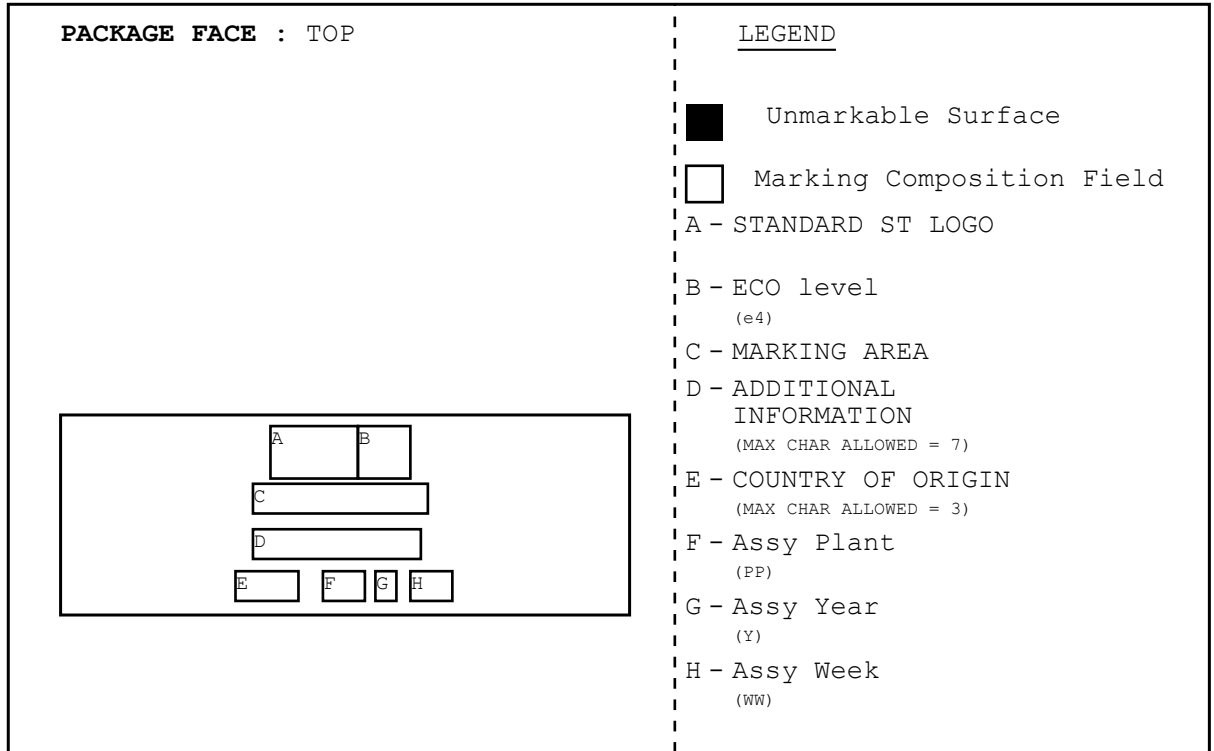
DM0066713_2

Table 7. D4E package mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	35.44	35.56	35.68
B	11.56	11.68	11.80
C	1.92	2.04	2.16
E	3.06	3.18	3.30
F	9.25	9.40	9.50
G	10.04	10.16	10.28
H	5.72	5.85	3.48
L	16.11	16.62	17.13
M	1.51	1.78	2.05
N	0.10	0.13	0.16
P	4.17	4.55	4.93
Q	30.96	31.24	31.52
R	1.55	1.62	1.69
S	2.09	2.16	2.23
T	41.08	41.22	
V	13.60	13.72	13.84
R1		1.59	
CH1		1.19	

5.2 Marking information

Figure 6. Marking composition



GADG040220211644GT

Revision history

Table 8. Document revision history

Date	Revision	Changes
16-Feb-2021	1	First release.
22-Sep-2021	2	Updated Table 3. ESD protection. Updated Table 4. Static (per side). Minor text changes.

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