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RF6263

3V 900MHZ LINEAR POWER AMPLIFIER MODULE

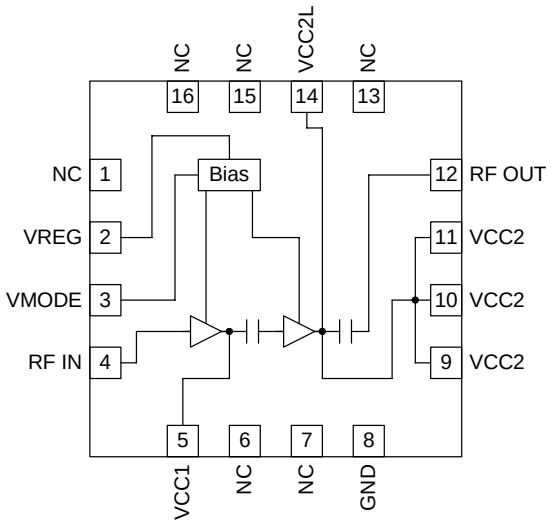
RoHS Compliant & Pb-Free Product
Package Style: QFN, 16-Pin, 3x3

Features

- Input Internally Matched@50Ω
- Output Internally Matched
- 23% Linear Efficiency @ 19dBm
- 40% Linear Efficiency @ 28dBm
- -50dBc ACPR @ 885kHz
- 18mA Idle Current in LPM

Applications

- 3V CDMA/AMPS Cellular Handset
- 3V CDMA2000/1XRTT Cellular Handset
- 3V CDMA2000/1X-EV-DO US-Cellular Handset
- Spread-Spectrum System



Functional Block Diagram

Product Description

The RF6263 is a high-power, high-efficiency linear amplifier module specifically designed for 3V handheld systems. The device is manufactured on an advanced third generation GaAs HBT process, and was designed for use as the final RF amplifier in 3V IS-95/CDMA2000-1X/ AMPS handheld digital cellular equipment, spread-spectrum systems, and other applications in the 824MHz to 849MHz band. The RF6263 has a digital control pin which when enabled will allow the amplifier to operate up to 19dBm output power with reduced current consumption. The low power mode current consumption can be reduced by more than 50% that of a standard power amplifier. The RF6263 is assembled in a 16-pin, 3mmx3mm, QFN package.

Ordering Information

RF6263	3V 900MHz Linear Power Amplifier Module
RF6263PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V
Supply Voltage ($P_{OUT} \leq 31$dBm)	+5.2	V
Control Voltage (V_{REG})	+3.9	V
Input RF Power	+10	dBm
Mode Voltage (V_{MODE})	+3.9	V
Operating Temperature	-30 to +110	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity Level (IPC/JEDEC J-STD-20)	MSL 2 @ 260 °C	

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power Mode - CDMA (V_{MODE} Low)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=0V, and P_{OUT}=28dBm for all parameters (unless otherwise specified).
Operating Frequency Range	824		849	MHz	
Linear Gain		28		dB	
Second Harmonics		-35	-30	dBc	
Third Harmonics		-40	-30	dBc	
Maximum Linear Output	28				
Linear Efficiency		40		%	
Maximum I_{CC}		465		mA	
ACPR @ 885kHz		-50		dBc	
ACPR @ 1.98MHz		-58		dBc	
Input VSWR		2:1			
Stability in Band			6:1		No oscillation>-70dBc
Stability out of Band			10:1		No damage
Noise Power		-133		dBm/Hz	At 45MHz offset.
Low Power Mode - CDMA (V_{MODE} High)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=2.8V, and P_{OUT}=19dBm for all parameters (unless otherwise specified).
Operating Frequency Range	824		849	MHz	
Linear Gain		18		dB	
Maximum Linear Output	19				
Linear Efficiency		23		%	
Maximum I_{CC}		100		mA	
		70		mA	P_{OUT}=16dBm
ACPR @885kHz		-49		dBc	
ACPR @1.98MHz		-62		dBc	
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation>-70dBc
			10:1		No damage

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
FM Mode					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=0V, and P_{OUT}=30.5dBm for all parameters (unless otherwise specified).
Operating Frequency Range	824		849	MHz	
AMPS Maximum Output Power		30.5		dBm	
AMPS Efficiency		50		%	
AMPS Gain		28			
AMPS Second Harmonics		-35	-30	dBc	
AMPS Third Harmonics		-40	-30	dBc	
Power Supply					
Supply Voltage	3.2	3.4	4.2	V	
High Gain Idle Current		55		mA	V_{MODE}=low and V_{REG}=2.8V
Low Gain Idle Current		18		mA	V_{MODE}=high and V_{REG}=2.8V
V_{REG} Current		2.5		mA	V_{MODE}=high
V_{MODE} Current		500		uA	
RF Turn On/Off Time			6	uS	
DC Turn On/Off Time			40	uS	
Total Current (Power Down)		0.2	2.0	uA	
V_{REG} Low Voltage	0		0.5	V	
V_{REG} High Voltage (Recommended)	2.75	2.85	2.95	V	
V_{REG} High Voltage (Operational)	2.7		3.0	V	
V_{MODE} Voltage	0		0.5	V	High Gain Mode
	2.0		3.0	V	Low Gain Mode

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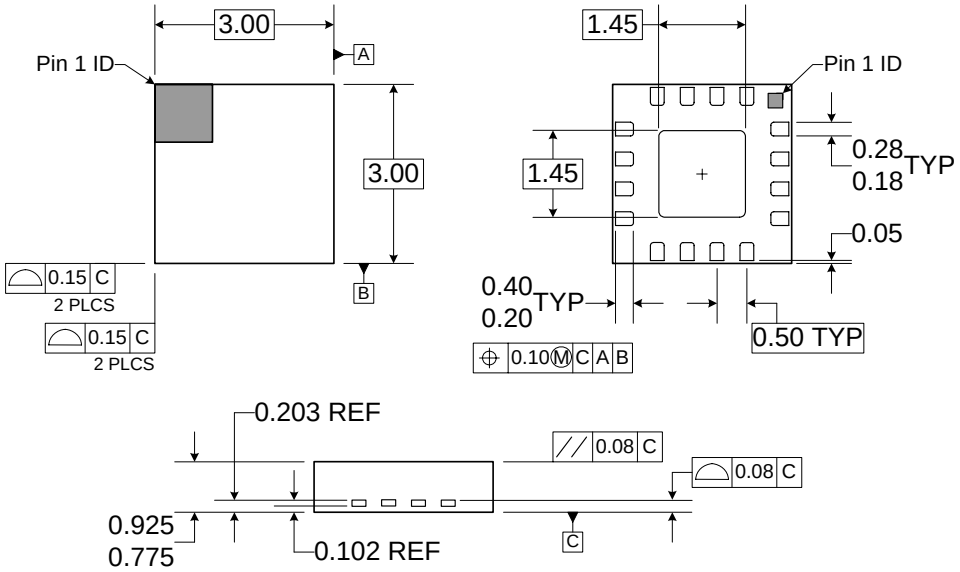
Pin	Function	Description	Interface Schematic
1	NC	No connection. Do not connect this pin to any external circuit.	
2	VREG	Regulated voltage supply for amplifier bias circuit. In power down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
3	VMODE	For nominal operation (High Power mode), V_{MODE} is set LOW. When set HIGH, devices are biased lower to improve efficiency.	
4	RF IN	RF input internally matched to 50Ω. This input is internally AC-coupled.	
5	VCC1	First stage collector supply. A 2200pF and 4.7μF decoupling capacitor are required.	
6	NC	No connection. Do not connect this pin to any external circuit.	
7	NC	No connection. Do not connect this pin to any external circuit.	
8	NC	No connection. Do not connect this pin to any external circuit.	
9	VCC2	High power output stage collector supply. Refer to schematic for required external components.	
10	VCC2	Same as pin 9.	
11	VCC2	Same as pin 9.	
12	RF OUT	RF output. Internally AC-coupled.	
13	NC	No connection. Do not connect this pin to any external circuit.	
14	VCC2L	Low power output stage collector supply. Refer to schematic for required external components.	
15	NC	No connection. Do not connect this pin to any external circuit.	
16	NC	No connection. Do not connect this pin to any external circuit.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Package Drawing



Shaded areas represent pin 1. ***Dimensions in mm.***

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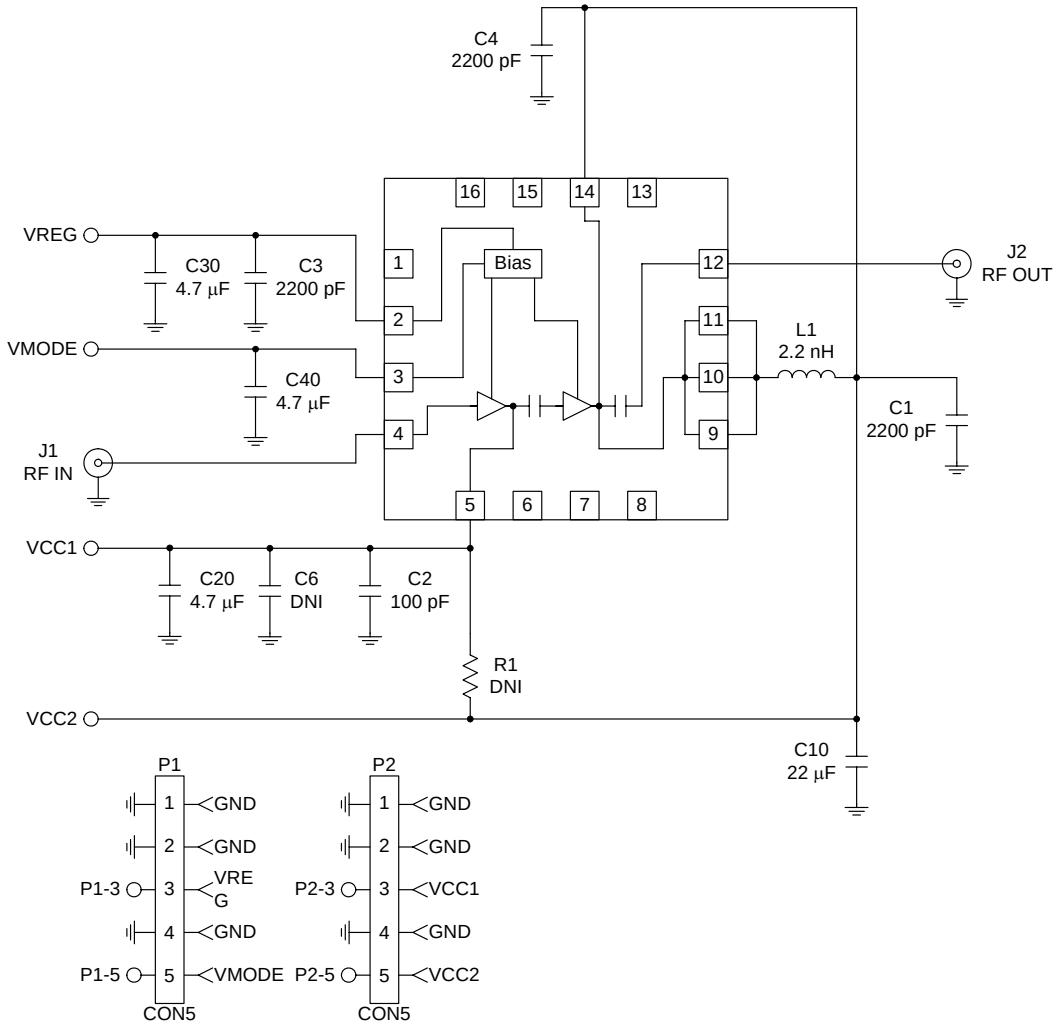
Evaluation Board Schematic - CDMA



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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for PFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

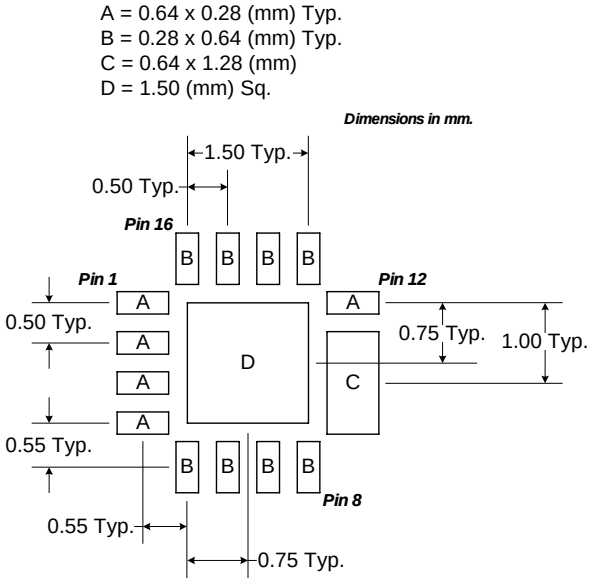

Figure 1. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

A = 0.74 x 0.38 (mm) Typ.
B = 0.38 x 0.74 (mm) Typ.
C = 1.60 (mm) Sq.

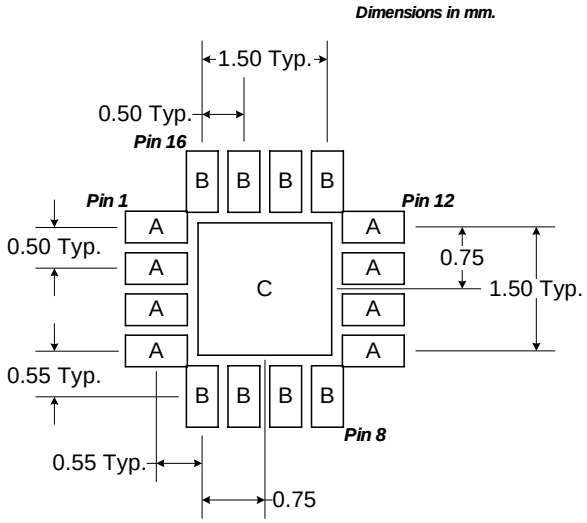

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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Tape and Reel Information

Carrier tape basic dimensions are based on EIA481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

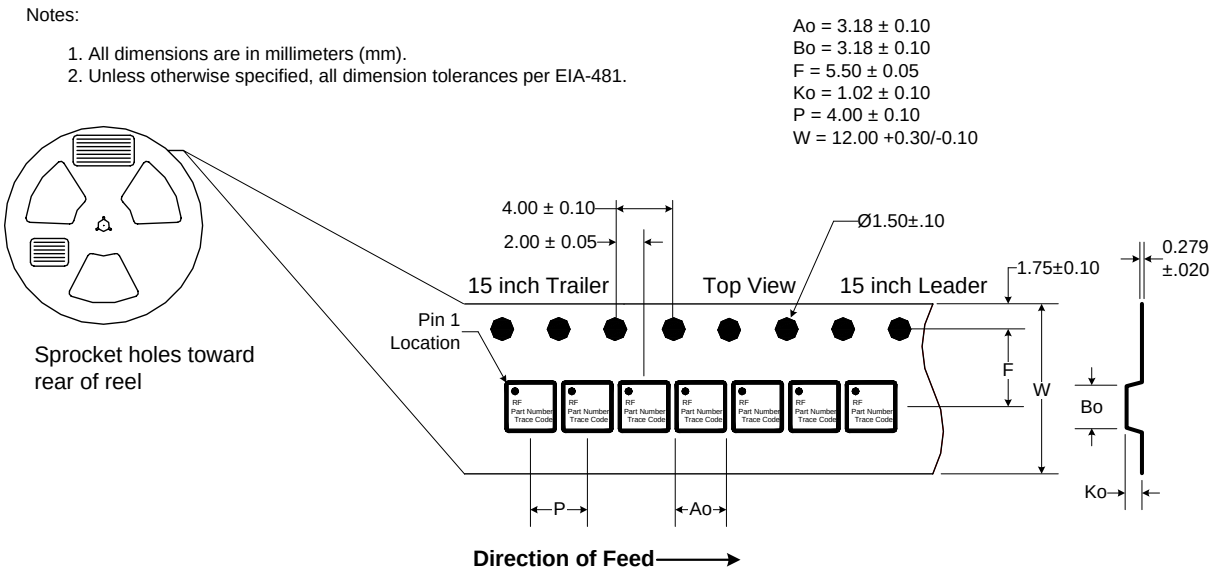
Carrier tape is wound or placed onto a shipping reel either 330 mm (13 inches) in diameter or 178 mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier, ESD bag, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, column 8 of Joint Industry Standard IPC/JEDEC J-STD-033A.

The following table provides useful information for carrier tape and reels used for shipping the devices described in this document.

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF6263TR7	7 (178)	2.4 (61)	12	4	Single	2500

QFN (Carrier Tape Drawing with Part Orientation)



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