RF6280

POWER MANAGEMENT IC

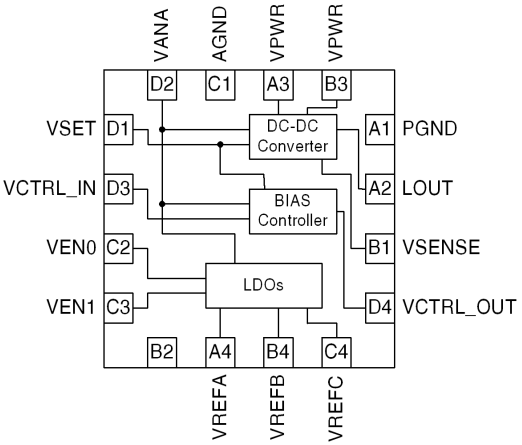
Package Style: 15-Bump WLCSP, 4x4 Array, 2mmx2mm

Features

- Peak Efficiency Up To 96%
- High Efficiency Over Various Loads
- Transient Response < 10µs
- 650mA Current Capability
- Variable Output Voltage (0V to V_{BATT})
- 2.5MHz PWM Switching Frequency
- Automatic Bypass Mode
- Over Temperature Shutdown
- Current Limit
- Analog Bias Control (Automatic and Buffer)
- Three Individual Fast Transient 2.85V LDOs
- Controls up to 3 UMTS PAs
- Small, Wafer-Level, Chip-Scale Package

Applications

- W-CDMA Handsets



Functional Block Diagram

Product Description

The RF6280 is a multi-functional Power Management IC which is used in conjunction with power amplifiers and designed to be used in 3V handheld systems. The RF6280 consists of a Pulse Width Modulated (PWM) voltage mode DC-DC converter, three 2.85V LDOs, and analog bias control circuit to adjust the PA bias. The DC-DC Converter is a buck converter that provides high efficiency over a wide output voltage range with minimal ripple. It has a fast response to load and line transients, and fast response to programmed (V_{SET}) voltage changes. The converter includes an auto-bypass function which allows the handset to operate at lower battery voltage while helping maintain PA linearity at maximum output power. The converter output voltage is set by a variable control voltage, V_{SET}. The RF6280 has three individual LDOs which are enabled by a digital two bit logic signal. The three LDO outputs are used for band select in tri-band W-CDMA handsets.

Ordering Information

RF6280	Power Management IC
RF6280PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

Absolute Maximum Ratings

Parameter	Rating	Unit
Input Supply Voltage (V_{BAT_ABS})	-0.2 to +6.0	V
Analog Input (V_{SET})	V_{BAT}-0.2	V
V_{CTRL_IN}	V_{BAT}-0.2	V
$V_{ENO,1}$	V_{BAT}-0.2	V
Operating Ambient Temperature (T_{CASE})	-30 to +85	°C
Storage Temperature (T_{STORE})	-40 to +150	°C
Electrostatic Protection (V_{HBM})	-2000 to +2000	V
Maximum Junction Temperature	150	°C
Converter Output Current	1000	mA
LDO Output Current	10	mA
Analog Bias Control Current	5	µA

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DC-DC Converter					L=1.5µH, C3=4.7µF, 25°C, V_{BAT}=3.7V (typ.); Min/Max: -30°C to 85°C, V_{BAT}=3.0V to 5.5V
Operating Battery Voltage (V_{BAT})	3.0	3.7	5.5	V	
V_{SET} (V_{SET})	0		2.0	V	
V_{SET} Current			1.0	µA	V_{SET}=1.7V
V_{OUT} Transfer Function Gain	2.35	2.45	2.55	V/V	V_{SET}=0.24V to 1.36V, V_{OUT}/V_{SET}
Output Current (I_{LOAD})			650	mA	
Load Regulation		2	30	mV/A	I_{OUT}=25mA to 200mA, V_{OUT}=1V
Line Regulation		0.8	20	mV/V	V_{BAT}=3.1V to 4.6V, I_{LOAD}=100mA, V_{OUT}=1.0V
Dropout Voltage (V_{DO}) 100% DC		175	300	mV	V_{SET}=1.6V, I_{LOAD}=500mA, ResrL=100mΩ
Dropout Voltage (Bypass)		60	100	mV	V_{BAT}=3.1V, V_{SET}=1.7V, I_{LOAD}=500mA, ResrL=100mΩ
Output Ripple Voltage		8	30	mV_{P-P}	V_{OUT}=1.85V, duty cycle=50%
Efficiency (DC-to-DC Converter)		96		%	I_{LOAD}=460mA, V_{OUT}=3.4V
		92		%	I_{LOAD}=200mA, V_{OUT}=1.5V
		60		%	I_{LOAD}=25mA, V_{OUT}=0.6V
Frequency (F_{SW})	1.50	2.50	3.50	MHz	
DC Idle Current		1.30	2.75	mA	V_{SET}=0V, no load, V_{CTRL_IN}=1.0V (buffer mode)
DC Idle Current		1.60	2.75	mA	V_{SET}=0V, no load, V_{CTRL_IN}=0V (auto V_{CTRL} mode)
DC Leakage			1.0	µA	V_{SET}=0V, no load, V_{EN1}=V_{ENO}=0V
V_{OUT} Start-up Time		10	30	µs	V_{OUT}=0V to 3.4V, no load
		8	30	µs	V_{OUT}=0V to 0.6V, no load
V_{OUT} Transition Time - Rising		4	25	µs	V_{OUT}=0.6V to 3.4V, I_{LOAD}=450mA
V_{OUT} Transition Time - Falling		5	25	µs	V_{OUT}=3.4V to 0.6V, I_{LOAD}=15mA
V_{SET} Bypass Voltage (V_{SETBYP})	1.45	1.55	1.65	V	V_{BAT}<3.3V
Bypass to SMPS Transition Time		20	50	µs	V_{SET}<1.45V, V_{BATT}>3.70V

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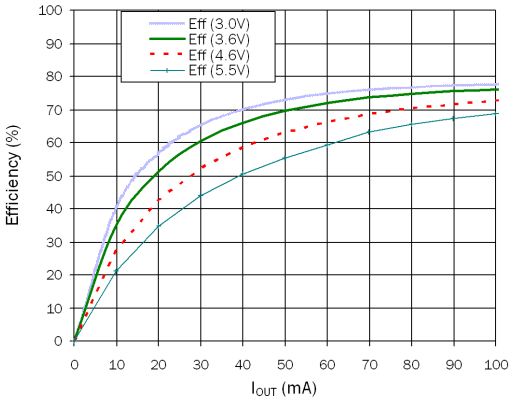
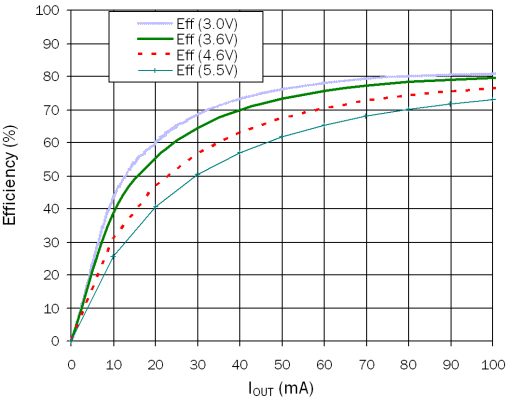
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DC-DC Converter, cont.					
SMPS to Bypass Transition Time		4	5	µs	V_{SET}>1.65V, V_{BATT}<3.20V
Enable Logic Pin High (V_{EN1H}, V_{EN0H})	1.20			V	V_{EN0} or V_{EN1} will enable DC to DC converter
Enable Logic Pin Low (V_{EN1L}, V_{EN0L})			0.6	V	V_{EN0} and V_{EN1} at low level will disable DC to DC converter
V_{EN0}, V_{EN1} Current			1.0	µA	V_{EN0}, V_{EN1}=1.7V
Thermal Shutdown	135	140	145	°C	
Thermal Hysteresis		15		°C	
Current Limit (I_{LIM})		1.6	3.0	A	
SMPS PSRR		60		dB	V_{OUT}=1.0V, 10kHz
		52		dB	V_{OUT}=1.0V, 1MHz
Controller					
V_{REF} Start-up Time		2	5	µs	$V_{EN0,1}$=0V to 1.3V
V_{REF} Output Voltage	2.60	2.85	3.10	V	
I_{REF}		2	10	mA	
V_{REF} Load Regulation		3	15	mV/mA	I_{REF}=0mA to 5mA
V_{REF} Line Regulation		3	20	mV/V	V_{BATT}=3.0V to 4.6V
V_{REF} PSRR		45		dB	10kHz, I_{REF}=5mA
V_{CTRL_IN}	0		2.4	V	
V_{CTRL_IN} Current			1.0	µA	V_{CTRL_IN}=2.4V
V_{CTRL_OUT} Start-up Time		3	10	µs	$V_{EN0,1}$=0V to 1.3V, V_{CTRL_IN}=0V to 2.4V
V_{CTRL_OUT} Response Time		1	10	µs	$V_{EN0,1}$=1.3V, V_{CTRL_IN}=1.0V to 2.0V
V_{CTRL_OUT} (Buffer Mode)	0.95	1.00	1.05	V	V_{CTRL_IN} to V_{CTRL_OUT}, I_L=500µA, V_{CTRL_IN}=1.0V
V_{CTRL_OUT} (Automatic Mode)	1.00	1.17	1.30	V	V_{CTRL_IN}<0.3V, I_L=500µA, V_{SET}=0V

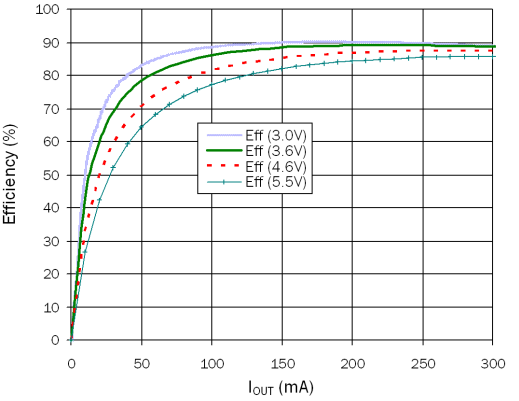
Efficiency (Buffer Mode) versus I_{OUT} (V_{OUT}=0.6V)



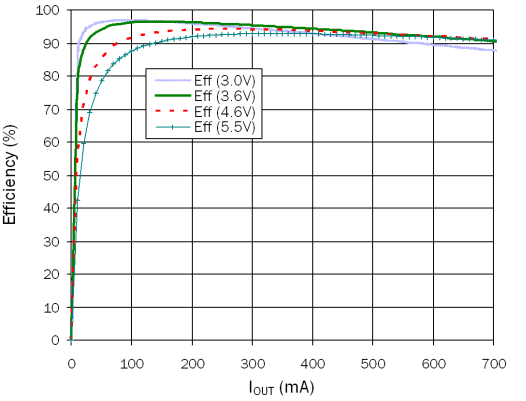
Efficiency (Buffer Mode) versus I_{OUT} (V_{OUT}=0.8V)



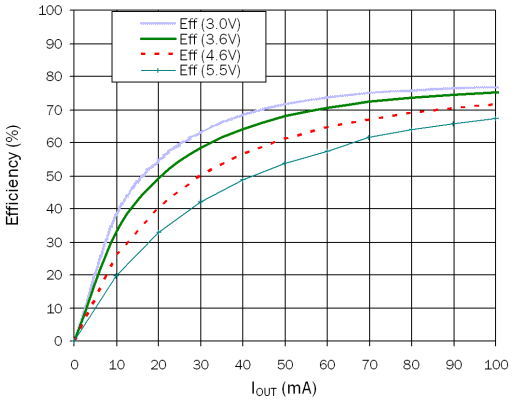
Efficiency (Buffer Mode) versus I_{OUT} (V_{OUT}=1.5V)



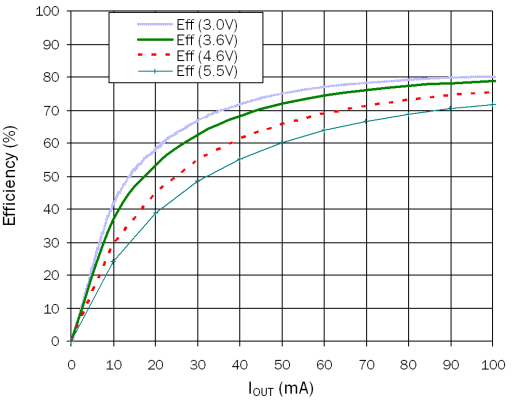
Efficiency (Buffer Mode) versus I_{OUT} (V_{OUT}=3.4V)



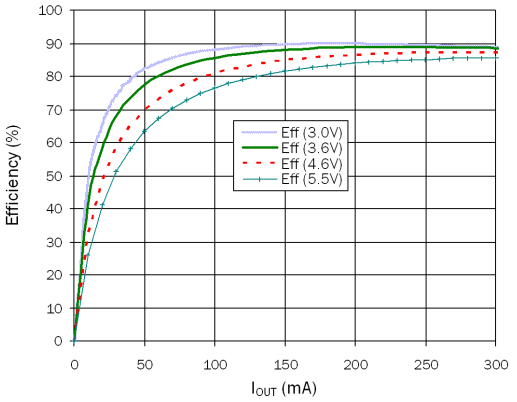
Efficiency (ABC Mode) versus I_{OUT} (V_{OUT}=0.6V)



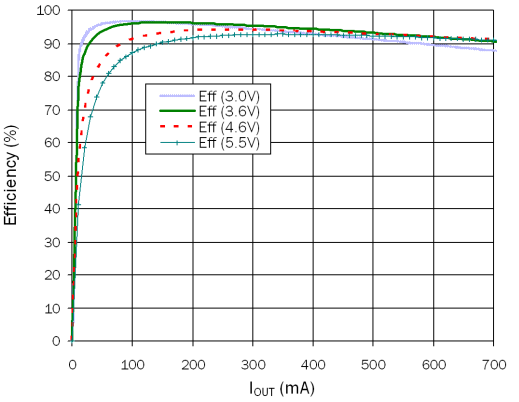
Efficiency (ABC Mode) versus I_{OUT} (V_{OUT}=0.8V)



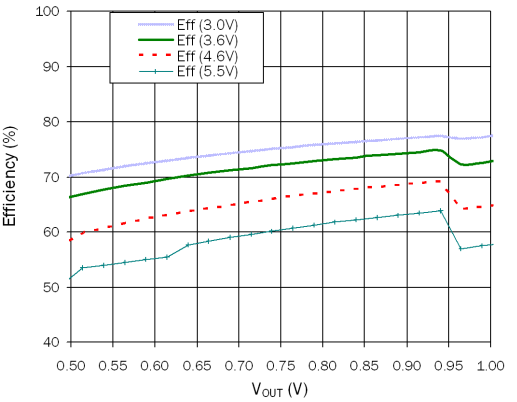
Efficiency (ABC Mode) versus I_{OUT} (V_{OUT}=1.5V)



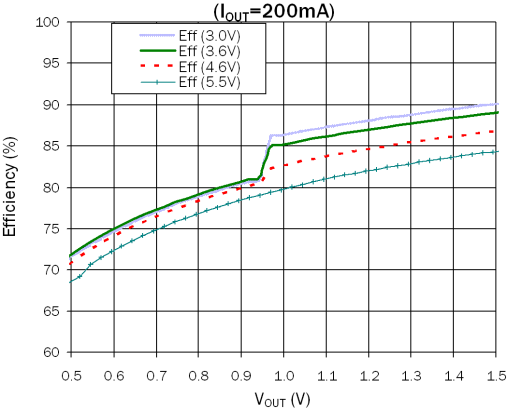
Efficiency (ABC Mode) versus I_{OUT} (V_{OUT}=3.4V)



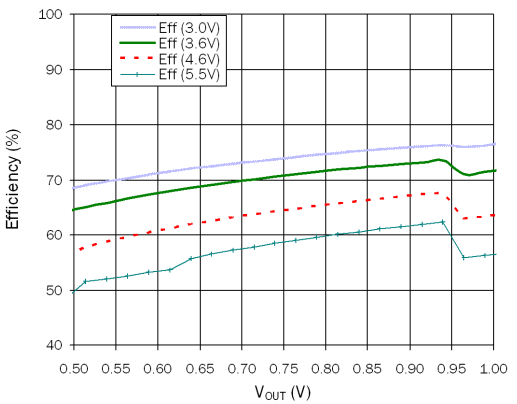
Efficiency (Buffer Mode) versus V_{OUT} (I_{OUT}=50mA)



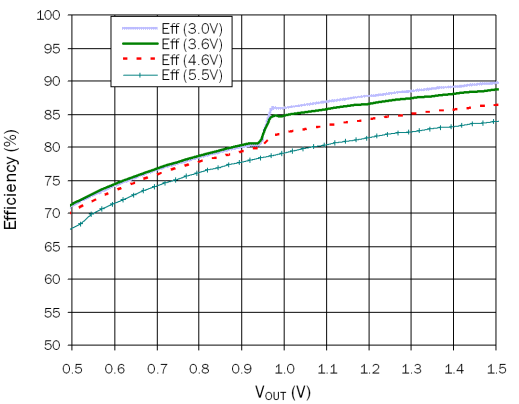
Efficiency (Buffer Mode) versus V_{OUT} (I_{OUT}=200mA)



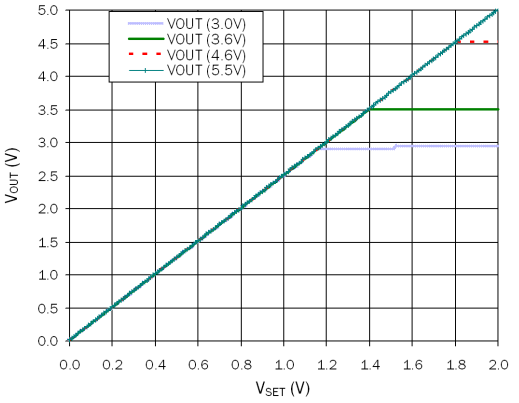
Efficiency versus V_{OUT} (I_{OUT}=50mA)



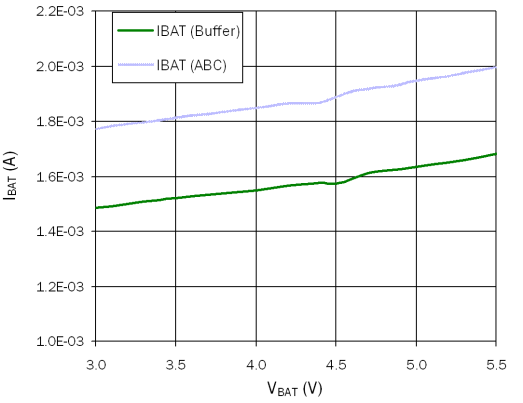
Efficiency (ABC Mode) versus V_{OUT} (I_{OUT}=200mA)



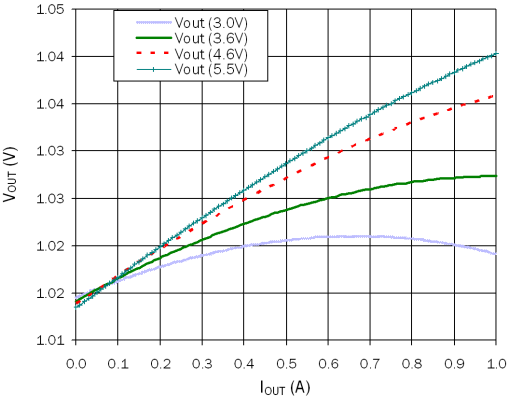
V_{OUT} versus V_{SET} (I_{OUT}=200mA)



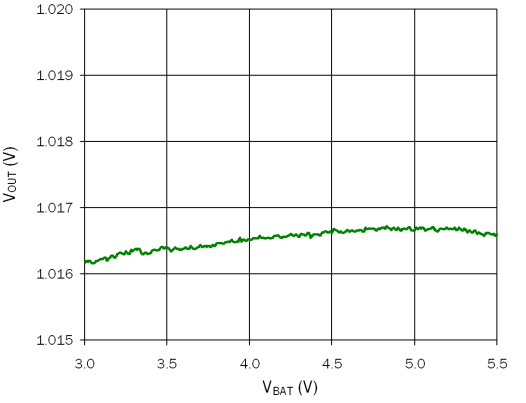
DC Idle Current



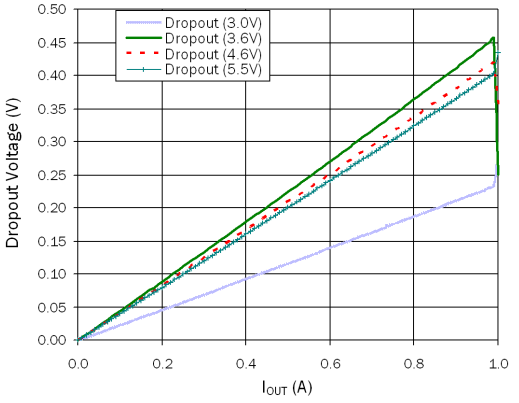
Load Regulation



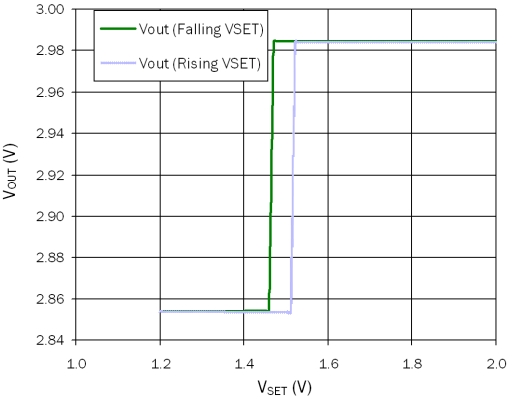
Line Regulation



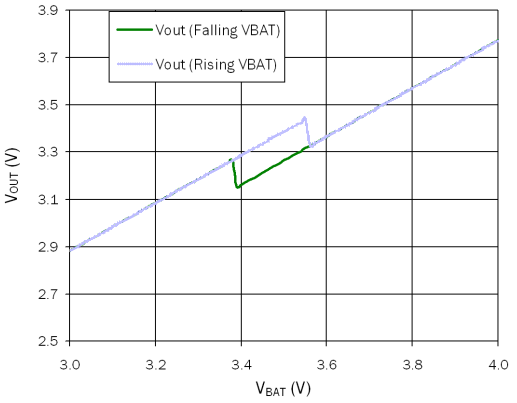
Dropout Voltage



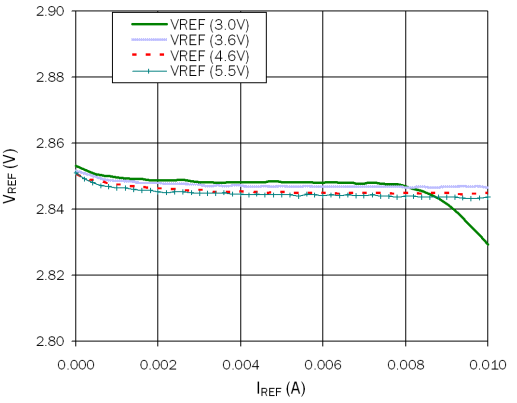
Bypass FET Threshold (Change V_{SET})



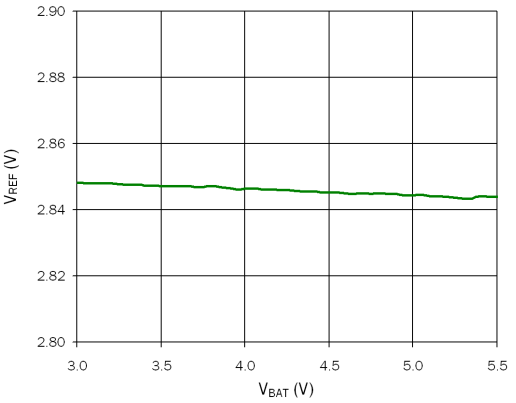
Bypass FET Threshold (V_{BAT} Change)



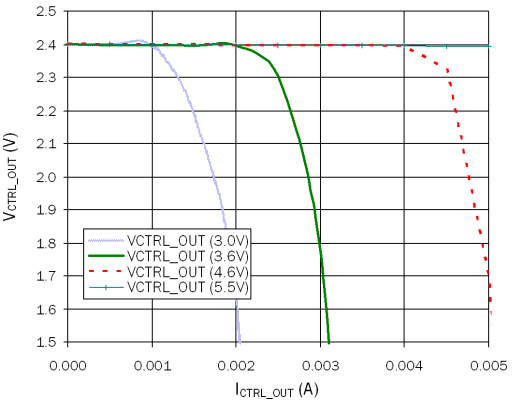
V_{REF} Load Regulation



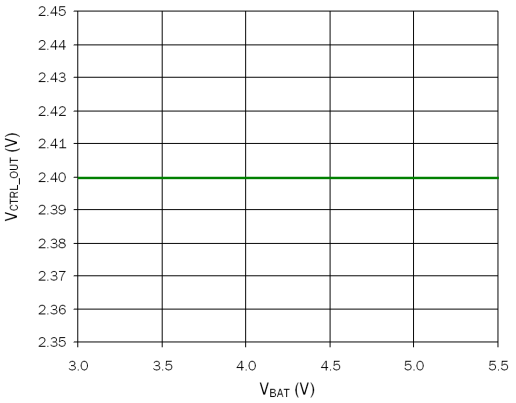
V_{REF} Line Regulation (I_{REF}=5mA)



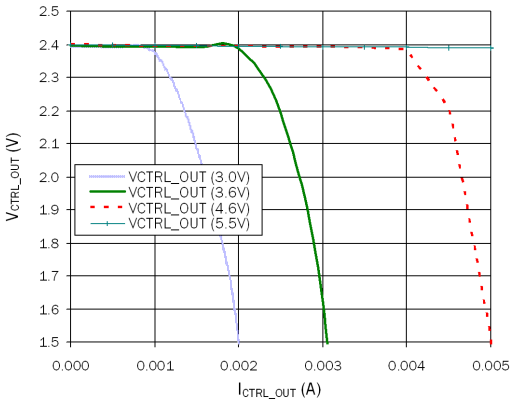
Buffer Load Regulation



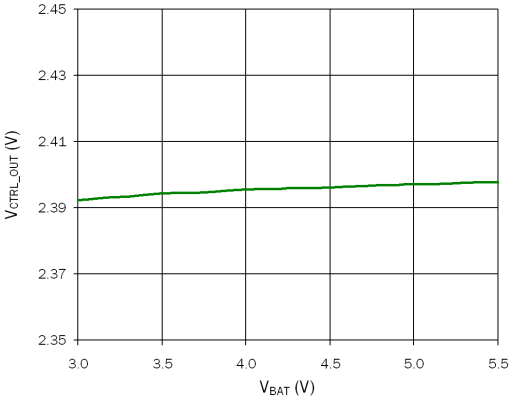
Buffer Line Regulation



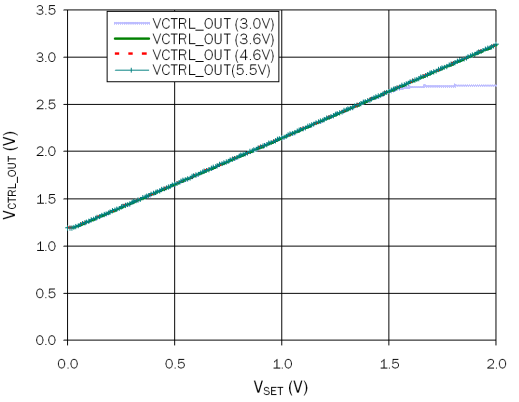
Auto Bias Control Load Regulation



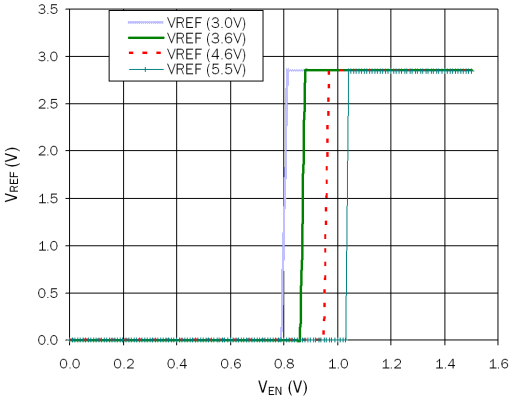
Auto Bias Control Line Regulation



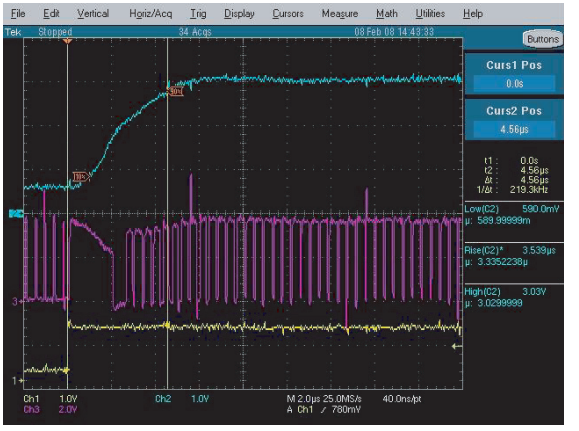
ABC Transfer Function



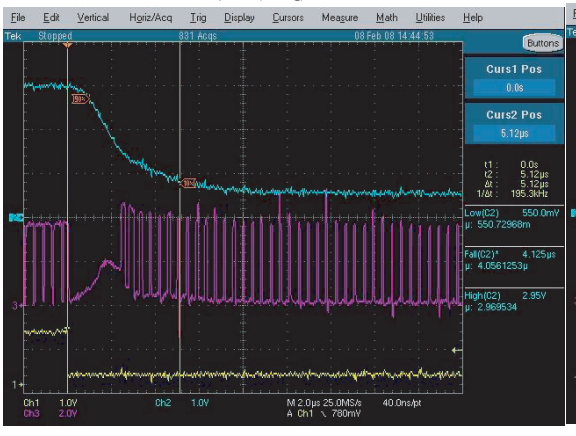
V_{EN} Threshold



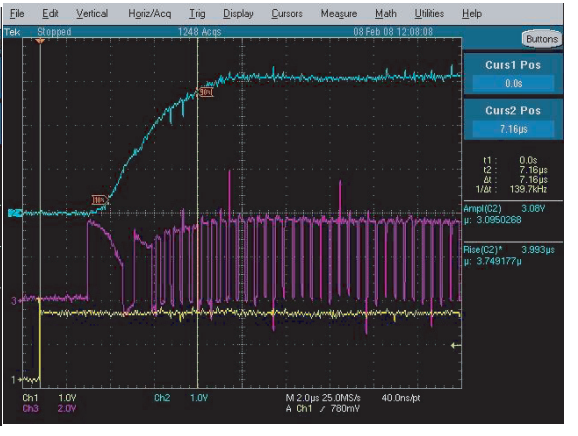
Transient Response (Rising) VOUT = 0.6V to 3.4V



Transient Response (Falling) VOUT = 3.4V to 0.6V



Turn-On Time (VOUT = 0V to 3.1V)



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Pin	Function	Description
A1	PGND	DC-DC Converter Power Ground.
A2	LOUT	DC-DC Converter Switch Output. Connect to the filter inductor as recommended on application schematic.
A3	VPWR	Supply used for the final output stage.
A4	VREFA	2.85V LDO output. Enabled when VEN0 is high and VEN1 is low. A 1nF capacitive load may be needed.
B1	VSENSE	Feedback node from the output. Connect to a point after the V_{OUT} inductor.
B2	NC	No connect. This pin is removed from the package.
B3	VPWR	Supply used for the final output stage.
B4	VREFB	2.85V LDO output. Enabled when VEN0 is low and VEN1 is high. A 1nF capacitive load may be needed.
C1	AGND	Ground for the analog circuits. Isolate from PGND to help reduce noise.
C2	VEN0	LDO enable input, refer to truth table for band select. This pin also enables the DC to DC converter and VCTRL circuitry.
C3	VEN1	LDO enable input, refer to truth table for band select. This pin also enables the DC to DC converter and VCTRL circuitry.
C4	VREFC	2.85V LDO output. Enabled when VEN0 and VEN1 are both high. A 1nF capacitive load may be needed.
D1	VSET	Analog reference input used to set the output voltage and VCTRL_OUT voltage if the Auto VCTRL feature is used by holding VCTRL_IN low.
D2	VANA	Supply used for the Analog circuitry inside the power management IC. Should be isolated from the VPWR supply with a ferrite bead. A 1µF decoupling capacitor may be needed.
D3	VCTRL_IN	Analog reference input used to set the PA bias voltage. If held low (<0.3V), Auto VCTRL will be enabled.
D4	VCTRL_OUT	Buffered output used to control the PA bias. Analog signal output is either a buffered VCTRL_IN or an internally generated signal controlled by VSET.

LDO Select Truth Table

LDO	V_{EN1}	V_{EN0}
A	L	H
B	H	L
C	H	H
Shutdown	L	L

Note: V_{EN0} or V_{EN1} at high level will enable the DC to DC converter and V_{CTRL} circuitry.

Bypass Control Table

Mode	V_{SET}	V_{BATT}
Bypass Enable	>1.55V	<3.35V
Bypass Disable	<1.45V	>3.55V

V_{CTRL} Table

Mode	V_{CTRL_IN}	V_{CTRL_OUT}
Automatic	<0.3V	$V_{CTRL\_OUT}=V_{SET}+1.14V$
Buffer	>1.0V	$V_{CTRL\_OUT}=V_{CTRL\_IN}$

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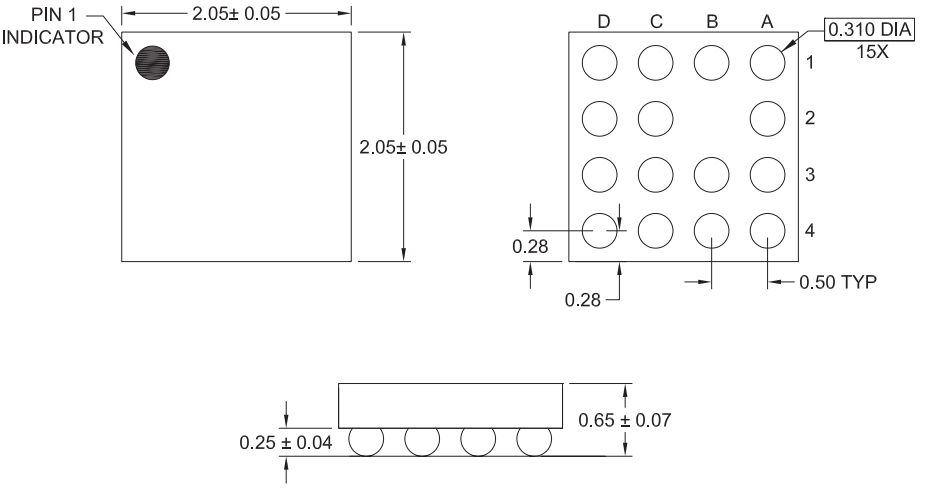
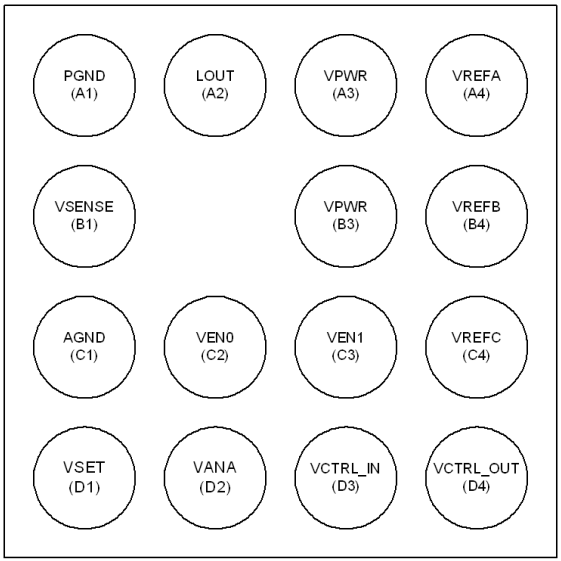
Package Drawing

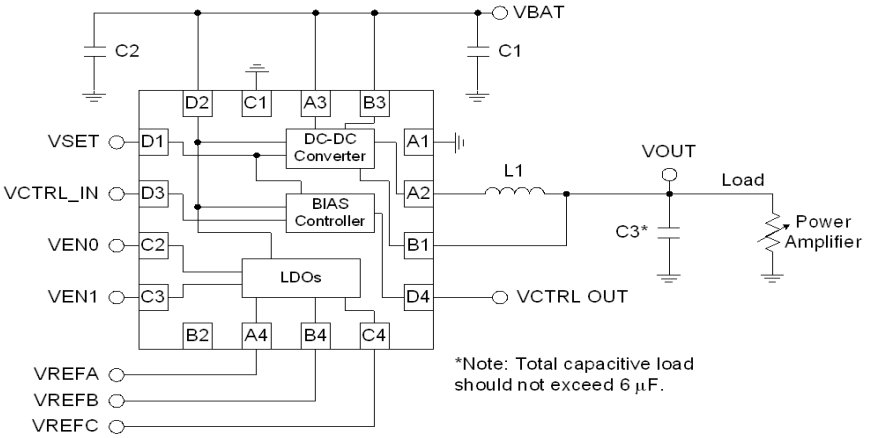


Pin Out



Notes:
1. 4x4 array (15 bumps)
2. SMPS Pins (8 bumps) VPWR (2), VANA, PGND, AGND, LOUT, VSET, VSENSE
3. Controller Pins (7 bumps) VEN1, VEN0, VREFA, VREFB, VREFC, VCTRL_IN, VCTRL_OUT
4. Bump dia.=300 μm, pitch=500 μm
5. Viewed from bottom side

Application Schematic



Designator	Case size	Qty	Value	Manufacturer	Part number
C3	0603	1	4.7uF	Taiyo Yuden	CEJMK107BJ475MA_T
	0603	1	4.7uF	Murata	GRM188R60J475KE19D
	0603	1	4.7uF	TDK	C1608X5R1A475K
C1	0805	1	10uF	Murata	GRM218R61A106KE19
	0805	1	10uF	Taiyo Yuden	CEJMK212BJ106KG_T
	0805	1	10uF	Panasonic	ECJ_2FB0J106M
C2	0402	1	1uF	Murata	GRM155R60J105ME19D
	0402	1	1uF	Taiyo Yuden	RMJMK105BJ105KVF
	0402	1	1uF	Panasonic	ECJ_0EB0J105M
L1	2.5x2.0x1.0	1	1.5uH	FDK	MIPS2520D1R5
	2.5x1.5x1.0	1	1.5uH	TDK	CPL2510T1R5M
	2.5x1.5x1.2	1	1.5uH	TDK	CPL2512T1R5M
	2.0x1.6x1.0	1	1.5uH	Murata	LQM2MPN1R5G0
	2.5x1.5x1.0	1	1.5uH	Murata	LQM2HPN1R5MG1
	2.5x2.0x1.2	1	1.5uH	FDK	MIPSA2520D1R5

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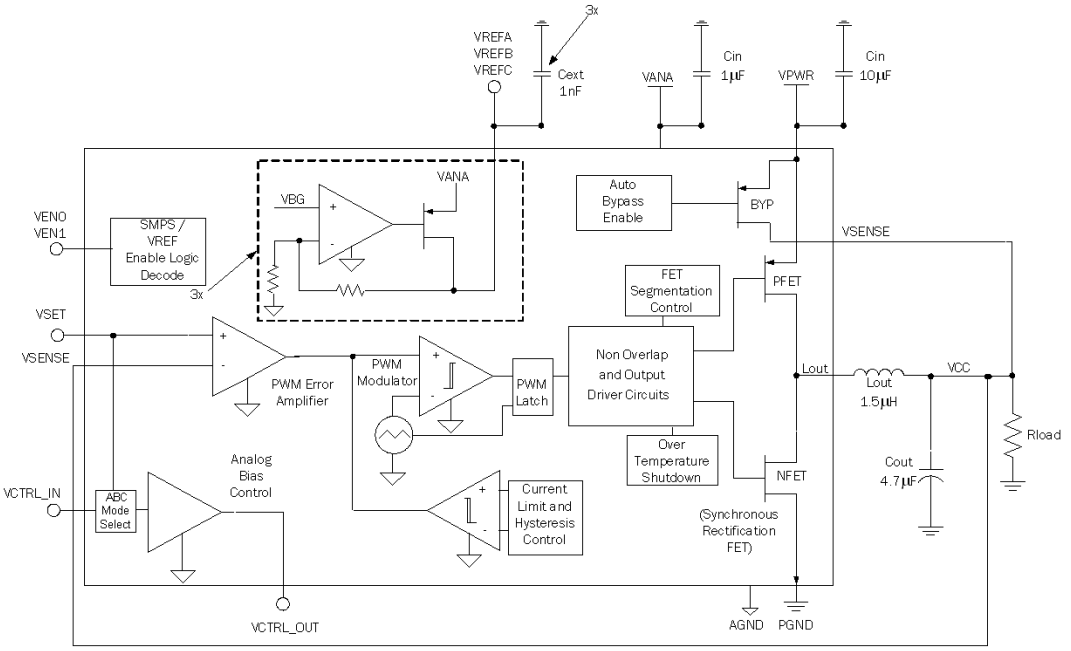
Theory of Operation

Overview



The RF6280 power management IC is designed to operate with up to 3 power amplifiers in 3V UMTS handheld systems. The RF6280 consists of one variable PWM voltage mode DC-DC buck converter, one bypass FET, three 2.85V LDOs and one analog bias controller. The DC-DC converter output voltage is determined by the analog input voltage on the V_{SET} pin ($V_{OUT}=V_{SET}*2.5$) with full output swing from 0V to V_{BATT}. The DC-DC converter has been optimized for high efficiency at light current load conditions and fast transient response times to meet UMTS 25µs slot-to-slot transition specifications while maintaining a maximum operating current of 650mA in either PWM or bypass modes. Bypass mode is automatically enabled when V_{BATT} is low and the V_{SET} pin is taken high (refer to Bypass Control Table for voltage levels). The converter is enabled in all operating modes except for shutdown.

The three V_{REF} LDOs are designed to operate at a typical output voltage of 2.85V and output current of 5mA. They have been optimized to meet voltage and current tolerance, noise and PSRR specifications while maintaining transient start-up performance (see electrical specifications). The state of the V_{EN0} and V_{EN1} pins select the LDO band (refer to LDO Select Truth Table). Only one LDO is enabled at a time, the non-enabled LDOs remain at 0V. If the LDO is used to drive a logic-level enable input on the PA, or in cases where there is an unused output, removal of the 1nF external capacitor is recommended.

The analog bias control feature consists of a buffer in parallel with a voltage summer. If $V_{CTRL\_IN}=1V$ to 2.4V then $V_{CTRL\_OUT}=V_{CTRL\_IN}$ (buffer mode). If $V_{CTRL\_IN}=0V$ then $V_{CTRL\_OUT}=VSET+1.14V$. This transfer function sets the required V_{CTRL_OUT} voltage based on the V_{OUT} (V_{SET}) voltage. The transfer function has been empirically determined to meet the PA requirements over all operating conditions (see RFMD RD6280_Ref_design spec for more details). If neither function is required, it is recommend to tie the V_{CTRL_IN} pin high to reduce current. No external capacitor is required on the V_{CTRL_OUT} pin.

The RF6280 is a 2mmx2mm WLCSP device. There is a 4x4 bump array with one bump removed in the center for the location of the bypass FET.

DC-DC Buck Converter

DC-DC buck converter operation involves the stepping down of a higher battery voltage to a lower output voltage by the alternate switching of a PFET and NFET pair through an external LC filter. The desired output voltage, together with the battery voltage, primarily determine the duty cycle of the PFET/NFET switching pair. This control methodology is called pulse width modulation (PWM). The actual duty cycle is also dependent on internal losses and load current requirement. The output voltage is monitored (feedback) through the V_{SENSE} pin (voltage mode control).

At a switching frequency of 2.5MHz (typ), the PFET is automatically enabled every 400ns. The pulse width (or time when the PFET is disabled and the NFET is enabled) is continuously variable from 0% to 100% duty cycle. The PFET and NFET have been designed with non-overlapping control circuitry to prevent VBATT shoot-through current to ground.

In order to improve light load efficiencies the converter PFET/NFET pair has been appropriately sized and the switching frequency determined to optimize DC losses against AC switching losses in UMTS applications. Despite the optimization, the PFET/NFET pair remains capable of sourcing 650mA in both normal operating and bypass modes. In addition, FET segmentation and selective biasing have been employed to further enhance light load efficiencies.

Attention to the DC-DC buck converter transient performance (V_{OUT} from 600mV to 3.4V) has been addressed by appropriate selection of the error amplifier loop filter response and the external LC filter (L=1.5H and C=4.7F). In addition, the specific inductor has been selected to minimize area and thickness (2.5mmx2.0mmx1.0mm).

The control interface for the DC-DC buck converter involves the simultaneous operation of the V_{EN0}, V_{EN1}, and V_{SET} pins. The buck converter is enabled whenever V_{EN0} or V_{EN1} is enabled (see band select truth table). The buck converter is shutdown when $V_{EN0}=V_{EN1}=0V$. The analog V_{SET} pin determines the V_{OUT} voltage ($V_{OUT}=V_{SET}*2.5$). The L_{OUT} pin is the PFET/NFET pair switching output, the V_{SENSE} pin is the V_{OUT} feedback pin and the V_{PWR} (A3) and PGND pins are fully dedicated to the converter for the high switching currents.

There is also a bypass FET on this device. When bypass mode is automatically enabled (see Bypass Control Table) the bypass FET and the switching PFET are turned on at DC=100% to further reduce the dropout voltage across the FET and inductor. This feature is advantageous when the battery is low and nearly completely discharged. There is a fully dedicated V_{PWR} pin for the bypass FET (B3), however, it is recommended to short the V_{PWR} (A3) pad to the V_{PWR} (B3) pad to reduce bypass mode dropout mode further.

LDO Regulators

There are three identical V_{REF} LDO's on the RF6280, one for each PA in a tri-band UMTS phone application. The typical output voltage is 2.85V with a tolerance of +/-100mV over voltage, temperature, and process. Each regulator is capable of sourcing 10mA maximum, with typical source current of 5mA.

The LDO's have been optimized to supply 2.85V at a minimum $V_{BATT}=3.0V$. The startup time is 2µs with an external 1nF noise filter capacitor on the output which minimizes internally generated noise, and maximizes power supply rejection out to the DC-DC buck converter switching frequency. If the LDO is employed as a level-shifter, the external 1nF capacitor should be removed from the application.

The interface involves the simultaneous control of the V_{EN0} and V_{EN1} pins (see the LDO Select Truth Table). If a LDO is deselected, an internal pull-down with hold the output at 0V. This PMIC has three fully dedicated LDO output (V_{REFA}, V_{REFB}, and V_{REFC}). If a LDO is not used in the application, no external connection is required due to the internal pull-down.

Analog Bias Control

The analog bias control feature is designed to provide additional flexibility by either buffering the V_{CTRL} voltage or generating an automatic analog bias control voltage based on a previously empirically determined transfer function which relates the output voltage (V_{CTRL_OUT}) to V_{OUT}. This feature simplifies system design and reduces development time by eliminating the need to calibrate a software look-up table which correlates V_{CTRL_OUT} and V_{OUT}. In either mode, the driver is capable or sourcing or sinking 500µA.

The buffer is automatically enabled when V_{CTRL_IN}=1V to 2.4V. The auto analog bias control is automatically enabled when V_{CTRL_IN}=0V (see V_{CTRL} Table). If auto analog bias control is selected it is recommended to tie V_{CTRL_IN} low. In auto analog bias control mode V_{CTRL_OUT}=V_{SET}+1.14V. No external capacitance is required or expected on the V_{CTRL_OUT} pin.

The control interface for the analog bias control function involves the V_{CTRL_IN} pin, the V_{CTRL_OUT} pin, V_{EN0} and V_{EN1}, and the V_{SET} pin. Like the DC-DC buck converter, this feature is also enabled when V_{EN0} or V_{EN1} is enabled.

Shutdown
When V_{EN0} and V_{EN1} are both disabled, the device enters shutdown mode. In this mode, all features are disabled to minimize battery quiescent current (<0.1mA). From shutdown mode, the PMIC takes typically 2µs to start-up the internal circuitry.

Over Temperature Protection
An internal over temperature shutdown circuit is employed to protect the device from excessively high junction temperatures. The shutdown occurs at typically 140°C and will re-enable when the temperature drops by typically 20°C. The over temperature shutdown only effects the operation of the DC-DC buck converter.

LC Filter
The LC filter values were specifically selected to balance efficiency over the load current operating range and transient performance while minimizing board area. Inductors and capacitors of different values may be used at risk to converter stability and performance. Inductors of the same value, other than the recommended, may adversely affect the light load efficiency and dropout voltage of the system.

Board Layout
It is strongly recommended to follow good DC-DC converter layout practices in this application to reduce radiated and conducted system noise. Placement of C1 is critical and must be such to minimize the AC supply and ground return current loop through the PFET. In addition, the placements of the LC filter are also critical to minimize the AC supply and ground return current loop through the NFET.

PCB Design Requirements

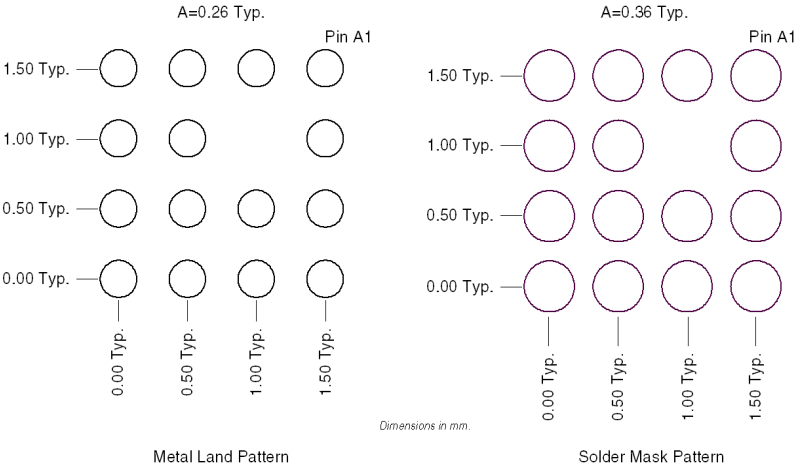
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3 u-inch to 8 u-inch gold over 180 u-inch nickel.

PCB Land Pattern Recommendation *

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern



Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2 mil to 3 mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.