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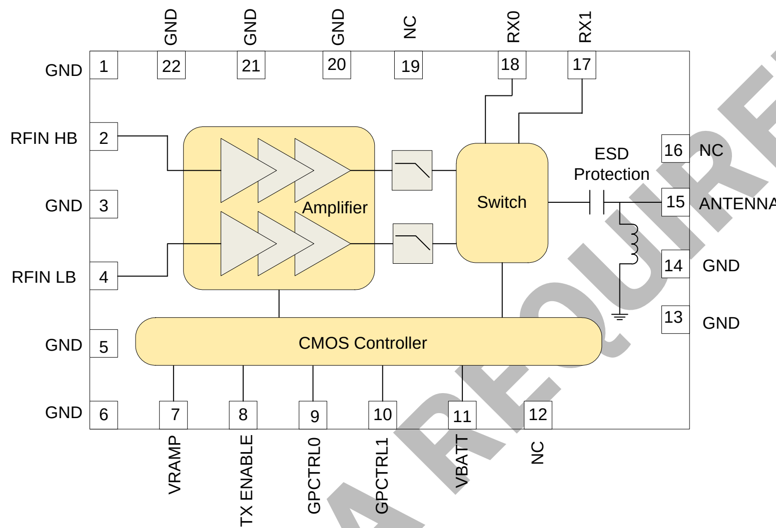
Proposed

RF7182D

DUAL-BAND TX, DUAL-BAND RX GSM, GPRS TRANSMIT MODULE

Package Style: Module 6.63mmx5.24mmx1.0mm



Functional Block Diagram

Features

- 8kV Robust ESD Protection at Antenna Port
- Enhanced Performance Transmit Module
- No External Routing
- High Efficiency at rated P_{OUT}
  V_{BATT}=3.5V
  EGSM900 40%
  DCS1800 36%
- Low RX Insertion Loss
- Symmetrical RX Ports
- 0dBm to 6dBm Drive Level, >50dB of Dynamic Range
- Integrated Power Flattening Circuit

Applications

- 3V Dual-Band GSM/GPRS Handsets
- EGSM900/DCS1800 Products
- GPRS Class 12 Compliant
- Portable Battery-Powered Equipment

Product Description

The RF7182D is a dual band (EGSM900/DCS1800) GSM/GPRS Class 12 compliant transmit module with two symmetrical receive ports. This transmit module builds upon RFMD's leading power amplifier with PowerStar® integrated power control technology, pHEMT switch technology, and integrated transmit filtering for best-in-class harmonic performance. The results are high performance, a reduced solution size, and ease of implementation. The device is designed for use as the final portion of the transmitter section in a GSM900/DCS1800 handset and eliminates the need for PA-to-antenna switch module matching network.

The RF7182D features RFMD's latest integrated power-flattening circuit, which significantly reduces current and power variation into load mismatch. The RF7182D also integrates an ESD filter to provide excellent ESD protection at the antenna port. The RF7182D is designed to provide maximum efficiency at rated P_{OUT}.

RF7182D	Dual-Band TX, Dual-Band RX GSM, GPRS Transmit Module
RF7182DSB	Transmit Module 5-Piece Sample Pack
RF7182DPCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.3 to +6.0	V
Power Control Voltage (V_{RAMP})	-0.3 to +1.8	V
Input RF Power	+10	dBm
Max Duty Cycle	50	%
Output Load VSWR	20:1	
Operating Temperature	-30 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
ESD					
ESD RF Ports			1000	V	HBM, JESD22-A114
			1000	V	CDM, JED22-A114
ESD Antenna Port			8	KV	IEC, 61000-4-2
ESD Any Other Port			1000	V	HBM, JESD22-A114
			1000	V	CDM, JEDEC, JESD22-C101
Overall Power Control V_{RAMP}					
Power Control "ON"			1.8	V	Max. P_{OUT}
Power Control "OFF"		0.25		V	Min. P_{OUT}
V_{RAMP} Input Capacitance		15	20	pF	DC to 200kHz
V_{RAMP} Input Current			10	μA	$V_{RAMP}=V_{RAMP\ MAX}$
Power Control Range		50		dB	V_{RAMP}=0.25V to $V_{RAMP\ MAX}$
Overall Power Supply					
Power Supply Voltage	3.1	3.5	4.8	V	Operating Limits
Power Supply Current			10	μA	P_{IN}<-30dBm, TX Enable=Low, V_{RAMP}=0.25V, Temp=-20°C to +85°C, V_{BATT}=4.8V, GpCtrl0, GpCtrl=Low
Overall Control Signals					
GpCtrl0, GpCtrl1 "Low"	0	0	0.5	V	
GpCtrl0, GpCtrl1 "High"	1.25	2.0	V_{BATT}	V	
GpCtrl0, GpCtrl1 "High Current"		1	2	uA	
TX Enable "Low"	0	0	0.5	V	
TX Enable "High"	1.25	2.0	V_{BATT}	V	
TX Enable "High Current"		1	2	uA	
RF Port Input and Output Impedance		50		Ω	

TX ENABLE	GpCtrl1	GpCtrl0	TX Module Mode
0	0	0	Low Power Mode (Stand-by)
0	1	0	RX 0
0	1	1	RX 1
1	1	0	GSM900 TX Mode
1	1	1	DCS1800 TX Mode

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
EGSM900 Band					Nominal conditions unless otherwise stated. All unused ports are terminated. V_{BATT}=3.5V, P_{IN}=3dBm, Temp=+25°C, TX Enable=High, VRAMP=1.8V. TX Mode: GpCtrl1=High, GpCtrl0=Low, Duty Cycle=25%, Pulse Width=1154µS
Operating Frequency Range	880		915	MHz	
Input Power	0	3	6	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		2:1	2.5:1		Over P_{OUT} range (5dBm to 33dBm).
Maximum Output Power	33	33.9	36	dBm	Nominal conditions.
	31	34	37	dBm	V_{BATT}=3.1V to 4.8V, P_{IN}=0dBm to 6dBm, Temp=-20°C to +85°C, Duty Cycle=50%, Pulse Width=2308mS, $V_{RAMP}\leq$1.8V.
Minimum Power Into 3:1 VSWR	30	31.5		dBm	The measured delivered output power to the load with the mismatch loss already taken into account with 1dB variation margin.
Efficiency	36	40		%	Set V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=33dBm
2nd Harmonic		-40*	-33	dBm	V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=33dBm. *Typical value measured from worst case harmonic frequency across the band.
3rd Harmonic		-40*	-33	dBm	V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=33dBm. *Typical value measured from worst case harmonic frequency across the band.
All other harmonics up to 12.75GHz		-40	-33	dBm	V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=33dBm.
Non-harmonic Spurious up to 12.75GHz			-36	dBm	V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=33dBm, also over all power levels (5dBm to 33dBm).
Forward Isolation 1		-57	-41	dBm	TX Enable Low, P_{IN}=6dBm, V_{RAMP}=0.25V.
Forward Isolation 2		-27	-15	dBm	TX Enable High, P_{IN}=6dBm, V_{RAMP}=0.25V.
Output Noise Power		-81	-77	dBm	925MHz to 935MHz. V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=33dBm, RBW=100kHz.
		-85	-83	dBm	935MHz to 960MHz. V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=33dBm, RBW=100kHz.
		-117	-87	dBm	1805MHz to 1880MHz. V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=33dBm, RBW=100kHz.
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=12:1, all phase angles (Set $V_{RAMP=VRAMP\ RATED}$ for $P_{OUT}\leq$33dBm into 50Ω load; load switched to VSWR=12:1).
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=20:1, all phase angles (Set $V_{RAMP=VRAMP\ RATED}$ for $P_{OUT}\leq$33dBm into 50Ω load; load switched to VSWR=20:1).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS1800 Band					Nominal conditions unless otherwise stated. All unused ports are terminated. V_{BATT}=3.5V, P_{IN}=3dBm, Temp=+25°C, TX Enable=High, VRAMP=1.8V. TX Mode: GpCtrl1=High, GpCtrl0=High, Duty Cycle=25%, Pulse Width=1154µS
Operating Frequency Range	1710		1785	MHz	
Input Power	0	3	6	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		1.5:1	2.5:1		Over P_{OUT} range (0dBm to 30dBm).
Maximum Output Power	30	31.5	33	dBm	Nominal conditions.
	28	31.7	35	dBm	V_{BATT}=3.0V to 4.8V, P_{IN}=0dBm to 6dBm, Temp=-20°C to +85°C, Duty Cycle=50%, Pulse Width=2308mS, $V_{RAMP}\leq$1.8V.
Minimum Power Into 3:1 VSWR	27	28.7		dBm	The measured delivered output power to the load with the mismatch loss already taken into account with 1dB variation margin.
Efficiency	31	36		%	Set V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=30dBm
2nd Harmonic		-40*	-33	dBm	V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=30dBm. *Typical value measured from worst case harmonic frequency across the band.
3rd Harmonic		-40*	-33	dBm	V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=30dBm. *Typical value measured from worst case harmonic frequency across the band.
All other harmonics up to 12.75GHz		-40	-33	dBm	V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=30dBm.
Non-harmonic Spurious up to 12.75GHz			-36	dBm	V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=30dBm, also over all power levels (0dBm to 30dBm).
Forward Isolation 1		-68	-53	dBm	TX Enable Low, P_{IN}=6dBm, V_{RAMP}=0.25V.
Forward Isolation 2		-33	-15	dBm	TX Enable High, P_{IN}=6dBm, V_{RAMP}=0.25V.
Output Noise Power		-98	-77	dBm	925MHz to 935MHz. V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=30dBm, RBW=100kHz.
		-97	-83	dBm	935MHz to 960MHz. V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=30dBm, RBW=100kHz.
		-86	-79	dBm	1805MHz to 1880MHz. V_{RAMP}=$V_{RAMP\ RATED}$ for P_{OUT}=30dBm, RBW=100kHz.
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=12:1, all phase angles (Set V_{RAMP}=$V_{RAMP\ RATED}$ for $P_{OUT}\leq$30dBm into 50Ω load; load switched to VSWR=12:1).
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=20:1, all phase angles (Set V_{RAMP}=$V_{RAMP\ RATED}$ for $P_{OUT}\leq$30dBm into 50Ω load; load switched to VSWR=20:1).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RX Section					Nominal conditions unless otherwise stated. V_{BATT}=3.5V, P_{IN}=-10dBm, Temp=+25°C, TX Enable=Low, V_{RAMP}=0.2V RX0 mode: GpCtrl1=High, GpCtrl0=Low RX1 mode: GpCtrl1=High, GpCtrl0=High RX Frequencies: EGSM900=925MHz to 960MHz DCS1800=1805MHz to 1880MHz
Insertion Loss EGSM900 ANT-RX0/ RX1		1.2	1.5	dB	See note 1.
In-Band Ripple EGSM900 ANT-RX0/RX1		0.1	0.2	dB	
Input VSWR EGSM900 ANT-RX0/RX1		1.5:1	1.7:1		
Insertion Loss DCS1800 ANT-RX0/RX1		1.4	1.7	dB	See note 1.
In-Band Ripple DCS1800 ANT-RX0/RX1		0.1	0.2	dB	
Input VSWR DCS1800 ANT-RX0/RX1		1.8:1	2.0:1		
TX Section					
Switch Leakage P_{OUT} at RX Port EGSM900 ANT-RX0/RX1		-1	6	dBm	EGSM900 TX mode: Freq=880MHz to 915MHz, GpCtrl1=High, GpCtrl0=Low, V_{RAMP}=V_{RAMP} rated for P_{OUT}=33dBm at antenna port. See Note 2.
Switch Leakage P_{OUT} at RX Port DCS1800 ANT-RX0/RX1		2	6	dBm	DCS1800 TX mode: Freq=1710MHz to 1785MHz, GpCtrl1=High, GpCtrl0=High, V_{RAMP}=$V_{RAMPRATED}$ for P_{OUT}=30dBm at antenna port. See Note 2.

Note:
1. Better performance can be obtained in the high band with optimized matching..
2. Isolation specification set to ensure at least the following isolation at rated power:
Calculation Example: Isolation=P_{OUT} @ Antenna-P_{OUT} @ RX Port. Isolation LB=33-(-1)=34dB, HB=30-(2)=28dB.

Pin	Function	Description
1	GND	Ground.
2	RFIN HB	RF input to the DCS1800 band. This is a 50Ω input.
3	GND	Ground.
4	RFIN LB	RF input to the EGSM900 band. This is a 50Ω input.
5	GND	Ground.
6	GND	Ground.
7	VRAMP	VRAMP ramping signal from DAC. A simple RC filter is integrated into the module. VRAMP may not require additional filtering depending on the baseband selected.
8	TX ENABLE	This signal enables the PA module for operation with a logic high. The switch is put in TX mode determined by GpCtrl0 and GpCtrl1.
9	GPCTRL0	Control pin that together with GpCtrl1 selects the band of operation.
10	GPCTRL1	Control pin that together with GpCtrl0 selects the band of operation.
11	VBATT	Power supply for the module. This should be connected to the battery terminal using as wide a trace as possible.
12	NC	No internal connection; may be grounded on PCB.
13	GND	Ground.
14	GND	Ground.
15	Antenna	Antenna port. This is a 50Ω output.
16	NC	No internal connection; may be grounded on PCB.
17	RX1	This port is interchangeable with any other RX port.
18	RX0	This port is interchangeable with any other RX port.
19	NC	No internal connection; may be grounded on PCB.
20	GND	Ground.
21	GND	Ground.
22	GND	Ground.
23	GND	Ground.

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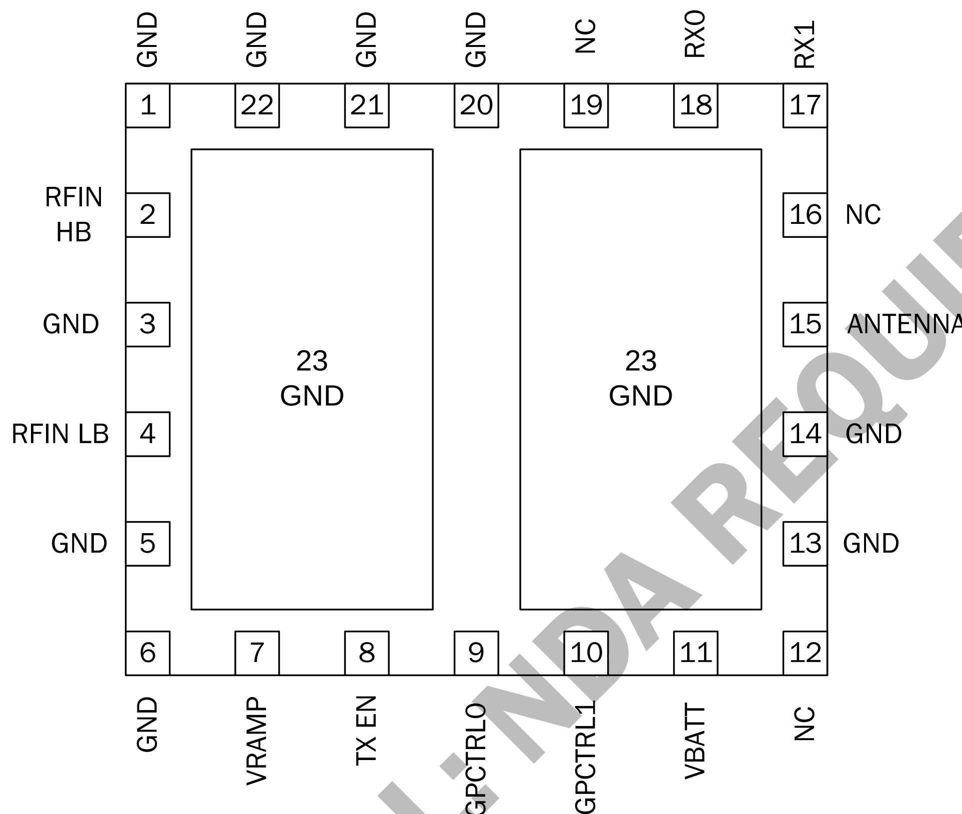
Pin Out

(Top View)



Theory of Operation

Product Description

The RF7182D is a dual-band, transmit module (TXM) with fully-integrated power control functionality, harmonic filtering, band selectivity, and TX/RX switching. The TXM is self-contained, having 50Ω I/O terminals and two symmetrical RX ports allowing dual-band operation. The power control function eliminates all power control circuitry, including directional couplers, diode detectors, and power control ASICs, etc. The power control capability provides 50dB of continuous control range and 70dB of total control range, using a DAC-compatible, analog voltage input. The TX Enable feature provides for PA activation (TX mode) or RX mode/standby. Internal switching provides a low-loss, low-distortion path from the antenna port to the TX path (or RX port), while maintaining proper isolation. Integrated filtering provides ETSI-compliant harmonic suppression at the antenna port even under high mismatch conditions, which is important as modern antennas often present a load that significantly deviates from nominal impedance.

Overview

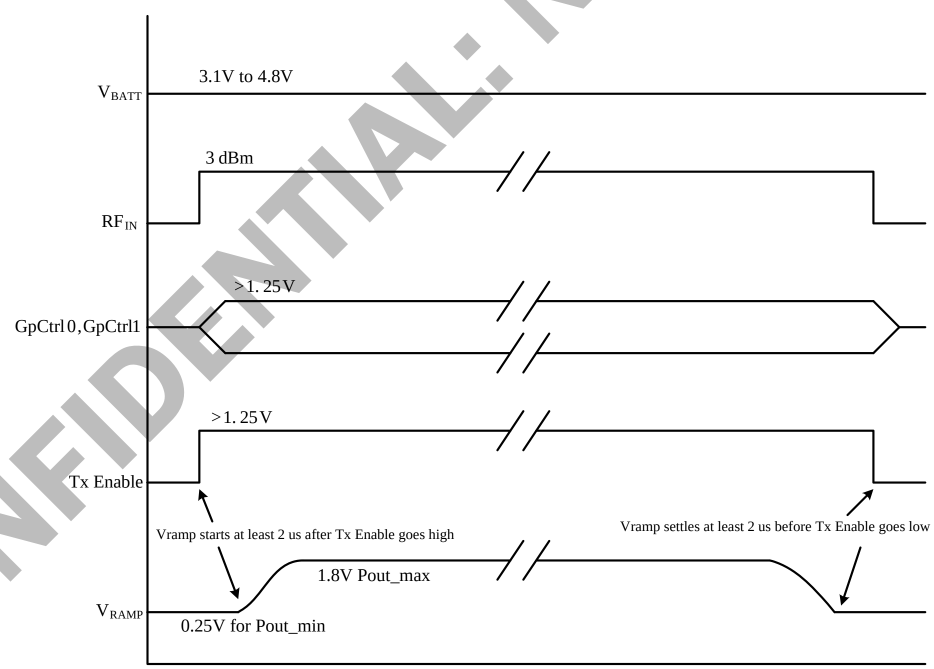
The RF7182D simplifies the phone design by eliminating the need for the complicated control loop, harmonic filters, and TX/RX switch along with their associated matching components. The power control loop can be driven directly from the DAC output in the baseband circuit. The module has two RX ports for EGSM900 and DCS1800 bands of operation. The two RX ports are symmetrical; they can be used either as EGSM900 or DCS1800. To control the mode of operation, there are three logic control signals: TX Enable, GpCtrl0, and GpCtrl1. The RF7182D offers high efficiency at the rated P_{OUT} as backed-off efficiency is improved in this TXM.

Power Ramping and Timing

The RF7182D should be powered-on according to the power-on sequence below. It is designed to prevent operation of the amplifier under conditions that could cause damage to the device or erratic operation.

There are some setup times associated with the control signals of the RF7182D. The most important of these is the settling time between TXEN going high and when VRAMP can begin to increase. This time is often referred to as the "pedestal." It is required so that the internal power control loop and bias circuitry can settle after being turned on. The RF7182D requires at least two seconds or two quarter-bit times for proper settling of the power control loop.

The power-down sequence is the reverse of the power-on sequence. As described in the figure below, VBATT is applied first to provide bias to the silicon control chip. Next, the RF drive is applied. Next, when TXEN is high the VRAMP signal is held at a constant 0.25V. Two seconds later, VRAMP begins to ramp up. The shape of VRAMP is important for maintaining the switching transients. The basic shape of the ramping function should be raised cosine to achieve best transient performance.



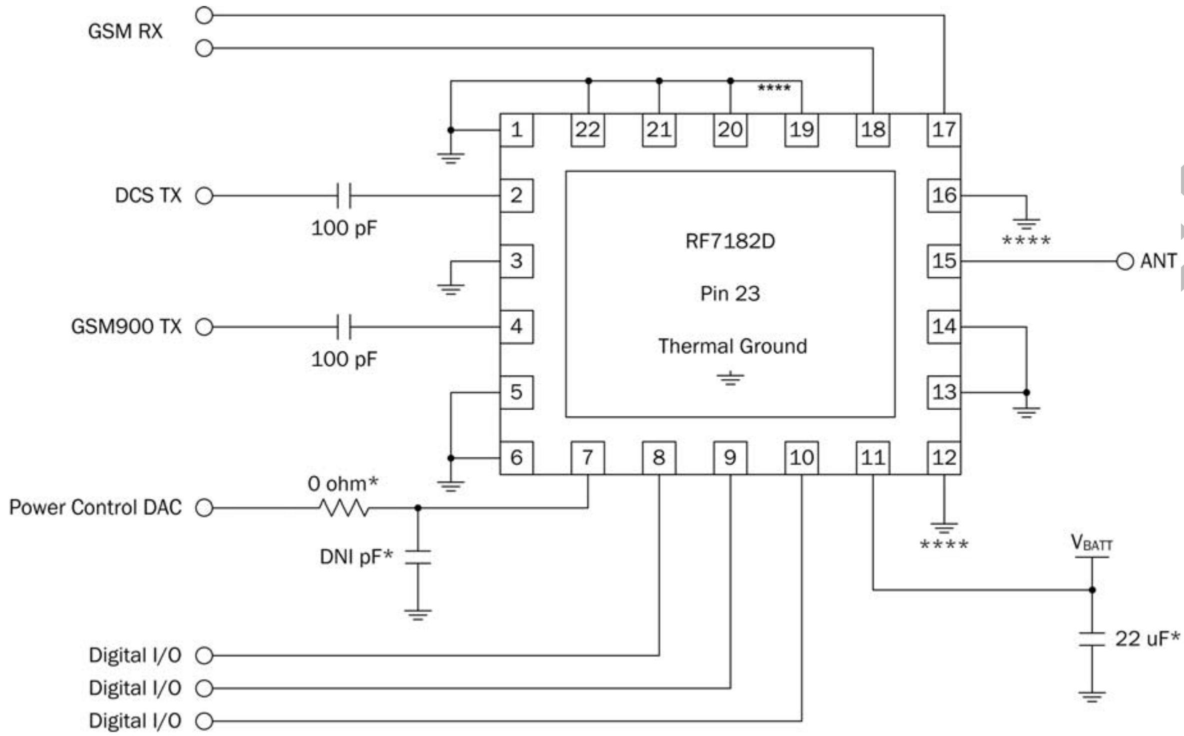
1. Apply V_{BATT}
2. Apply GpCtrl0, GpCtrl1, RFIN and TX Enable
3. Apply V_{RAMP} at least 2μs after TX Enable
4. The Power Down Sequence is in opposite order of the Power On Sequence

The RF7182D has an integrated power flattening circuit that reduces the amount of current variation when a mismatch is presented to the output of the PA. When a mismatch is presented to the output of the PA, its output impedance is varied and could present a load that will increase output power. As the output power increases, so does current consumption. The current consumption can become very high if not monitored and limited. The power flattening circuit is integrated onto the CMOS controller and requires no input from the user.

Into a mismatch, the current varies as the phase changes. The power flattening circuit monitors current through an internal sense resistor. As the current changes, the loop is adjusted in order to maintain current. The result is flatter power and reduced current into mismatch. The transeiver/baseband to regulate the ramping signal as the supply voltage decreases. The internal circuit monitors the supply voltage and adjusts the ramping signal such that the switching spectrum is minimally impacted.

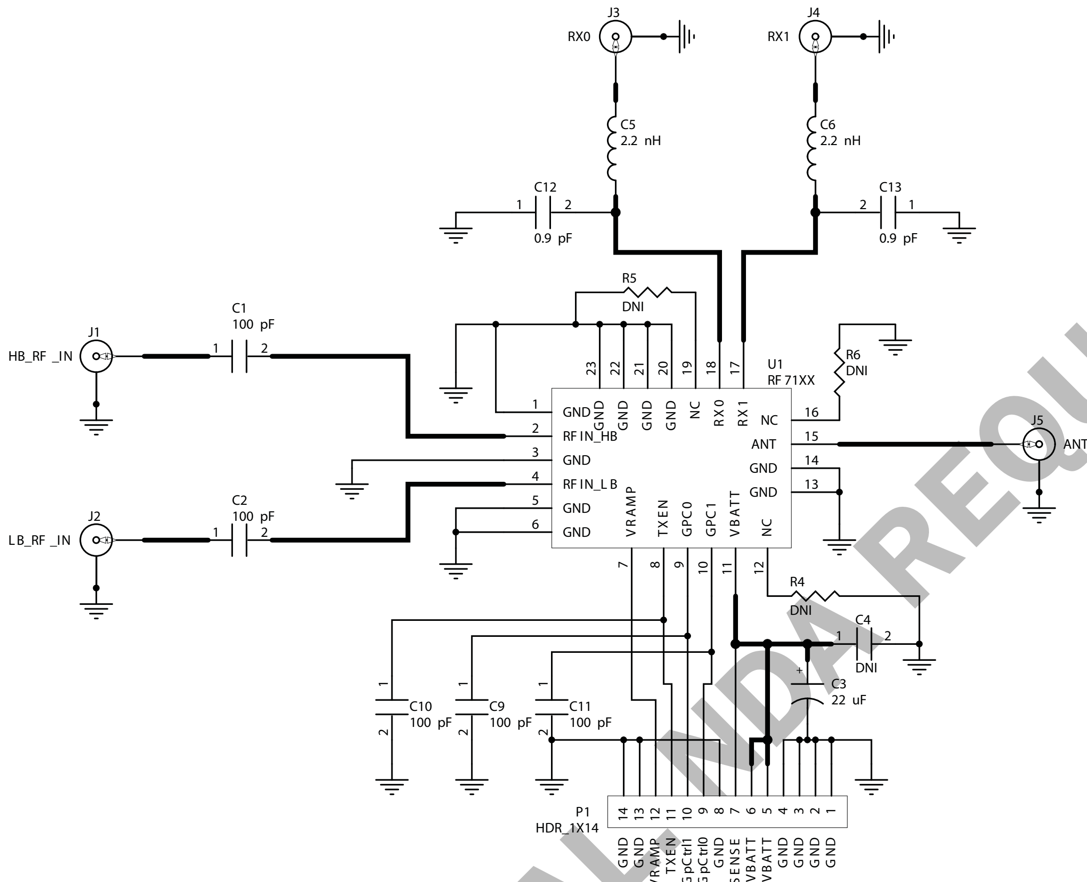
The RF7182D also incorporates a V_{BATT} tracking feature that eliminates the need for the transceiver/baseband to regulate the ramping signal as the supply voltage decreases. The internal circuit monitors the supply voltage and adjusts the ramping signal such that the switching spectrum is minimally impacted.

Application Schematic

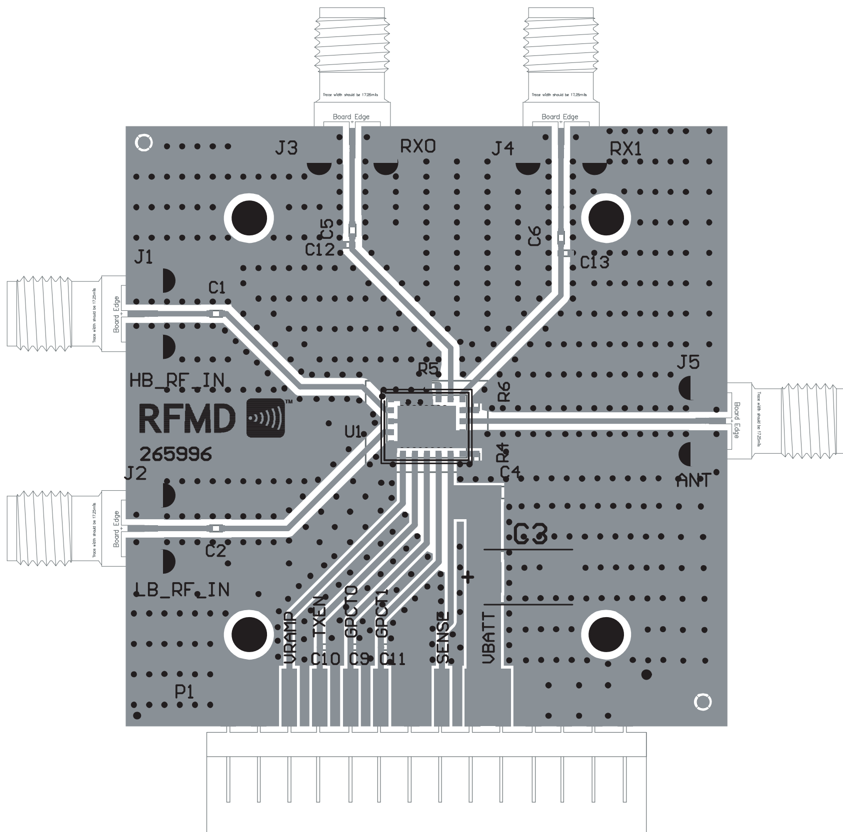


Notes:
* Suggested values only. Actual requirements will vary with application.
**All RF paths should be designed as 50 ohm microstrip or stripline.
***If a resistive attenuator network is used on the RF input to the power amplifier, it must be positioned on the transceiver side of the DC blocking capacitors (100 pF) to prevent adversely affecting amplifier biasing.
****NC pins on this module can be connected to ground.
*****RX0 and RX1 usually connect to SAW filters. A matching network may be used to provide a transformation from SAW impedance to RX port impedance.

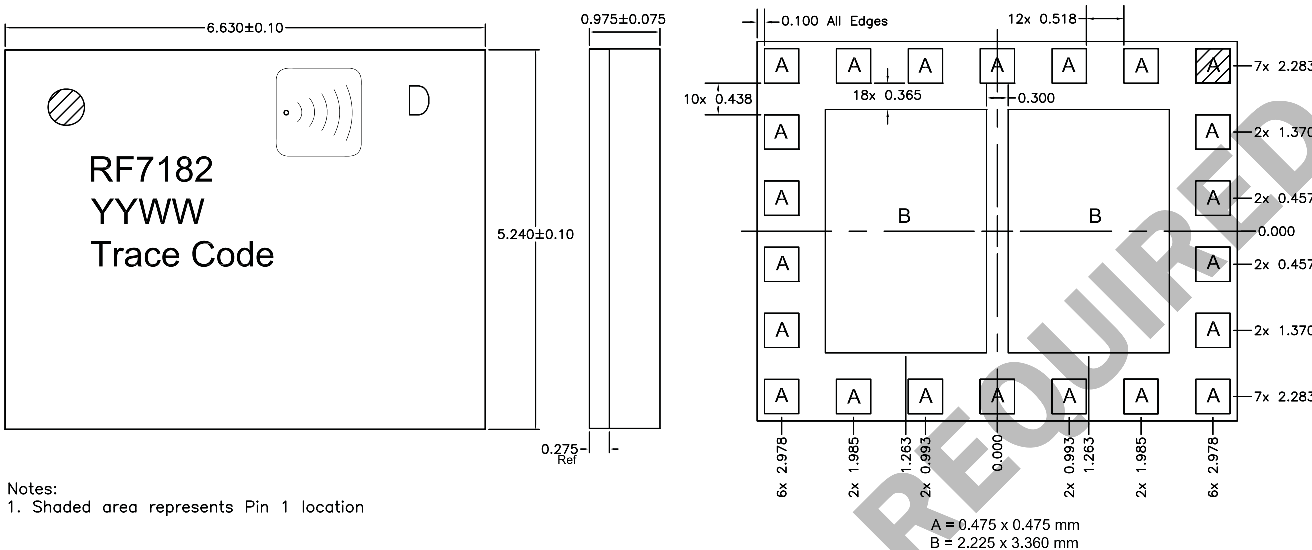
Evaluation Board Schematic



Evaluation Board Layout
Board Size 2.0" x 2.0"
Board Thickness 0.032", Board Material FR-4/Rogers, Multi-layer



Package Drawing



Notes:
1. Shaded area represents Pin 1 location.
2. All dimensions are TYP for reference only.
3. YY indicates year, WW indicates work week, and Trace Code is a sequential number assigned at devicce assembly.

PCB Design Requirements

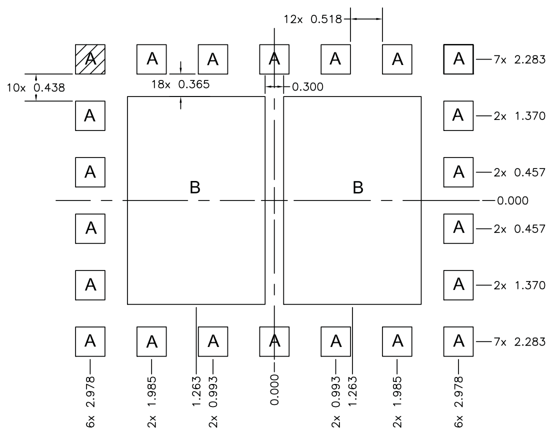
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3 μinch to 8 μinch gold over 180 μinch nickel.

PCB Land Pattern Recommendation

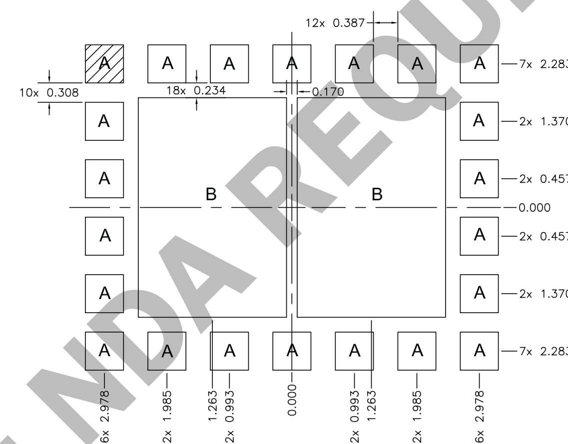
PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern



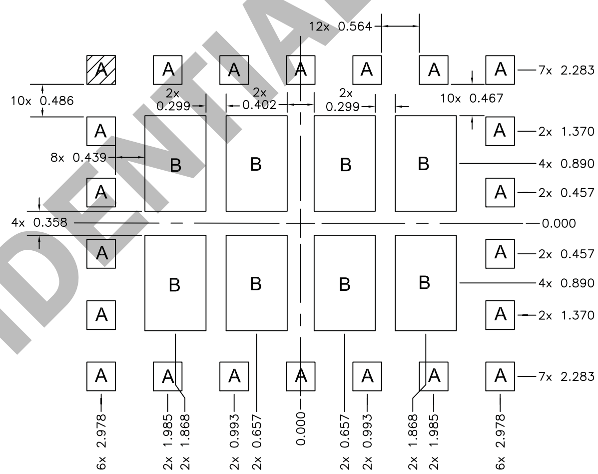
PCB METAL LAND PATTERN

A = 0.475 x 0.475 mm
B = 2.225 x 3.360 mm



PCB SOLDER MASK PATTERN

A = 0.605 x 0.605 mm
B = 2.355 x 3.490 mm



PCB STENCIL PATTERN

A = 0.428 x 0.428 mm
B = 0.912 x 1.422 mm

Notes:
1. Shaded area represents Pin 1 location.
2. All dimensions are TYP for reference only.

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Tape and Reel

Carrier tape basic dimensions are based on EIA 481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330mm (13 inches) in diameter or 178mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with the appropriate units of desiccant and a humidity indicator card, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, of Joint Industry Standard IPC/JEDEC J-STD-033.

The table below provides information for carrier tape and reels used for shipping the devices described in this document.

Tape and Reel

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF7182DTR13	13 (330)	4 (102)	12	8	Single	2500
RF7182DTR7	7 (178)	2.4 (61)	12	8	Single	750

Unless otherwise specified, all dimension tolerances per EIA-481.

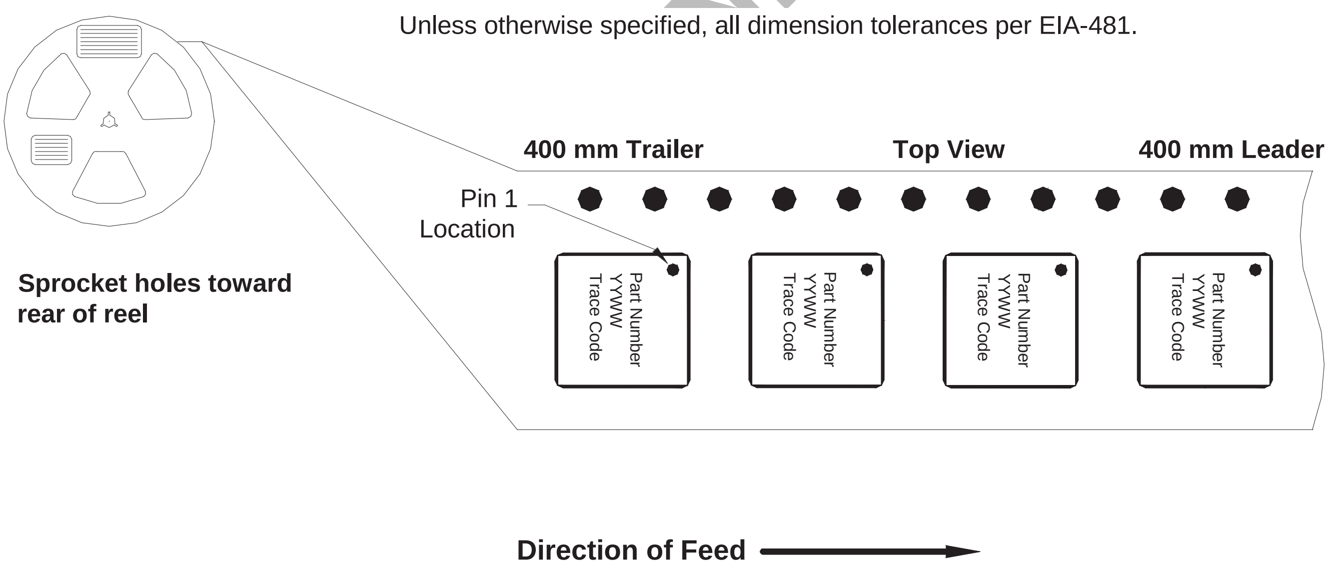

Figure 1. 5.24mmx6.63mm (Carrier Tape Drawing with Part Orientation)

RoHS* Banned Material Content

RoHS Compliant:	Yes
Package total weight in grams (g):	0.121
Compliance Date Code:	-
Bill of Materials Revision:	-
Pb Free Category:	e4

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Lead Frame	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted above.

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

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