Data Sheet September 2013

N-Channel Logic Level Power MOSFET 60V, 11A, 107 mΩ

These N-Channel enhancement-mode power MOSFETs are manufactured using the latest manufacturing process technology. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49158.

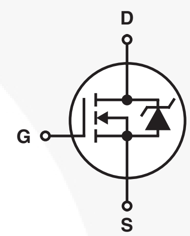
Ordering Information

PART NUMBER	PACKAGE	BRAND
RFD3055LE	TO-251AA	F3055L
RFD3055LESM9A	TO-252AA	F3055L

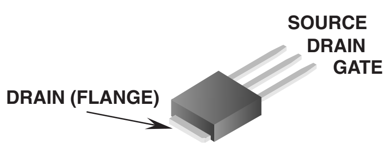
Features

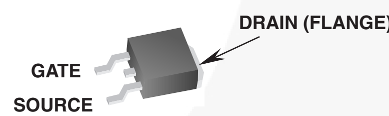
- 11A, 60V
- $r_{DS(ON)} = 0.107\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging





Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFD3055LE, RFD3055LESM9A	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±16	V
Continuous Drain Current	I_D	11	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	38	W
Derate Above 25^oC		0.25	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	3	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 55V$, $V_{GS} = 0V$		-	-	1	μA
		$V_{DS} = 50V$, $V_{GS} = 0V$, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm16V$		-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 8A$, $V_{GS} = 5V$ (Figure 11)		-	-	0.107	Ω
Turn-On Time	t_{ON}	$V_{DD} \approx 30V$, $I_D = 8A$, $V_{GS} = 4.5V$, $R_{GS} = 32\Omega$ (Figures 10, 18, 19)		-	-	170	ns
Turn-On Delay Time	$t_{d(ON)}$			-	8	-	ns
Rise Time	t_r			-	105	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	22	-	ns
Fall Time	t_f			-	39	-	ns
Turn-Off Time	t_{OFF}			-	-	92	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to 10V	$V_{DD} = 30V$, $I_D = 8A$, $I_{g(REF)} = 1.0mA$ (Figures 20, 21)	-	9.4	11.3	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0V$ to 5V		-	5.2	6.2	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to 1V		-	0.36	0.43	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz (Figure 14)		-	350	-	pF
Output Capacitance	C_{OSS}			-	105	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	23	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.94	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220AB		-	-	62	$^oC/W$
		TO-251AA, TO-252AA		-	-	100	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 8A$		-	1.25	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 8A$, $dI_{SD}/dt = 100A/\mu s$		-	66	ns

NOTES:

2. Pulse Test: Pulse Width ≤ 300ms, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse Width limited by max junction temperature. See Transient Thermal Impedance Curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves Unless Otherwise Specified

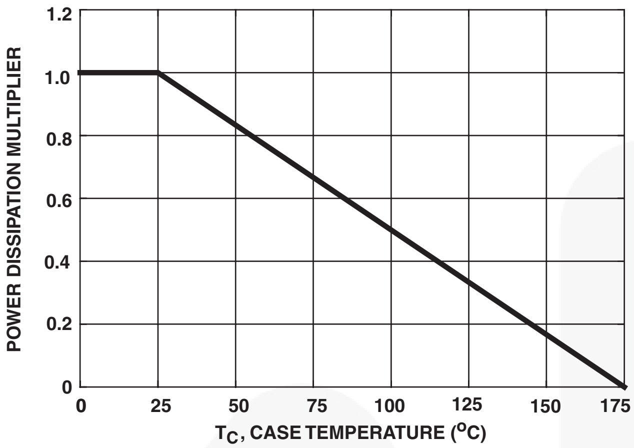


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

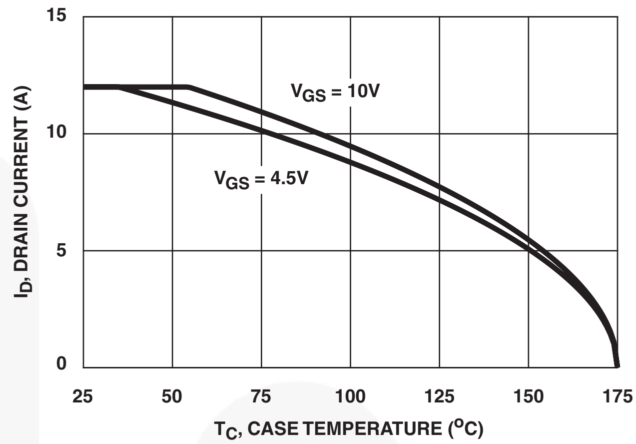


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

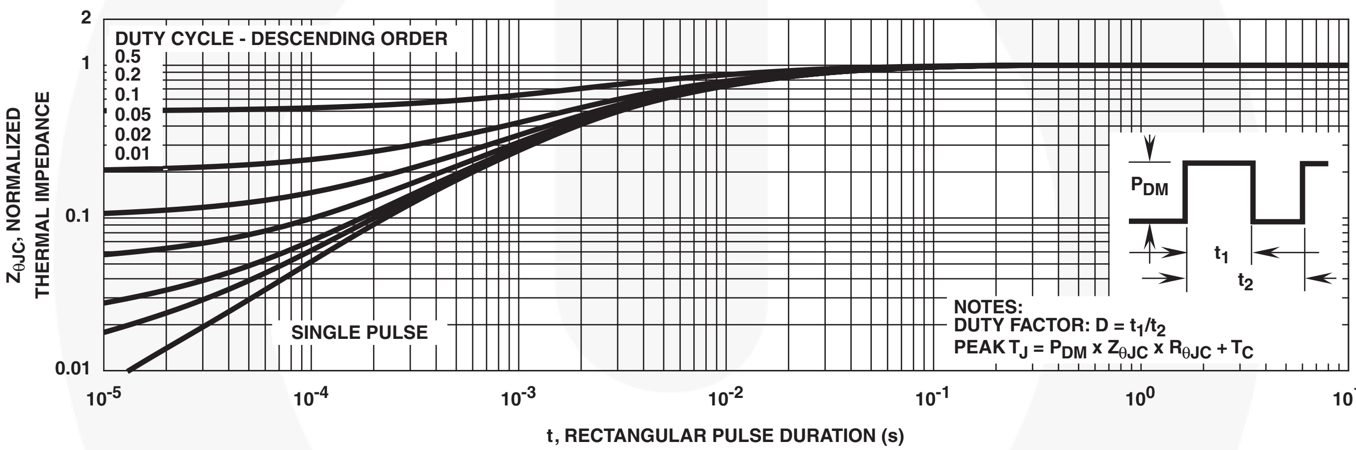


FIGURE 3. NORMALIZED TRANSIENT THERMAL IMPEDANCE

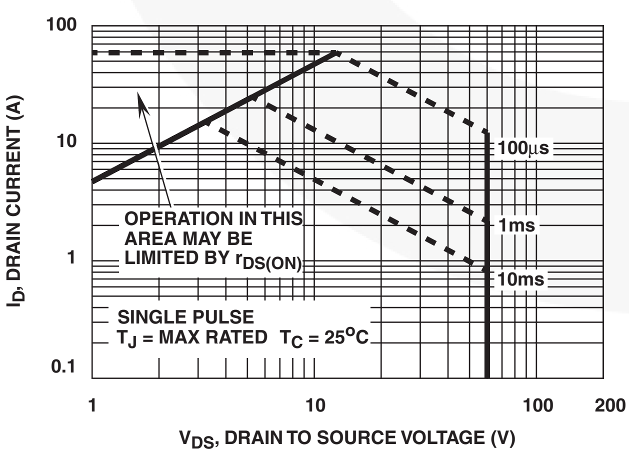


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

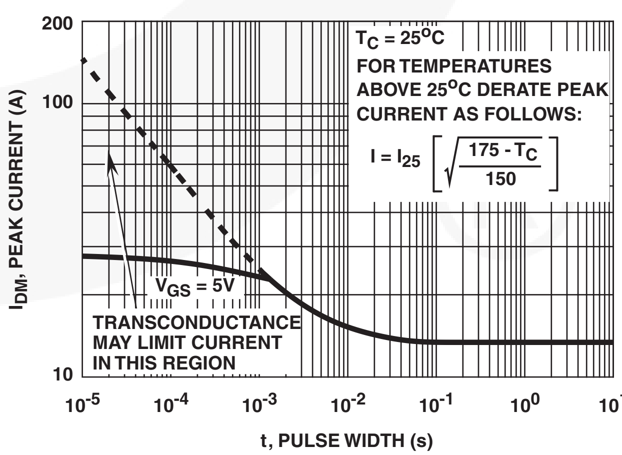
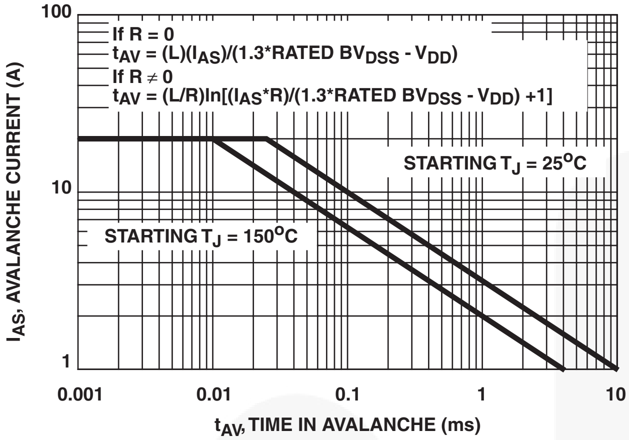


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified **(Continued)**



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

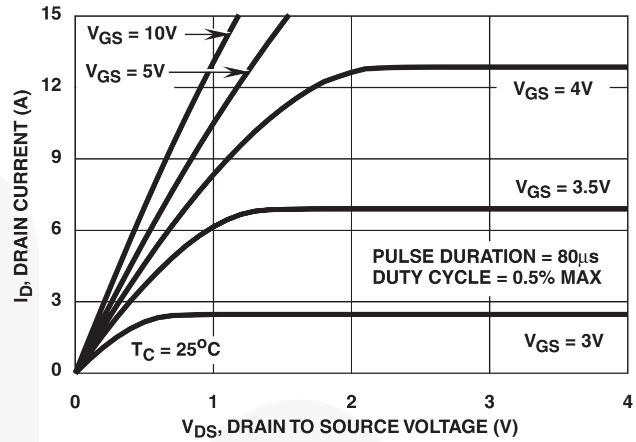


FIGURE 7. SATURATION CHARACTERISTICS

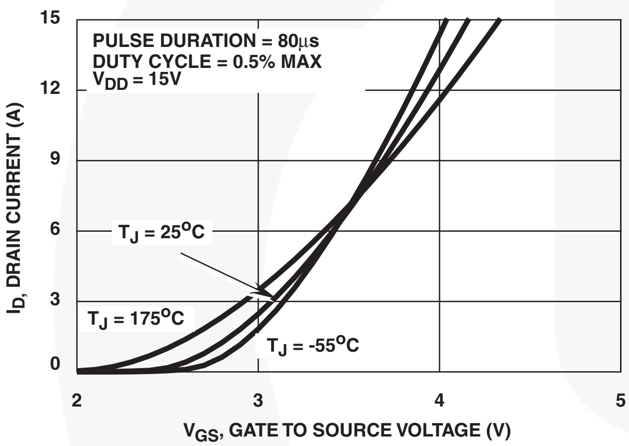


FIGURE 8. TRANSFER CHARACTERISTICS

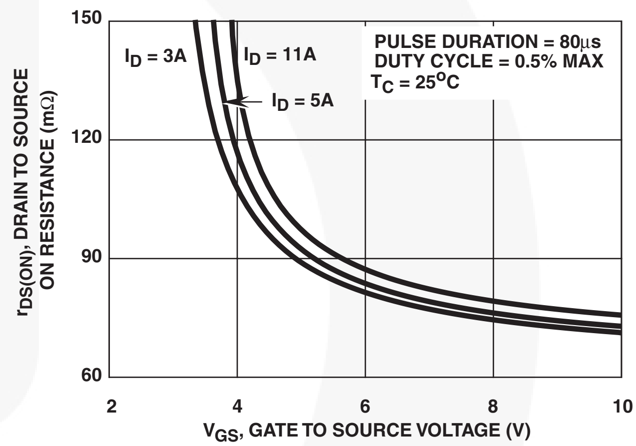


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

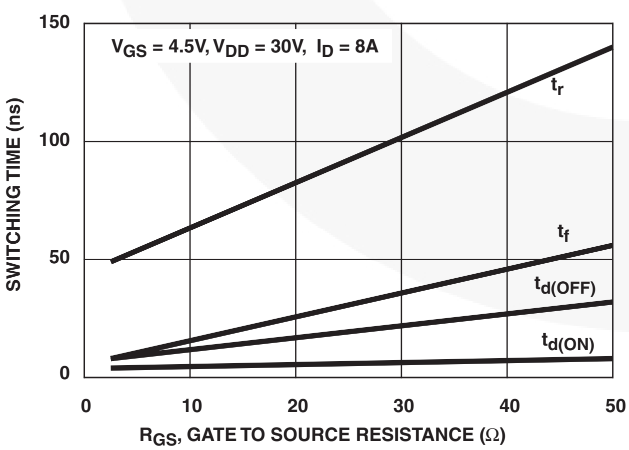


FIGURE 10. SWITCHING TIME vs GATE RESISTANCE

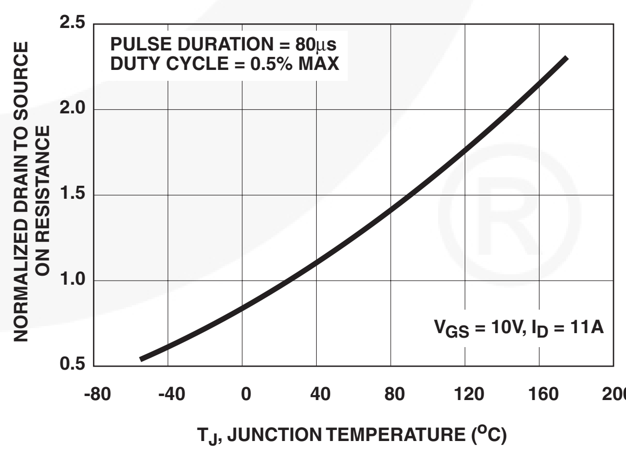


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

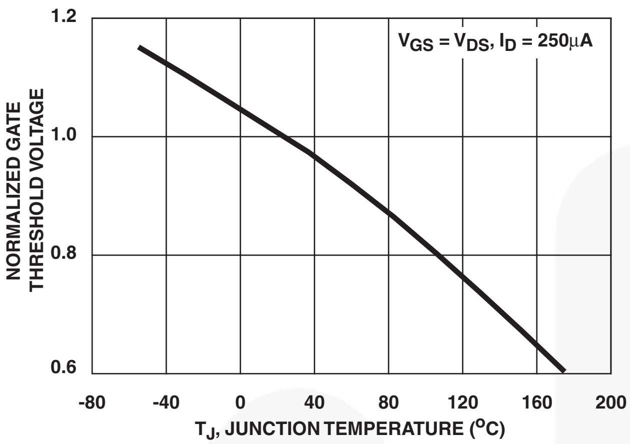


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

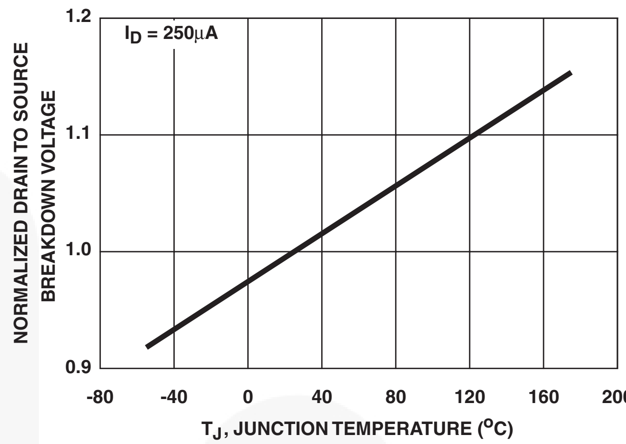


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

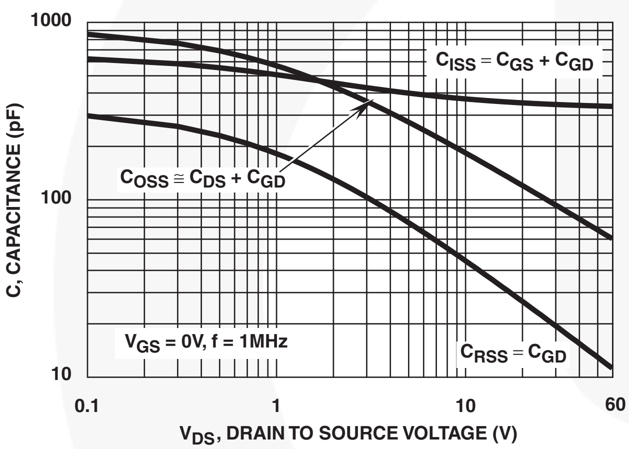
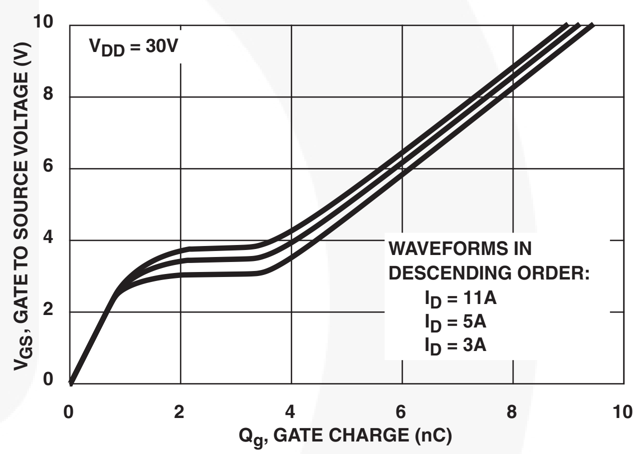


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

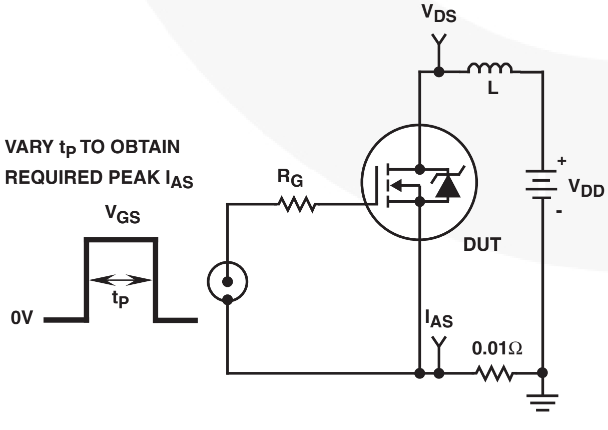


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

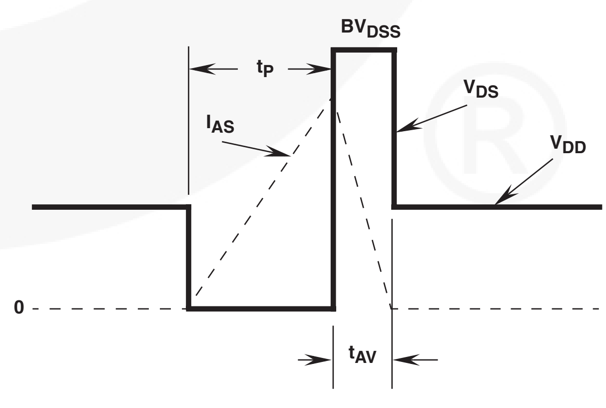


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

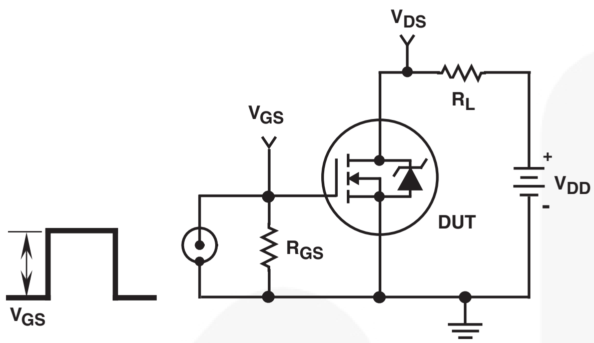


FIGURE 18. SWITCHING TEST CIRCUIT

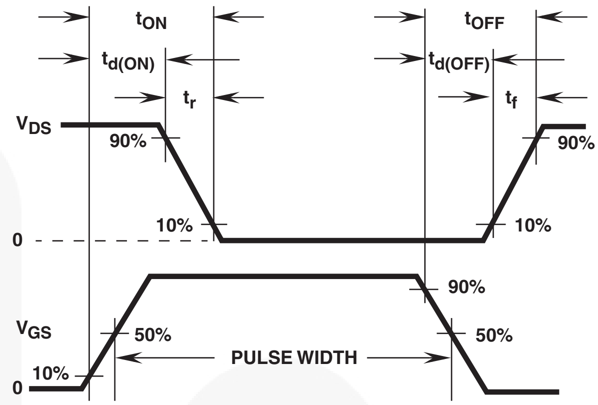


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

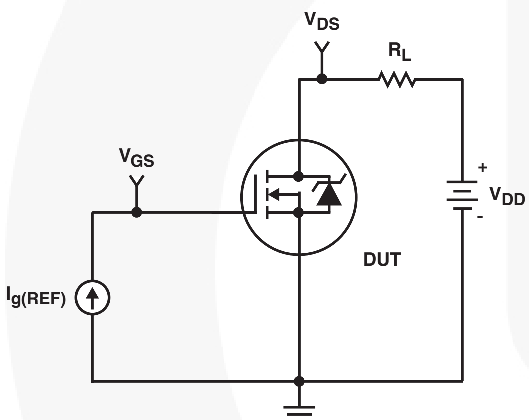


FIGURE 20. GATE CHARGE TEST CIRCUIT

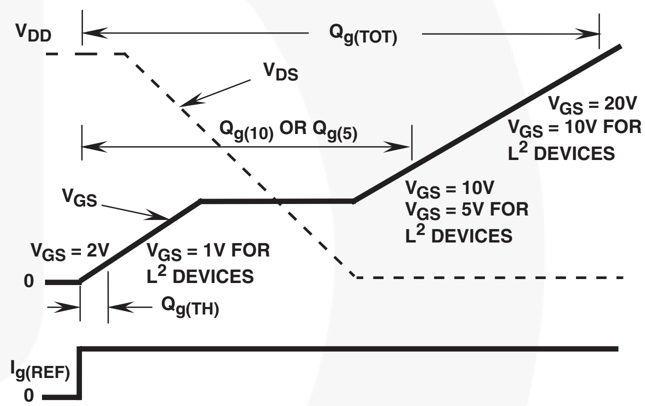
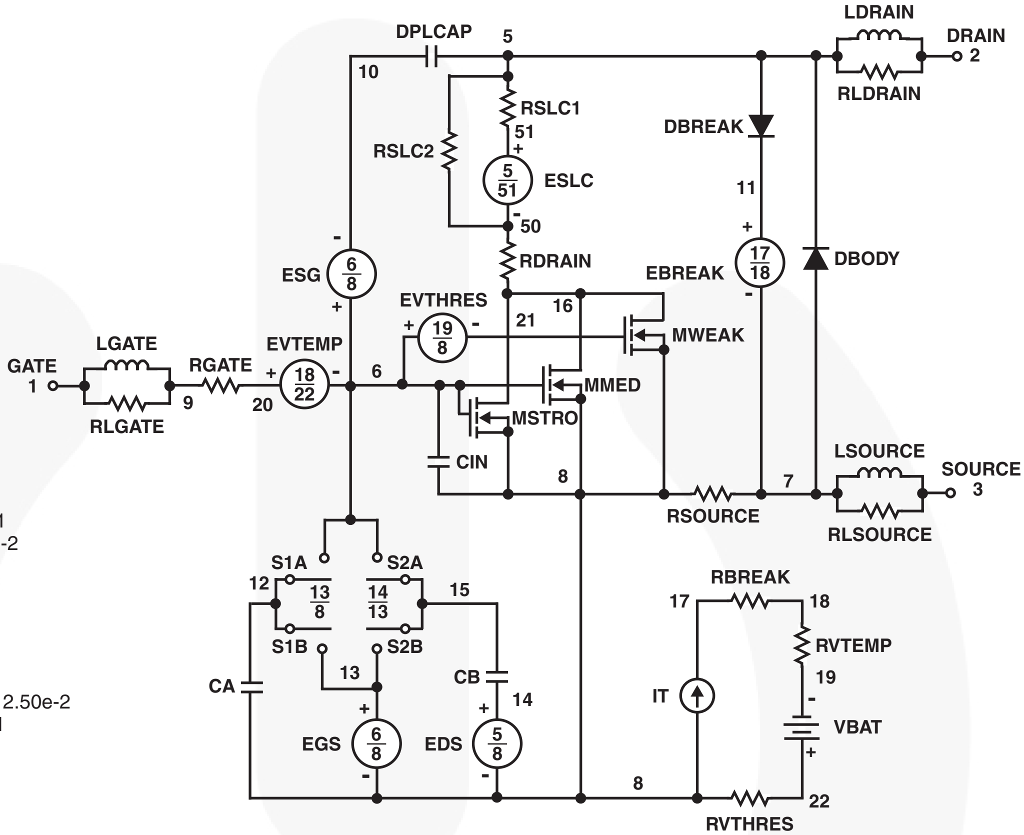


FIGURE 21. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

```
.SUBCKT RFD3055LE  2 1 3 ;       rev 1/30/95

CA  12  8 3.9e-9
CB  15  14 4.9e-9
CIN  6  8 3.25e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 67.8
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 1.0e-9
LGATE 1  9 5.42e-9
LSOURCE  3  7 2.57e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 3.7e-2
RGATE  9  20 3.37
RLDRAIN 2 5 10
RLGATE 1 9 54.2
RLSOURCE 3 7 25.7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 2.50e-2
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*30),3))}

.MODEL DBODYMOD D (IS = 1.75e-13  RS = 1.75e-2  TRS1 = 1e-4  TRS2 = 5e-6  CJO = 5.9e-10  TT = 5.45e-8 N = 1.03 M = 0.6)
.MODEL DBREAKMOD D (RS = 6.50e-1  TRS1 = 1.25e-4  TRS2 = 1.34e-6)
.MODEL DPLCAPMOD D (CJO = 3.21e-10  IS = 1e-30  N = 10 M = 0.81)
.MODEL MMEDMOD NMOS (VTO = 2.02 KP = .83 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.37)
.MODEL MSTROMOD NMOS (VTO = 2.39 KP = 14 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.78 KP = 0.02 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 33.7 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.06e-3  TC2 = 0)
.MODEL RDRAINMOD RES (TC1 = 1.23e-2  TC2 = 2.58e-5)
.MODEL RSLCMOD RES (TC1 = 0 TC2 = 0)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.19e-3 TC2 = -4.97e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.6e-3  TC2 = 1e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4  VOFF= -2.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.5  VOFF= -4)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -0.5  VOFF= 0)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 0  VOFF= -0.5)

.ENDS
```



For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66

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Email: orderlit@onsemi.com

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