HARRIS Semiconductor

RFM10N45, RFM10N50

10A, 450V and 500V, 0.600 Ohm, N-Channel Power MOSFETs

September 1998

Features

- **10A, 450V and 500V**
- **$r_{DS(ON)}$ = 0.600Ω**

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFM10N45	TO-204AA	RFM10N45
RFM10N50	TO-204AA	RFM10N50

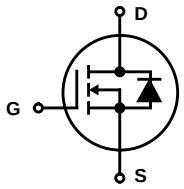
NOTE: When ordering, include the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

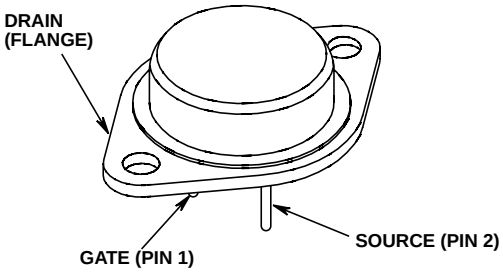
Formerly developmental type TA17435.

Symbol



Packaging

JEDEC TO-204AA



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **1788.1**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFM10N45	RFM10N50	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	450	500	V
Drain to Gate Voltage (R_{GS} = 1MΩ) (Note 1)	V_{DGR}	450	500	V
Continuous Drain Current	I_D	10	10	A
Pulsed Drain Current (Note 3)	I_{DM}	20	20	A
Gate to Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	^{o}C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	260	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFM10N45	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	450	-	-	V
RFM10M50			500	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA, (Figure 8)	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A, (Figures 6, 7)	-	-	0.600	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	V_{GS} = 10V, I_D = 10A			6.0	V
Turn-On Delay Time	$t_{d(ON)}$	V_{DS} = 250, $I_D \approx$ 5A, V_{GS} = 10V, R_G = 50Ω, R_L = 50Ω, (Figures 10, 11, 12)	-	26	60	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	525	900	ns
Fall Time	t_f		-	105	180	ns
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz, (Figure 9)	-	-	3000	pF
Output Capacitance	C_{OSS}		-	-	600	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	200	pF
Thermal Impedance Junction to Case	$R_{\theta JC}$		-	-	0.83	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 5A	-	-	1.4	V
Reverse Recovery Time	t_{rr}	I_{SD} = 4A, dI_{SD}/dt = 100A/μs	-	950	-	ns

NOTE:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

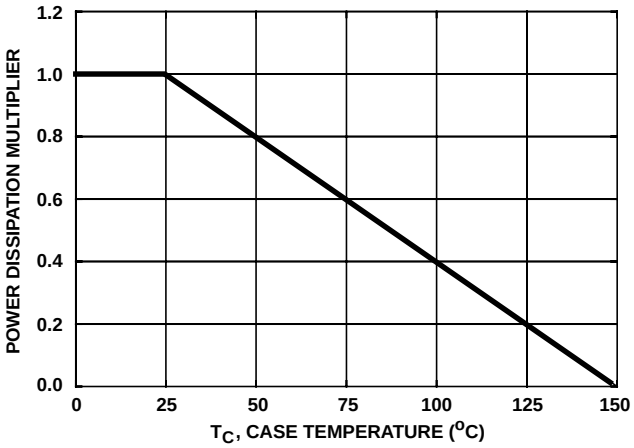


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

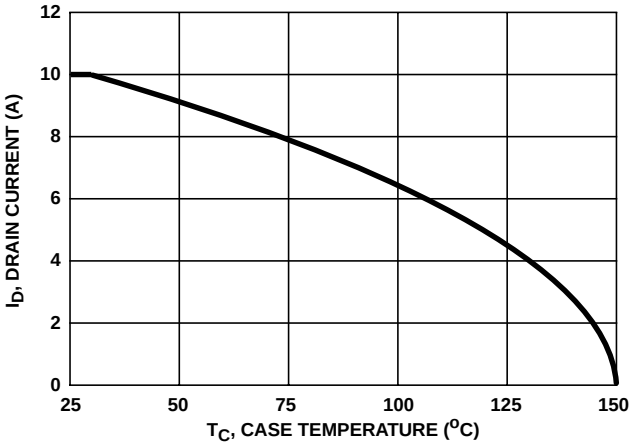


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

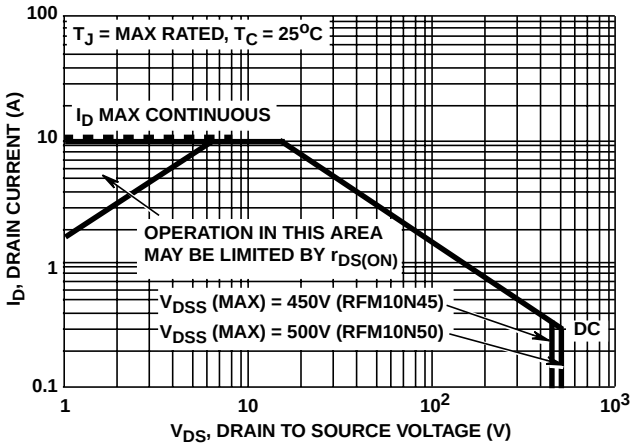


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

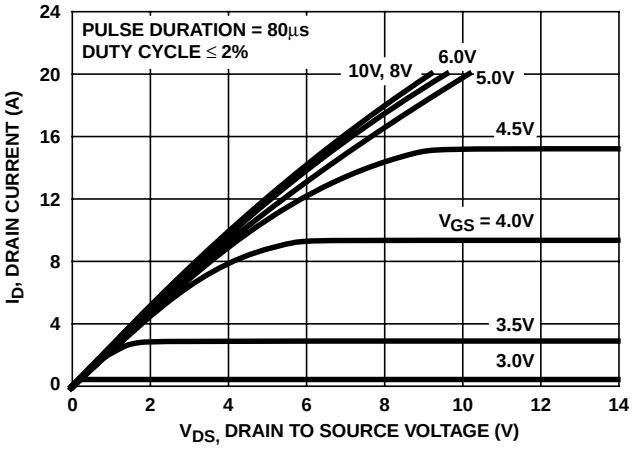


FIGURE 4. SATURATION CHARACTERISTICS

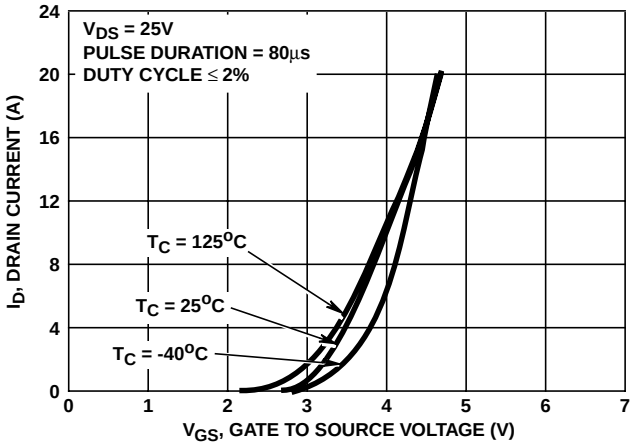


FIGURE 5. TRANSFER CHARACTERISTICS

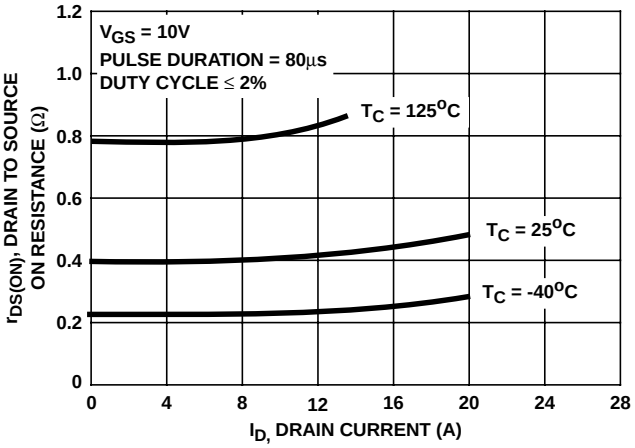


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

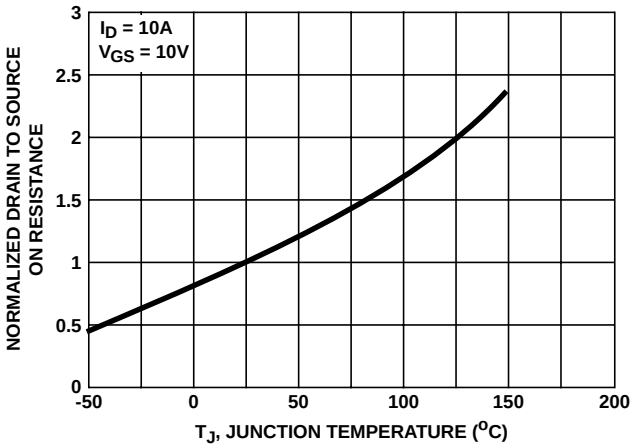


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

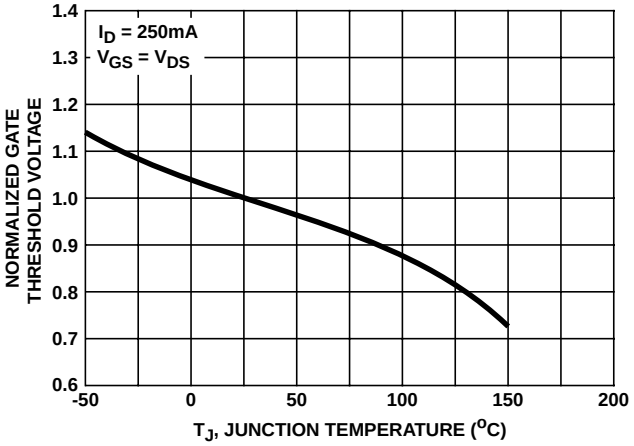


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

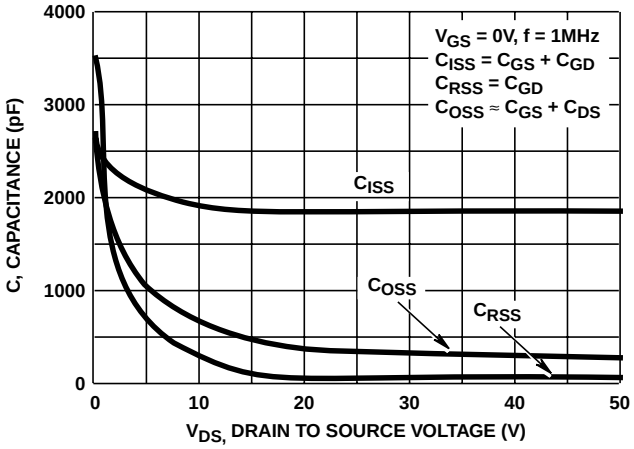
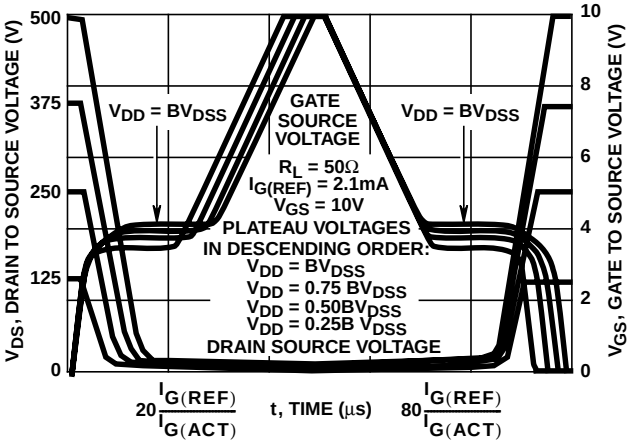


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

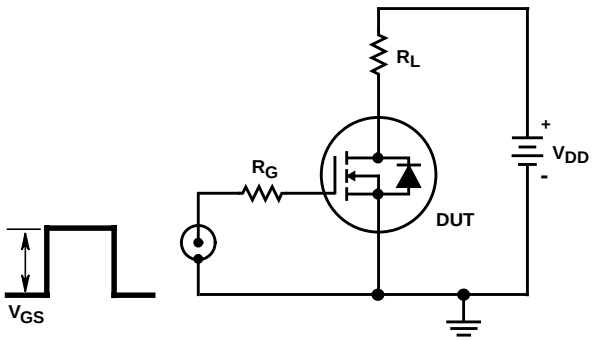


FIGURE 11. SWITCHING TIME TEST CIRCUIT

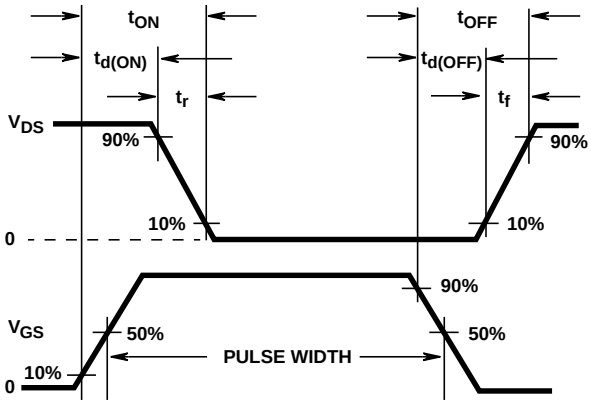


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS