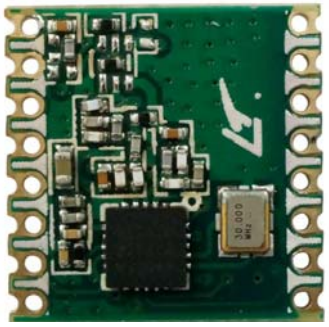
RFM24W ISM Transceiver module V 11

Features

- Frequency range = 142–1050 MHz
- Receive sensitivity = –126 dBm
- Modulation
  - (G)FSK & 4(G)FSK
  - OOK & ASK
- +11 dBmMax output power
- Low active power consumption
  - 10/13 mA RX
  - 19 mA TX at +10 dBm
- Ultra low current powerdown modes
  - 30 nA shutdown, 50 nA standby
- Data rate = 0.123 kbps to 1Mbps
- Fast wake and hop times
- Power supply = 1.8 to 3.6 V
- Excellent selectivity performance
  - 50 dB adjacent channel
- > 73 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
- Auto frequency control (AFC)
- Automatic gain control (AGC)
- Low Battery Detector
- Low BOM
- Temperature Sensor



RFM24W

Applications

- Smart metering (802.15.4g & Mbus)
- Remote control
- Home security and alarm
- Telemetry
- Garage and gate openers
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors

Description

The RFM24W module is high-performance, low current transceiver covering the sub-GHz frequency bands from 142 to1050 MHz. It offers outstanding sensitivity of –126 dBm while achieving extremely low active and standby current consumption. The RFM24W offers continuous frequency coverage across the entire sub-GHz band from 142–1050 MHz with extremely fine frequency resolution. The RFM24W offers exceptional output power of up to +11 dBm with outstanding TX efficiency. The high output power and sensitivity results in an industry leading link budget of 137 dB allowing extended ranges and highly robust communication links. Its active mode TX current consumption of 19 mA at +11 dBm and RX current of 10 mA coupled with extremely low standby current and fast wake times ensure extended battery life in the most demanding applications. The module is compliant with all worldwide regulatory standards: FCC, ETSI, and ARIB. All devices are designed to be compliant with 802.15.4g and WMbus smart metering standards.

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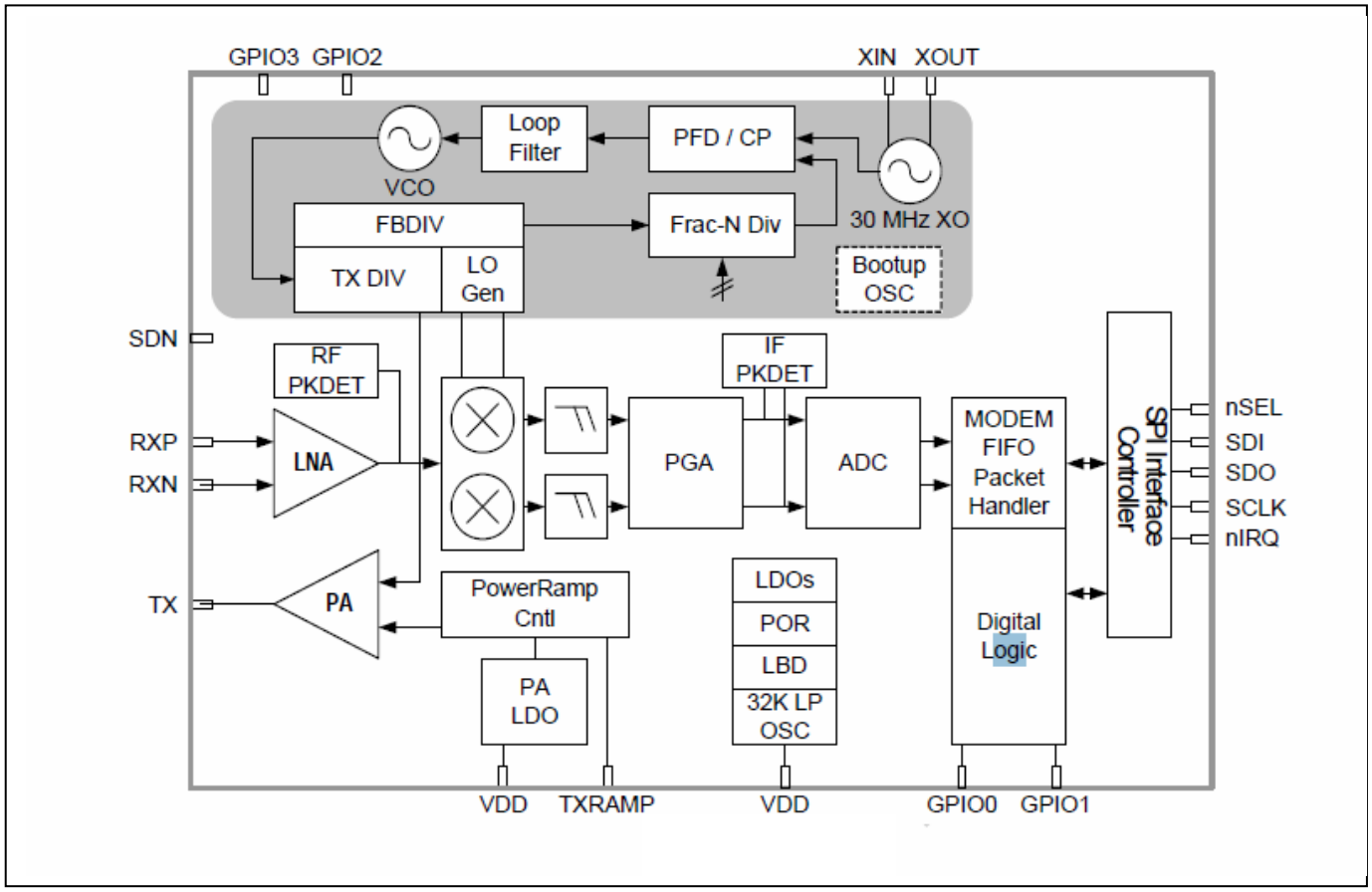
Functional Block Diagram



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1. Electrical Specifications

Table 1. DC Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range	V_{DD}		1.8	3.0	3.6	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF[2]	—	30	—	nA
	$I_{Standby}$	Register values maintained and RC oscillator/WUT OFF.	—	50	—	nA
	I_{Sleep}	RC Oscillator/WUT ON and all register values maintained, and all other blocks OFF.	—	900	—	nA
	$I_{Sensor-LBD}$	Low battery detector ON, register values maintained, and all other blocks OFF.[2]	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF.	—	1.8	—	mA
TUNE Mode Current	I_{Tune_RX}	RX Tune	—	6.5	—	mA
	I_{Tune_TX}	TX Tune	—	7.3	—	mA
RX Mode Current	I_{RXH}	High Performance Mode	—	13	—	mA
	I_{RXL}	Low Power Mode	—	10	—	mA
TX Mode Current	I_{TX_+10}	+10 dBm output power, Switched current match, 868 MHz	—	19	—	mA

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section of "1.1. Definition of Test Conditions" on page 11.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.

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Table 2. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range	FSYN		142	—	175	MHz
			284	—	350	MHz
			425	—	525	MHz
			850	—	1050	MHz
Synthesizer Frequency Resolution[2]	FRES-960	850—1050	—	57.22	—	Hz
	FRES-525	425—525	—	28.61	—	Hz
	FRES-350	283—350	—	19.07	—	Hz
	FRES-175	142—175	—	9.54	—	Hz
Synthesizer Settling Time[2]	tLOCK	Measured from leaving Ready mode with XOSC running to any frequency includ-ing VCO Calibration	—	50	—	µs
Phase Noise[2]	L ϕ (fM)	ΔF = 10 kHz, 460MHz	—	–106	—	dBc/Hz
		ΔF = 100 kHz, 460MHz	—	–120	—	dBc/Hz
		ΔF = 1 MHz, 460MHz	—	–123	—	dBc/Hz
		ΔF = 10 MHz, 460MHz	—	–130	—	dBc/Hz

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
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Table 3. Receiver AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RX Frequency Range	F_{RX}		142	—	175	MHz
			284	—	350	MHz
			425	—	525	MHz
			850	—	1050	MHz
RX Sensitivity	P_{RX-_2}	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250Hz)[2]	—	–126	—	dBm
	P_{RX-_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)[2]	—	–110	—	dBm
	P_{RX-_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)[2]	—	–106	—	dBm
	P_{RX-_125}	(BER < 0.1%) (125 kbps, GFSK, BT = 0.5, Δf = ±62.5 kHz)	—	–103	—	dBm
	P_{RX-_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–97	—	dBm
	P_{RX-_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, Δf = ±TBΔ kHz)	—	–88	—	dBm
	P_{RX-_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)[2]	—	–110	—	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)[2]	—	–102	—	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)[2]	—	–99	—	dBm
RX Channel Bandwidth[2]	BW		1.1	—	850	kHz
BER Variation vs Power Level[2]	P_{RX_RES}	Up to +5 dBm Input Level	—	0	0.1	ppm
RSSI Resolution	RES_{RSSI}		—	±0.5	—	dB
±1-Ch Offset Selectivity[2]	C/I_{1-CH}	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer and desired modulated with 2.4 kbps ΔF = 1.2 kHz GFSK with BT = 0.5, channel spacing = 25 kHz	—	–50	—	dB
±2-Ch Offset Selectivity[2]	C/I_{2-CH}		—	–52	—	dB

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.

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Table 3. Receiver AC Electrical Characteristics[1] (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Blocking 100K— 1 MHz	100K BLOCK	Desired Ref Signal 3 dB above sensitivity. Interferer and desired modulated with 2.4 kbps△F = 1.2 kHz GFSK	—	–57	—	dB
Blocking 1 MHz offset[2]	1 M BLOCK		—	–73	—	dB
Blocking at 8 MHz offset[2]	8MBLOCK		—	–83	—	dB
Image Rejection[2]	IMREJ	IF=468 kHz	—	–35	—	dB
Spurious Emissions[2]	POB_RX1	Measured at RX pins	—	—	–54	dBm

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.

Table 4. Transmitter AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TX Frequency Range	FTX		142	—	175	MHz
			284	—	350	MHz
			425	—	525	MHz
			850	—	960	MHz
(G)FSK Data Rate[2]	DRFSK		0.123	—	500	kbps
4(G)FSK Data Rate[2]	DR4FSK		0.123	—	1	MHz
OOK DataRate[2]	DROOK		0.123	—	120	kbps
Modulation Deviation Range	Δf_{960}	850–1050 MHz	—	3.75	—	MHz
	Δf_{525}	425–525 MHz	—	1.875	—	MHz
	Δf_{350}	283–350 MHz	—	1.25	—	MHz
	Δf_{175}	142–175 MHz	—	0.625	—	MHz
Modulation Deviation Resolution[2]	$F_{RES-960}$	850–1050 MHz	—	57.22	—	Hz
	$F_{RES-525}$	425–525 MHz	—	28.61	—	Hz
	$F_{RES-350}$	283–350 MHz	—	19.07	—	Hz
	$F_{RES-175}$	142–175 MHz	—	9.54	—	Hz

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
3. Output power is dependent on matching components and board layout.

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Output Power Range[1]	P_{TX}		-40	—	+11	dBm
TX RF Output Steps[2]	$\triangle P_{RF\_OUT}$	Using switched current match within 6 dB of max power	—	0.1	—	dB
TX RF Output Level[2] Variation vs. Temperature	$\triangle P_{RF\_TEMP}$	–40 to +85℃	—	1	—	dB
TX RF Output Level Variation vs. Frequency[2]	$\triangle P_{RF\_FREQ}$	Measured across 902–928 MHz	—	0.5	—	dB
Transmit Modulation Filtering[2]	B*T	Gaussian Filtering Bandwith Time Product	—	0.5	—	
Harmonics[2]	P_{2HARM}	Using reference design TX matching network and filter with max output power. Harmonics reduce linearly with output power.	—	—	-42	dBm
	P_{3HARM}		—	—	-42	dBm
Spurious Emissions[2]	P_{OB-TX1}	P_{OUT} = 11 dBm, Frequencies <1 GHz	—	—	–54	dBm
	P_{OB-TX2}	1–12.75 GHz, excluding harmonics	—	—	–42	dBm

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
3. Output power is dependent on matching components and board layout.

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Table 5. Auxiliary Block Specifications[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Temperature Sensor Accuracy[2]	TS_A	After calibration	—	TBD	—	°C
Temperature Sensor Sensitivity[2]	TS_S		—	1.85	—	mV/°C
Low Battery Detector Resolution[2]	LBD_{RES}		—	50	—	mV
Microcontroller Clock Output Frequency Range	F_{MC}	Configurable to 30 MHz, 15 MHz, 10 MHz, 4 MHz, 3 MHz, 2 MHz, 1 MHz, or 32.768 kHz	32.768K	—	30M	Hz
Temperature Sensor Conversion	$TEMP_{CT}$		—	3	—	msec
XTAL Range	$XTAL_{Range}$		25		32	MHz
30 MHz XTAL Start-Up time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	—	250	—	µs
30 MHz XTAL Cap Resolution[2]	$30M_{RES}$		—	100	—	fF
32 kHz XTAL Start-Up Time[2]	t_{32k}		—	1	—	sec
32 kHz Accuracy using Internal RC Oscillator[2]	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	4.5	—	ms

Notes:

1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.

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Table 6. Digital IO Specifications (GPIO_x, SCLK, SDO, SDI, nSEL, nIRQ)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	—	8	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	—	8	ns
Input Capacitance	C_{IN}		—	—	2	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	–10	—	10	µA
Input Current If Pullup is Activated	I_{INP}	V_{IL}=0 V	1	—	3	µA
Maximum Output Current	I_{OmaxLL}	DRV<1:0>=LL		1.8		mA
	I_{OmaxLH}	DRV<1:0>=LH		3.5		mA
	I_{OmaxHL}	DRV<1:0>=HL		5		mA
	I_{OmaxHH}	DRV<1:0>=HH		7		mA
Logic High Level Output Voltage	V_{OH}	I_{OUT} = 500 µA	V_{DD} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	I_{OUT} = 500 µA	—	—	V_{DD} x 0.2	V

Note: All specifications guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 11.

Table 7. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.6	V
Instantaneous $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +8.0	V
Sustained $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +6.5	V
Voltage on Digital Control Inputs	–0.3, V_{DD} + 0.3	V
Voltage on Analog Inputs	–0.3, V_{DD} + 0.3	V
RX Input Power	+10	dBm
Operating Ambient Temperature Range T_A	–40 to +85	°C
Thermal Impedance θ_{JA}	30	°C/W
Junction Temperature T_J	+125	°C
Storage Temperature Range T_{STG}	–55 to +125	°C

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX $V_{RF\text{-}peak}$ on TX output pin. Caution: ESD sensitive device.

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1.1. Definition of Test Conditions

Production Test Conditions:

- T_A = +25 °C
- V_{DD} = +3.3 VDC
- Sensitivity measured at 919 MHz
- TX output power measured at 915 MHz
- External reference signal (XOUT) = 1.0 V_{PP} at 30 MHz, centered around 0.8 VDC
- Production test schematic (unless noted otherwise)
- All RF input and output levels referred to the pins of the RFM24W module

Qualification Test Conditions:

- T_A = –40 to +85 °C
- V_{DD} = +1.8 to +3.6 VDC
- Using TX/RX Split Antenna reference design or production test schematic
- All RF input and output levels referred to the pins of the RFM24W

Module

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2. Functional Description

The RFM24W module is high-performance, low-current, wireless ISM transceivers that cover the sub-GHz bands. The wide operating voltage range of 1.8–3.6 V and low current consumption make the RFM24W an ideal solution for battery powered applications. The RFM24W operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the 2/4-level FSK/GFSK or OOK/ASK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.
A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 0.123 kbps to 1 Mbps. The RFM24W operates in the frequency bands of 142–175, 283–350, 425–525, and 850–1050 MHz with a maximum accuracy of 57.22 Hz frequency accuracy. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The RFM24W is designed to support single coin cell operation with current consumption below 19 mA for +10 dBm output power. Two match topologies are available for the RFM24W, class-E and switched-current. Class-E matching provides optimal current consumption, while switched-current matching demonstrates the best performance over varying battery voltage with slightly higher current consumption. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. The RFM24W supports frequency hopping, TX/RX switch control, and antenna diversity switch control to extend the link range and improve performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. Antenna diversity is completely integrated into the RFM24W and can improve the system link budget by 8–10 dB, resulting in substantial range increases under adverse environmental conditions. A highly configurable packet handler allows for autonomous encoding/decoding of nearly any packet structure. Additional system features, such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, and preamble detection, reduce overall current consumption and allows for the use of lower-cost system MCUs. An integrated temperature sensor, power-on-reset (POR), and GPIOs further reduce overall system cost and size. The RFM24W is designed to work with an MCU, crystal, and a few passives to create a very low-cost system.

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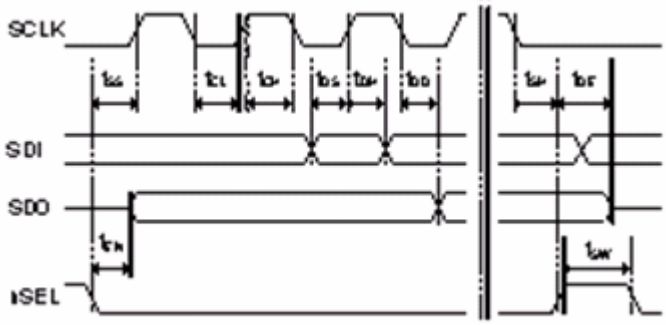
3. Controller Interface

3.1. Serial Peripheral Interface (SPI)

The RFM24W communicates with the host MCU over a standard 4-wire serial peripheral interface (SPI): SCLK, SDI, SDO, and nSEL. The SPI interface is designed to operate at a maximum of 10 MHz. The SPI timing parameters are demonstrated in Table 8. The host MCU writes data over the SDI pin and can read data from the device on the SDO output pin. Figure 3 demonstrates an SPI write command. The nSEL pin should go low to initiate the SPI command. The first byte of SDI data will be one of the firmware commands followed by n bytes of parameter data which will be variable depending on the specific command. The rising edges of SCLK should be aligned with the center of the SDI data.

Table 8. Serial Interface Timing Parameters

Symbol	Parameter	Min (ns)	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	

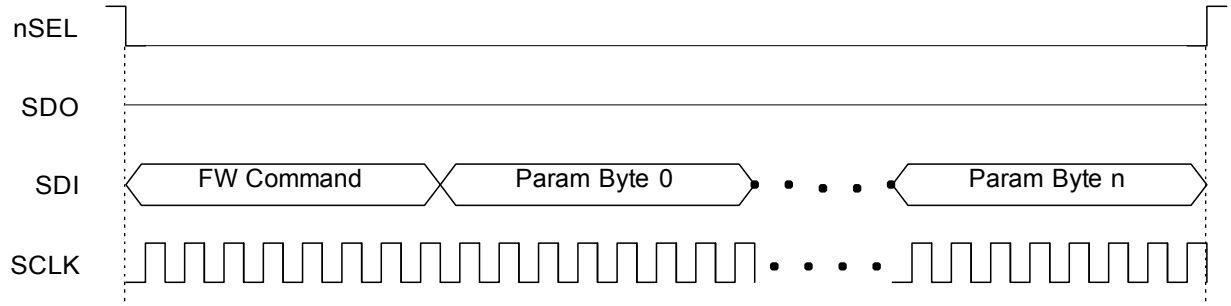


Figure 3. SPI Write Command

The RFM24W contains an internal MCU which controls all the internal functions of the radio. For SPI read commands a typical MCU flow of checking clear-to-send (CTS) is used to make sure the internal MCU has executed the command and prepared the data to be output over the SDO pin. Figure 4 demonstrates the general flow of an SPI read command. Once the CTS value reads FFh then the read data is ready to be clocked out to the host MCU. The typical time for a valid FFh CTS reading is 20 µs. Figure 5 demonstrates the remaining read cycle after CTS is set to FFh. The internal MCU will clock out the SDO data on the negative edge so the host MCU should process the SDO data on the rising edge of SCLK.

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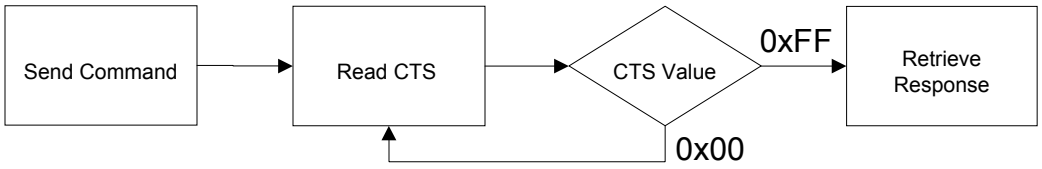
Firmware Flow



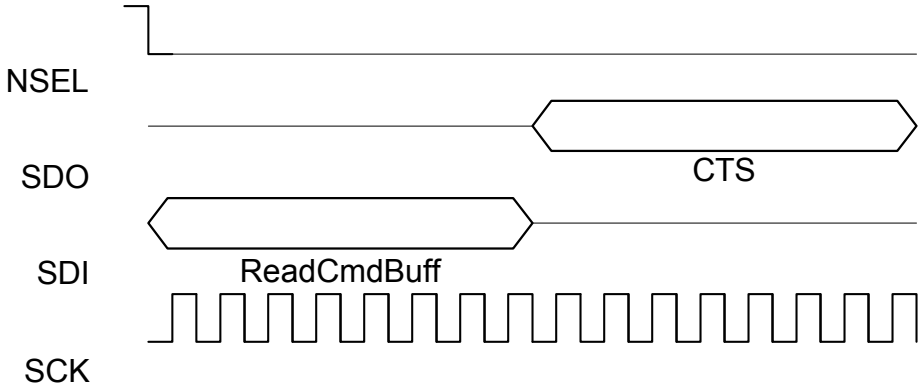


Figure 4. SPI Read Command—Check CTS Value

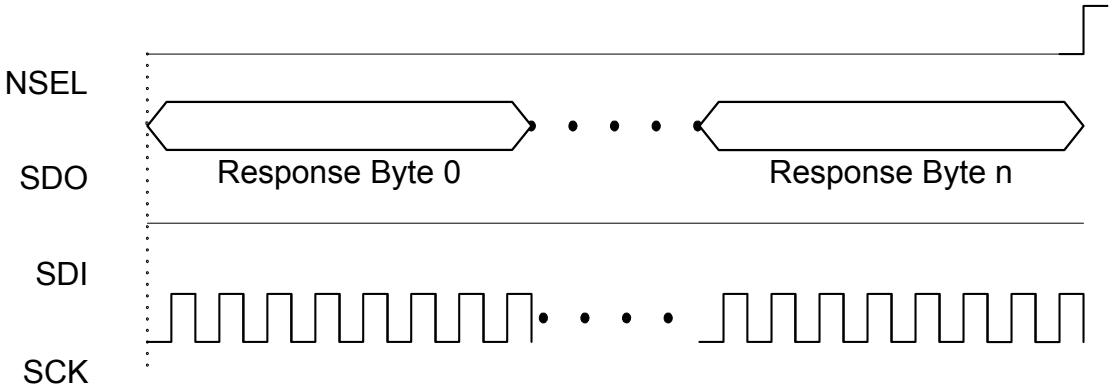


Figure 5. SPI Read Command—Clock Out Read Data

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3.2. Fast Response Registers

The fast response registers are registers that can be read immediately without the requirement to monitor and check CTS. There are four fast response registers that can be programmed for a specific function. The fast response registers can be read through API commands, 0x51 for Fast Response A, 0x53 for Fast Response B, 0x55 for Fast Response C, and 0x57 for Fast Response D. The fast response registers can be configured by the "FRR_CTL_X_MODE" properties.

The fast response registers may be read in a burst fashion. After the initial 16 clock cycles, each additional 8 clock cycles will clock out the contents of the next fast response register in a circular fashion

3.3. Operating Modes and Timing

There are four primary states in the Si446x radio state machine: SHUTDOWN, IDLE, TX, and RX (see Figure 6). The SHUTDOWN state completely shuts down the radio to minimize current consumption. There are five different configurations/options for the IDLE state which can be selected to optimize the chip to the applications needs. API commands "Start RX", "Start TX", and "Change State" control the operating mode/state with the exception of SHUTDOWN which is controlled by SDN, pin 1. Table 9 shows each of the operating modes with the time required to reach either RX or TX mode as well as the current consumption of each mode.

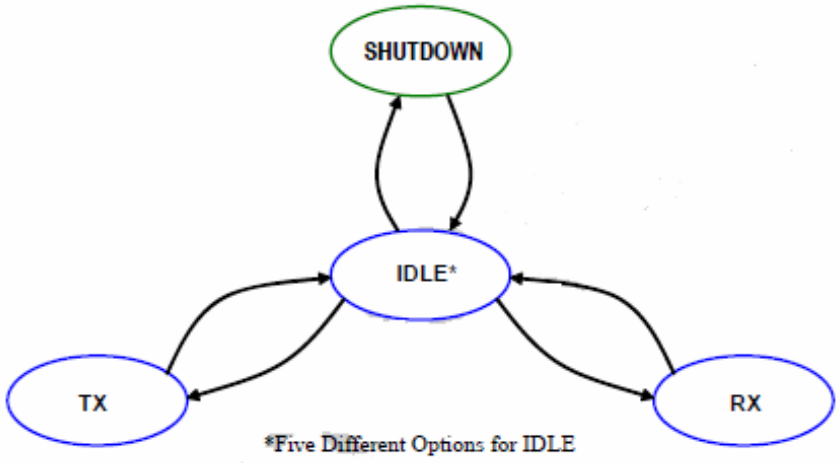

Figure 6. State Machine Diagram

Table 9. Operating Modes Response Time and Current Consumption

State/Mode	Response Time to		Current in State /Mode (µA)
	TX	RX	
Shut Down State	20 ms	20 ms	30 nA
Idle States: Standby Mode Sleep Mode SPI Active Mode Ready Mode Tune Mode	 400 µs 400 µs 320 µs 100 µs 100 µs	 400 µs 400 µs 320 µs 100 µs 100 µs	 50 nA 900 nA 340 µA 1.8 mA 5 mA
TX State	NA	100 µs	19 mA @ +10 dBm
RX State	100 µs	NA	10 or 13 mA

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Figure 7 demonstrates the timing and current consumption in each mode associated with commanding the chip from SHUTDOWN to TX state. Figure 8 demonstrates the timing and current consumption for each mode associated with commanding the chip from STANDBY to TX state. The most advantageous state to use will depend on the duty cycle of the application or how often the part is in either RX or TX state. In most applications the utilization of the STANDBY state will be most advantageous for battery life but for very low duty cycle applications SHUTDOWN will have an advantage. For the fastest timing the next state can be selected in the "Start RX" or "Start TX" API commands to minimize SPI transactions and internal MCU processing.

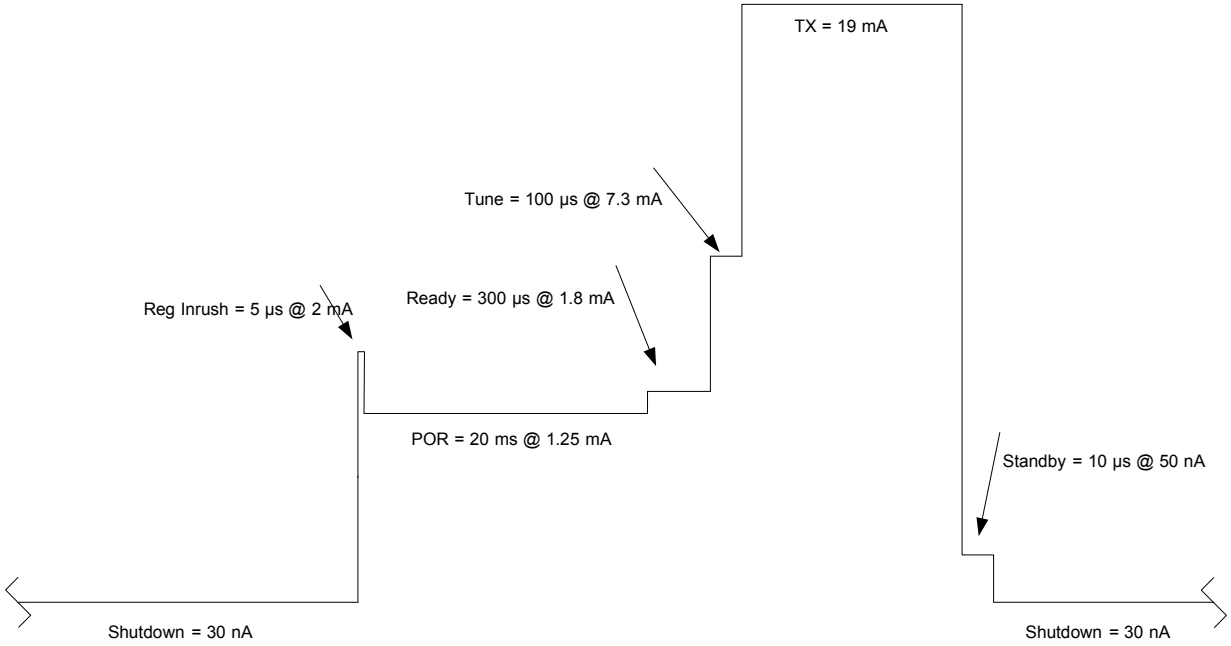

Figure 7. Start-Up Timing and Current Consumption using Shutdown State

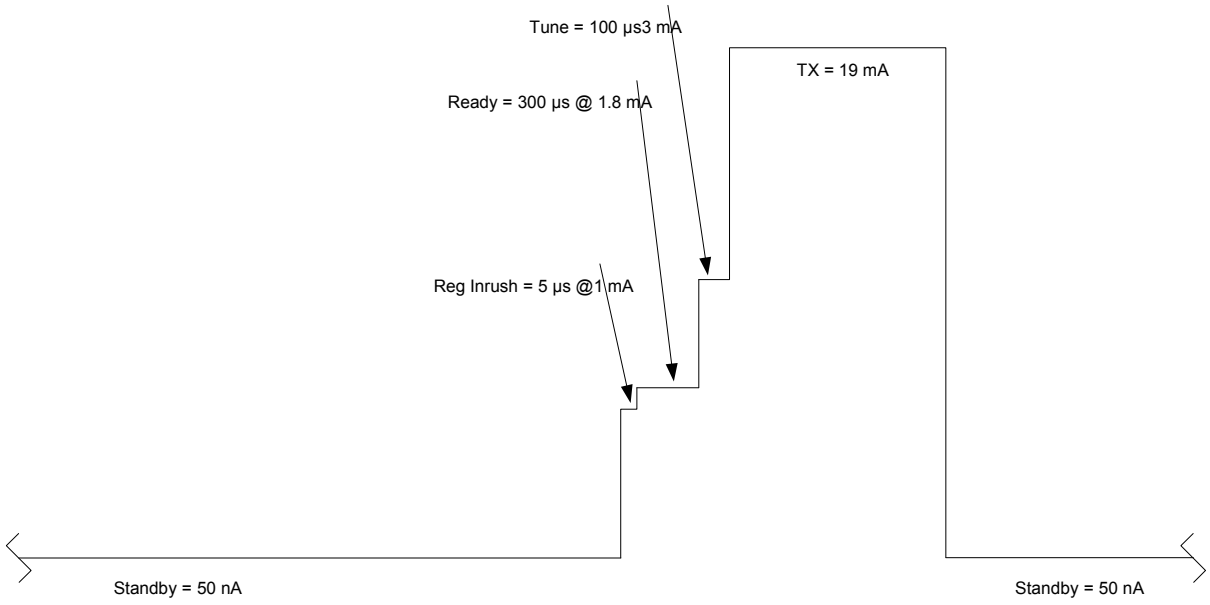

Figure 8. Start-Up Timing and Current Consumption using Standby State

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3.3.1. SHUTDOWN State

The SHUTDOWN state is the lowest current consumption state of the device with nominally less than 20 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 1) high. The SDN pin should be held low in all states except the SHUTDOWN state. In the SHUTDOWN state, the contents of the registers are lost and there is no SPI access. When coming out of the SHUTDOWN state a power on reset (POR) will be initiated along with the internal calibrations.

3.3.2. IDLE States

There are five different modes in the IDLE state which may be commanded. All modes have a tradeoff between current consumption and response time to TX/RX mode. This tradeoff is shown in Table 9. After the POR event, SWRESET, or exiting from the SHUTDOWN state the chip will default to the IDLE-READY mode.

3.3.3. STANDBY Mode

STANDBY mode has the lowest current consumption of the five IDLE states. In this state the register values are maintained with all other blocks disabled. The SPI is accessible during this mode but an SPI event will enable an internal boot oscillator and automatically move the part to SPI ACTIVE mode. After an SPI event the host will need to re-command the device back to STANDBY mode through the “Change State” API command to achieve the 100 nA current consumption. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.4. SLEEP Mode

In SLEEP mode the Wake-Up-Timer and a 32 kHz clock source are enabled. The source of the 32 kHz clock can either be an internal 32 kHz RC oscillator which is periodically calibrated or a 32 kHz oscillator using an external XTAL.The SPI is accessible during this mode but an SPI event will enable an internal boot oscillator and automatically move the part to SPI ACTIVE mode. After an SPI event the host will need to re-command the device back to SLEEP. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.5. SPI ACTIVE Mode

In SPI ACTIVE mode the SPI and a boot up oscillator are enabled. After SPI transactions during either STANDBY or SLEEP mode the device will not automatically return to these modes. A “Change State” API command will be required to return to either the STANDBY or SLEEP modes.

3.3.6. READY Mode

READY Mode is designed to give a fast transition time to TX or RX state with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to TX or RX mode by eliminating the crystal start-up time.

3.3.7. TX State

The TX state may be entered from any of the IDLE modes by using the “Start TX” or “Change State” API command. A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA. The following sequence of events will occur automatically when going from STANDBY mode to TX mode.

1. Enable the digital LDO and the analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).
3. Enable PLL.
4. Calibrate VCO/PLL.
5. Wait until PLL settles to required transmit frequency (controlled by an internal timer).
6. Activate power amplifier and wait until power ramping is completed (controlled by an internal timer).
7. Transmit packet.

Steps in this sequence may be eliminated depending on which IDLE mode the chip is configured to prior to commanding to TX. By default, the VCO and PLL are calibrated every time the PLL is enabled. When the “Start TX” API command is utilized the next state may be defined to ensure optimal timing and turnaround.

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3.3.8. RX State

The RX state may be entered from any of the IDLE modes by using the “Start RX” or “Change State” API command. A built-in sequencer takes care of all the actions required to transition from one of the IDLE modes to the RX state. The following sequence of events will occur automatically to get the chip into RX mode when going from STANDBY mode to RX mode:

1. Enable the digital LDO and the analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).
3. Enable PLL.
4. Calibrate VCO
5. Wait until PLL settles to required receive frequency (controlled by an internal timer).
6. Enable receiver circuits: LNA, mixers, and ADC.
7. Enable receive mode in the digital modem.

Depending on the configuration of the radio all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC. Similar to the TX state the next state after RX may be defined in the “Start RX” API command.

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.4. Application Programming Interface (API)

An application programming interface (API) which the host MCU will communicate with is embedded inside the device. The API is divided into two sections, commands and properties. The commands are used to control the chip and retrieve its status. The properties are general configurations which will change infrequently. The available commands are shown in Table 10.

Table 10. API Commands

Number	Name	Description
0x00	NOP	No operation command
0x01	PART_INFO	Reports basic information about the device
0x02	POWER_UP	Boot options and XTAL freq offset
0x04	PATCH_IMAGE	OTP patch version
0x10	FUNC_INFO	Returns the function revision information of the device
0x11	SET_PROPERTY	Sets the value of a property
0x12	GET_PROPERTY	Retrieves the value of a property
0x13	GPIO_PIN_CFG	Configures the GPIO pins
0x14	GET_SENSOR_READING	Retrieves temp sensor, low battery detector, or ADC reading
0x15	FIFO_RESET	Resets the TX and RX FIFO
0x20	GET_INT_STATUS	Returns the interrupt status
0x21	GET_PH_STATUS	Returns the packet handler status and interrupts
0x22	GET_MODEM_STATUS	Returns the modem status and interrupts
0x23	GET_CHIP_STATUS	Returns the chip status and interrupts
0x31	START_TX	Changes to TX state and configures common parameters
0x32	START_RX	Changes to RX state and configures common parameters
0x33	REQUEST_DEVICE_ STATE	Returns current device state
0x34	CHANGE_STATE	Commands the part to any of the defined states or modes
0x50	FAST RESPONSE A	Fast response registers for faster read access
0x51	FAST RESPONSE B	Fast response registers for faster read access
0x53	FAST RESPONSE C	Fast response registers for faster read access
0x57	FAST RESPONSE D	Fast response registers for faster read access
0x66	TX_FIFO_WRITE	Write data to TX FIFO
0x77	RX_FIFO_READ	Read data from RX FIFO

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The description of the “Start TX” command is shown in Figure 9 as an example. If a property has previously been set or a default configuration is sufficient it is not necessary to write all arguments. For instance if the user wants to command the part to TX state with the default or previous settings for CHANNEL[7:0], TXCOMPLETE_STATE[3:0], etc then only the CMD 0x31 needs to be sent. It is not necessary to send the remaining arguments unless it is desired to change these arguments.

- START_TX
  - Summary: *Switches to TX state. Command arguments are retained though sleep state, so these only need to be written when they change.*
  - Purpose
    - Switches to TX state when condition is met. Switch to specified state when TX packet completes.
  - Command Stream

START_TX Command	7	6	5	4	3	2	1	0
CMD	0x31							
CHANNEL	CHANNEL[7:0]							
CONDITION	TXCOMPLETE_STATE[3:0]				0	RETRANSMIT	START[1:0]	
TX_LEN	TX_LEN[15:8]							
TX_LEN	TX_LEN[7:0]							

  - Reply Stream

START_TX Reply	7	6	5	4	3	2	1	0
CMD_COMPLETE	CTS[7:0]							

  - Parameters
    - CHANNEL[7:0] - Channel number
    - TXCOMPLETE_STATE[7:4] - State to go to when current packet TX completes.
      - 0 = No change
      - 1 = Sleep state.
      - 2 = Spi Active state.
      - 3 = Ready state.
      - 4 = Tune state.
      - 5 = TX state.
      - 6 = RX state.
      - 7 = TRX state.
      - 8 = Shutdown state.
      - 9 = Cal Complete state.
    - RETRANSMIT
      - 0 = Send data that has been written to fifo.
      - 1 = Send last packet again (and no new data has been written to fifo)

Figure 9. Start TX Command Description

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3.5. Interrupts

The RFM24W is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Registers. The nIRQ output signal will then be reset until the next change in status is detected.

The interrupts sources are grouped into three groups: Packet Handler, Chip Status, and Modem. The individual interrupts in these groups can be enabled/disabled in the interrupt property registers, 0101, 0102, and 0103. An interrupt must be enabled for it to trigger an event on the nIRQ pin. The interrupt group must be enabled as well as the individual interrupts in API property 0100.

Once an interrupt event occurs and the nIRQ pin is low there are two ways to read and clear the interrupts. All of the interrupts may be read and cleared in the “Get INT Status” API command. By default all interrupts will be cleared once read. If only specific interrupts want to be read in the fastest possible method the individual interrupt groups (Packet Handler, Chip Status, Modem) may be read and cleared by the “Get Modem Status”, “Get PH (packet handler) Status, and “Get Chip Status” API commands.

The instantaneous status of a specific function maybe read if the specific interrupt is enabled or disabled. The status results are provided after the interrupts and can be read with the same commands as the interrupts.

The fast response registers can also give information about the interrupt groups but reading the fast response registers will not clear the interrupt and reset the nIRQ pin.

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4. Modulation and Hardware Configuration Options

The RFM24W supports different modulation options and can be used in various configurations to tailor the device to any specific application or legacy system for drop in replacement. The modulation and configuration options are set in API property, MODEM_MOD_TYPE.

- Summary: *Modulation Type*
- Purpose
  - This property selects between OOK, FSK, 4FSK and GFSK modulation, modulation source, and tx direct mode control.
  - The modulator must be configured for one mode through the entire packet. If portions of the packet alternate between FSK and 4FSK modes, the modem should be programmed to 4FSK mode
- Property: 0x2000
- Default: 0x00
- Fields
  - TX_DIRECT_MODE_TYPE - default:0
    - 0 = Direct mode operates in synchronous mode
    - 1 = Direct mode operates in non-synchronous mode
  - TX_DIRECT_MODE_GPIO[1:0] - default:0x0
    - 0 = TX direct mode uses gpio0 as data source
    - 1 = TX direct mode uses gpio1 as data source
    - 2 = TX direct mode uses gpio2 as data source
    - 3 = TX direct mode uses gpio3 as data source
  - MOD_SOURCE[1:0] - default:0x0
    - 0 = Modulation source is packet handler fifo
    - 1 = Modulation source is direct mode pin
    - 2 = Modulation source is pseudo-random generator
  - MOD_TYPE[2:0] - default:0x0
    - 0 = CW
    - 1 = OOK
    - 2 = FSK
    - 3 = GFSK
    - 4 = 4FSK
- Register View

MODEM_MOD_TYPE							
7	6	5	4	3	2	1	0
TX_DIRECT_MODE_TYPE	TX_DIRECT_MODE_GPIO[1:0]		MOD_SOURCE[1:0]		MOD_TYPE[2:0]		
0	0x0		0x0		0x0		

Figure 10. Modulation and Hardware Configuration Options

4.1. Modulation Types

The RFM24W supports five different modulation options: Gaussian Frequency Shift Keying (GFSK), Frequency Shift Keying (FSK), Four Level GFSK (4GFSK), Four Level FSK (4FSK), On-Off Keying (OOK), and Amplitude Shift Keying (ASK). Minimum Shift Keying (MSK) can also be created by using GFSK settings. GFSK is the recommended modulation type as it provides the best performance and cleanest modulation spectrum. The modulation type is set by the “MOD_TYPE[2:0]” registers in the “MODEM_MOD_TYPE” API property. A continuous-wave (CW) carrier may also be selected for RF evaluation purposes. The modulation source may also be selected to be a pseudo-random source for evaluation purposes.

4.2. Hardware Configuration Options

There are three main methods to transfer RX/TX data from the host MCU to the RF device. There are various other configurations options of these three main methods that will be described in the individual subsections.

- **FIFO Mode**—Utilizes the internal 64byte TX and RX FIFO’s. Permits use of the internal packet handler.
- **Direct Mode**—Data/Data CLK are programmed directly onto a GPIO but a 101010… preamble is used
- **RAW Direct Mode**—Data is programmed directly onto a GPIO but a 101010.. preamble is NOT used.

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4.2.1. FIFO Mode

In FIFO mode, the transmit and receive data is stored in integrated FIFO register memory. The TX FIFO is accessed by writing command 66h followed directly by the data/clk that the host wants to write into the TX FIFO. The RX FIFO is accessed by writing command 77h followed by the number of clock cycles of data the host would like to read out of the RX FIFO. The RX data will be clocked out onto the SDO pin.

In TX mode if the packet handler is enabled, the data bytes stored in FIFO memory are "packaged" together with other fields and bytes of information to construct the final transmit packet structure. These other potential fields include the Preamble, Sync word, Header, CRC checksum, etc. The configuration of the packet structure in TX mode is determined by the Automatic Packet Handler (if enabled), in conjunction with a variety of Packet Handler properties. If the Automatic Packet Handler is disabled, the entire desired packet structure should be loaded into FIFO memory; no other fields (such as Preamble or Sync word will be automatically added to the bytes stored in FIFO memory). For further information on the configuration of the FIFOs for a specific application or packet size, see "6. Data Handling and Packet Handler" on page 29. In RX mode, only the bytes of the received packet structure that are considered to be "data bytes" are stored in FIFO memory. Which bytes of the received packet are considered "data bytes" is determined by the Automatic Packet Handler (if enabled), in conjunction with the Packet Handler configuration. If the Automatic Packet Handler is disabled, all bytes following the Sync word are considered data bytes and are stored in FIFO memory. Thus, even if Automatic Packet Handling operation is not desired, the preamble detection threshold and Sync word still need to be programmed so that the RX Modem knows when to start filling data into the FIFO. When the FIFO is being used in RX mode, all of the received data may still be observed directly (in realtime) by properly programming a GPIO pin as the RXDATA output pin; this can be quite useful during application development. When in FIFO mode, the chip will automatically exit the TX or RX State when either the ipksent or ipkvalid interrupt occurs. The chip will return to the IDLE state programmed in the argument of the “START TX” or “START RX” API command, TXCOMPLETE_STATE[3:0] or RXCOMPLETE_STATE[3:0]. For example, the chip may be placed into TX mode by sending the “START TX” command and by writing the 30h to the TXCOMPLETE_STATE[3:0] argument. The chip will transmit all of the contents of the FIFO and the ipksent interrupt will occur. When this event occurs, the chip will return to the READY state as defined by TXCOMPLETE_STATE[3:0] = 30h.

4.2.2. Direct Mode

For legacy systems that perform packet handling within the host MCU or other baseband chip, it may not be desirable to use the FIFO. For this scenario, a Direct Mode is provided which bypasses the FIFOs entirely. In TX direct mode, the TX modulation data is applied to an input pin of the chip and processed in "real time" (i.e., not stored in a register for transmission at a later time). Any of the GPIO may be configured for use as the TX Data input function. Furthermore, an additional pin may be required for a TX Clock output function if GFSK modulation is desired (only the TX Data input pin is required for FSK). To achieve direct mode the GPIO must be configured in “GPIO_PIN_CFG” API command as well as the “MODEM_MOD_TYPE” API property. For GFSK “TX_DIRECT_MODE_TYPE” must be set to synchronous. For ASK or FSK direct mode type should be set to asynchronous. The MOD_SOURCE[1:0] should be set to 01h for are all direct mode configurations. In RX direct mode, the RX Data and RX Clock can be programmed for direct (real-time) output to GPIO pins. The microcontroller may then process the RX data without using the FIFO or packet handler functions of the RFIC. In RX direct mode, the chip must still acquire bit timing during the Preamble, and thus the preamble detection threshold must still be programmed. Once the preamble is detected, certain bit timing functions within the RX Modem change their operation for optimized performance over the remainder of the packet. It is not required that a Sync word be present in the packet in RX Direct mode; however, if the Sync word is absent then the skipsyn bit must be set, or else the bit timing and tracking function within the RX Modem will not be configured for optimum performance.

4.2.3. RAW Direct Mode

The only difference between RAW Direct Mode and Direct Mode is the structure of the packet being used. In a conventional packet structure there is a 101010 preamble pattern which the internal modem uses to perform such functions as clock recovery. Many legacy applications do not have a 101010 preamble pattern so a special demodulator has been designed into the Si446x family to handle these types of application scenarios. The RAW mode demodulator will result in slightly less performance than the standard demodulator with a conventional preamble pattern but it will still provide glitch-less, stable, low jitter data. To achieve RAW mode the device should be configured as described in “4.2.2. Direct Mode” and also the RAW mode options should be selected in the calculator API.

5. Internal Functional Blocks

The following sections provide an overview to the key internal blocks and features.

5.1. RX Chain

The internal low-noise amplifier (LNA) is designed to be a wide-band LNA that can be matched with three external discrete components to cover any common range of frequencies in the sub-GHz band. The LNA has extremely low noise to suppress the noise of the following stages to achieve optimal sensitivity so no external gain or front-end modules are necessary. The LNA has gain control which is controlled by the internal automatic gain control (AGC) algorithm. The LNA is followed by an I-Q mixer, filter, programmable gain amplifier (PGA), and ADC. The I-Q mixers downconvert the signal to an intermediate frequency. The PGA then boosts the gain to be within dynamic range of the ADC. The ADC rejects out of band blockers and converts the signal to the digital domain where filtering, demodulation, and processing is performed. Peak detectors are integrated at the output of the LNA and PGA for use in the AGC algorithm.

5.2. RX Modem

Using high-performance ADCs allows channel filtering, image rejection, and demodulation to be performed in the digital domain which allows for large amounts of flexibility to optimize the device for a particular application. The digital modem performs the following functions:

- Channel selection filter
- TX modulation
- RX demodulation
- Automatic Gain Control (AGC)
- Preamble detection
- Invalid preamble detection
- Radio signal strength indicator (RSSI)
- Automatic frequency compensation (AFC)
- Packet handling including EZMAC® features
- Cyclic redundancy check (CRC)

The digital channel filter and demodulator are optimized for ultra low power consumption and are highly configurable. Supported modulation types are GFSK, FSK, 4GFSK, 4FSK, ASK, and OOK. The channel filter can be configured to support bandwidths ranging from 850 down to 1.1 kHz. A large variety of data rates are supported ranging from 0.123 up to 1 Mbps. The configurable preamble detector is used to improve the reliability of the sync-word detection. The sync-word detector is only enabled when a valid preamble is detected, significantly reducing the probability of false detection. The received signal strength indicator (RSSI) provides a measure of the signal strength received on the tuned channel. The resolution of the RSSI is 0.5 dB. This high resolution RSSI enables accurate channel power measurements for clear channel assessment (CCA), carrier sense (CS), and listen before talk (LBT) functionality. The extensive programmability of the packet header allows for advanced packet filtering which in turn enables a mix of broadcast, group, and point-to-point communication. A wireless communication channel can be corrupted by noise and interference, and it is therefore important to know if the received data is free of errors. A cyclic redundancy check (CRC) is used to detect the presence of erroneous bits in each packet. A CRC is computed and appended at the end of each transmitted packet and verified by the receiver to confirm that no errors have occurred. The packet handler and CRC can significantly reduce the load on the system microcontroller allowing for a simpler and cheaper microcontroller. The digital modem includes the TX modulator which converts the TX data bits into the corresponding stream of digital modulation values to be summed with the fractional input to the sigma-delta modulator. This modulation approach results in highly accurate resolution of the frequency deviation. A Gaussian filter is implemented to support GFSK and 4GFSK, considerably reducing the energy in the adjacent channels. The default bandwidth-time product (BT) is 0.5 for all programmed data rates, but it may be adjusted to other values.

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5.2.1. Automatic Gain Control (AGC)

The AGC algorithm is implemented digitally using an advanced control loop optimized for fast response time. The AGC occurs within a single bit or in less than 2 μs. Peak detectors at the output of the LNA and PGA allow for optimal adjustment of the LNA gain and PGA gain to optimize IM3, selectivity, and sensitivity performance.

5.2.2. Auto Frequency Correction (AFC)

Frequency mistuning caused by crystal inaccuracies can be compensated by enabling the digital automatic frequency control (AFC) in receive mode. There are two types of integrated frequency compensation, modem frequency compensation, and AFC by adjusting the PLL frequency. With AFC disabled the modem compensation can correct for frequency offsets up to ±0.25 times the IF bandwidth. When the AFC is enabled, the received signal will be centered in the pass-band of the IF filter, providing optimal sensitivity and selectivity over a wider range of frequency offsets up to ±0.35 times the IF bandwidth. When AFC is enabled, the preamble length needs to be long enough to settle the AFC. In general, one byte of preamble is sufficient to settle the AFC.

5.2.3. Image Rejection and Calibration

Since the receiver utilizes a low-IF architecture the selectivity will be affected by the image frequency. The IF frequency is 468.75kHz and the image frequency will be at 937.5kHz below the RF frequency. The native image rejection of the RFM24W is 35dB. The calibration is performed during the initial cold boot and does not require an external signal source. Also available in the Si4464/63 is the option to shift the IF frequency. With this option the IF frequency can be shifted to the adjacent channel putting the image frequency in the alternate channel.

5.2.4. Received Signal Strength Indicator

The received signal strength indicator (RSSI) is an estimate of the signal strength in the channel to which the receiver is tuned. The RSSI measurement is done after the channel filter so it is only a measurement of the in-band signal power, desired or undesired. There are multiple options for reading the RSSI which are configured in “MODEM_RSSI_CONTROL”. The RSSI can be set to update every bit or averaged over a four bit period. A latched version of the RSSI may be saved and read after the packet. The current RSSI value or latched RSSI value are read by readying the “GET_MODEM_STATUS” API command. The RSSI value can also be programmed into one of the fast response registers. Clear channel assessment (CCA) may also be performed by programming an RSSI threshold in “MODEM_RSSI_THRESH” and enabling this interrupt or programming a GPIO for this function.

To minimize the amount of time associated with reading the RSSI for frequency hopping applications automatic hop control is available based on an RSSI threshold. Automatic hop features are available to hop based on the availability of preamble or not, see the section for fast frequency hopping for more details on this feature.

5.3. Synthesizer

An integrated Sigma Delta (ΣΔ) Fractional-N PLL synthesizer capable of operating over the bands from 142–175, 283-350MHz, 425–525, and 850–1050 MHz. Using a ΣΔ synthesizer has many advantages; it provides flexibility in choosing data rate, deviation, channel frequency, and channel spacing. The transmit modulation is applied directly to the loop in the digital domain through the fractional divider which results in very precise accuracy and control over the transmit deviation. The frequency resolution in the 850–1050 MHz band is 57.22 Hz with more resolution in the other bands. The nominal reference frequency to the PLL is 30 MHz but any XTAL frequency from 25MHz to 32MHz may be used. The configuration calculator will automatically account for the XTAL frequency being used. The PLL utilizes a differential LC VCO, with integrated on-chip inductors. The output of the VCO is followed by a configurable divider which will divide down the signal to the desired output frequency band.

5.3.1. Synthesizer Frequency Control

$$RF\_carrier=(fc\_inte+\frac{txfo+fc\_frac+if\_freq}{2^{19}})\times\frac{freq\_xo\times2\times(2-hi\_pfm\_div\_mode)}{outdiv}(Hz)$$

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5.3.1.1. EZ Frequency Programming

5.3.1.2. Fast Frequency Hopping

5.4. Transmitter (TX)

The RFM24W is designed to supply +10dBm output power for less than 20mA for applications which require operation from a single coin cell battery. The RFM24W can also operate with either class-E or switched current matching. All PA options are single-ended to allow for easy antenna matching and low BOM cost. Automatic ramp-up and ramp-down is automatically performed to reduce unwanted spectral spreading.

5.5. Crystal Oscillator

The RFM24W includes an integrated crystal oscillator with a fast start-up time of less than 250 µs. The design is differential with the required crystal load capacitance integrated on-chip to minimize the number of external components. By default, all that is required off-chip is the crystal. The default crystal is 30MHz but the circuit is designed to handle any XTAL from 25 to 32 MHz. If a crystal different than 30MHz is used the "GLOBAL_CLK_XTAL_ADJUST" API property must be modified. The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through "XXX" API property. The total internal capacitance is 12.7 pF and is adjustable in 127 steps (100 fF/step). The crystal frequency adjustment can be used to compensate for crystal production tolerances. Utilizing the on-chip temperature sensor and suitable control software, the temperature dependency of the crystal can be canceled.

A TCXO or external signal source can easily be used in lieu of a conventional XTAL and should be connected to the XIN pin. The incoming signal is ac coupled internally to a squaring buffer so no external ac coupling or dc bias is required. If dc is provide it should be set to 500 mV. The incoming signal amplitude is should be set in the range from 500–900 mV. The internal capacitor bank will create a capacitive divider when an external source is used so the XTAL capacitor bank should be set to 0.

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6. Data Handling and Packet Handler

6.1. RX and TX FIFOs

Two 64 byte FIFOs are integrated into the chip, one for RX and one for TX, as shown in Figure 11. Writing to command register 66h will load data into the TX FIFO and reading from command register 77h will read data from the RX FIFO. The TX FIFO has a threshold for when the FIFO is almost empty which is set by the "TX_FIFO_EMPTY" property. An interrupt event occurs when the data in the TX FIFO reaches the almost empty threshold. If more data is not loaded into the FIFO then the chip automatically exits the TX State after the ipksent interrupt occurs. The RX FIFO has one programmable threshold which is programmed by setting the "RX_FIFO_FULL" property. When the incoming RX data crosses the Almost Full Threshold an interrupt will be generated to the microcontroller via the nIRQ pin. The microcontroller will then need to read the data from the RX FIFO. Both the TX and RX FIFOs may be cleared or reset with the "FIFO_RESET" command.

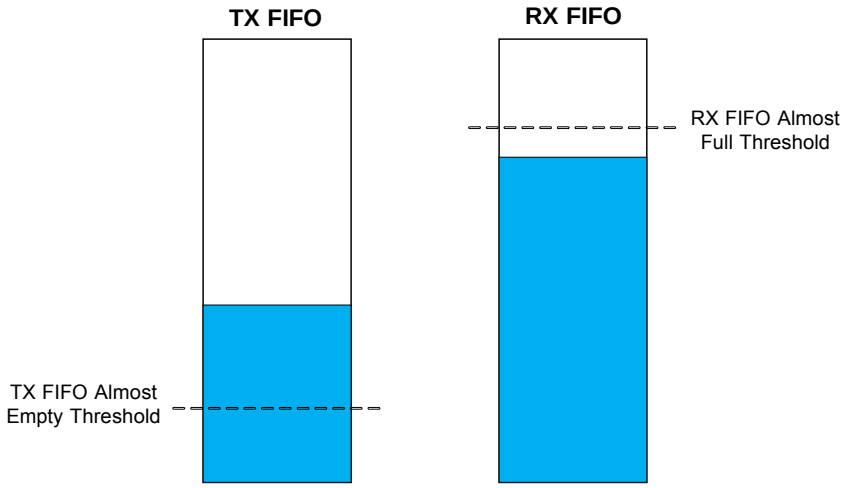

Figure 11. TX and RX FIFOs

6.2. Packet Handler

When using the FIFOs, automatic packet handling may be enabled for TX mode, RX mode, or both. The usual fields for network communication (such as preamble, synchronization word, headers, packet length, and CRC) can be configured to be automatically added to the data payload. The fields needed for packet generation normally change infrequently and can therefore be stored in registers. Automatically adding these fields to the data payload in TX mode and automatically checking them in RX mode greatly reduces the amount of communication between the microcontroller and Si446x. It also greatly reduces the required computational power of the microcontroller. The general packet structure is shown in Figure 12. Any or all of the fields can be enabled and checked by the internal packet handler. The Header/Frame/Length section is entirely configurable to almost any packet configuration with the match/value configuration properties. Reference designs and examples are available for 15.4g and MBUS packet structures.

Figure 12. Packet Handler Structure

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7. RX Modem Configuration

The RFM24W can easily be configured for different datarate, deviation, frequency, etc. by using the WDS settings calculator which will generate an initialization file to be used by the host MCU.

8. Auxiliary Blocks

8.1. Temperature Sensor

8.2. Low Battery Detector

8.3. Wake-up Timer and 32 kHz Clock Source

8.4. Low Duty Cycle Mode (Auto RX Wake-Up)

8.5. Antenna Diversity

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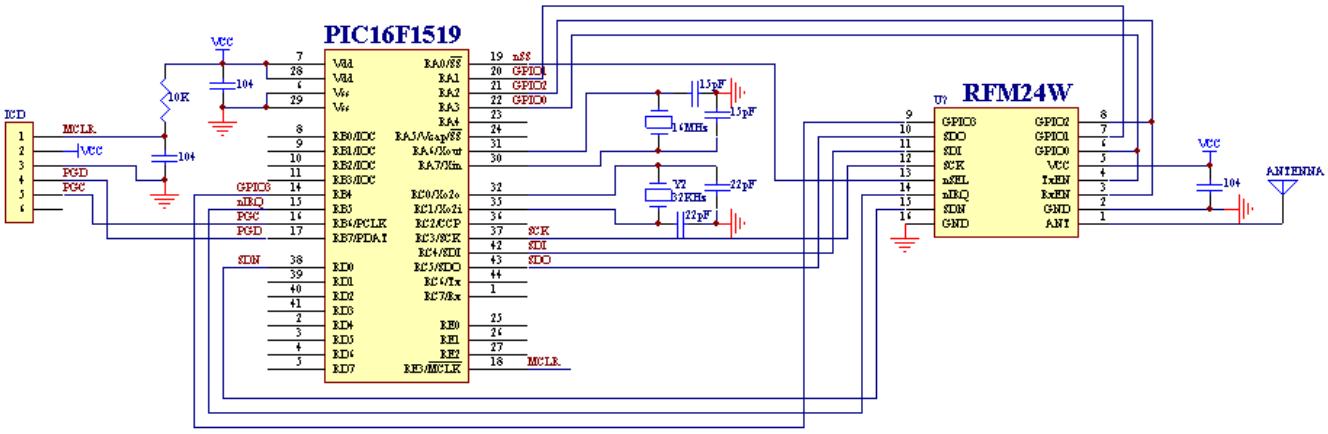
9. Reference Design



RFM24W Reference Design Schematic 1

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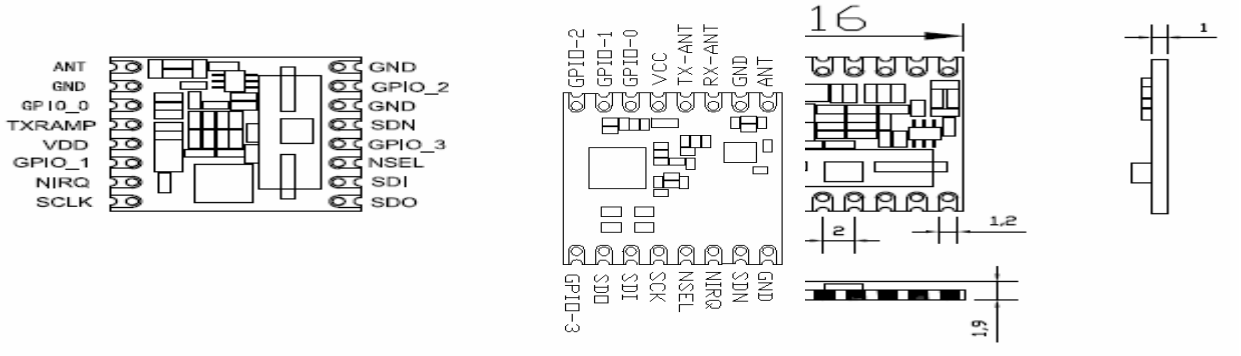
10. Pin Descriptions

RFM24W-S2



Pin Name	I/0	Description
GND	GND	Connect to PCB ground.
SDN	I	**Shutdown Input Pin**. 0–VCC V digital input. SDN should be = 0 in all modes except Shutdown mode. When SDN =1 the chip will be completely shutdown and the contents of the registers will be lost.
NIRQ	I	**General Microcontroller Interrupt Status Output.** When the Si4463/62/61 exhibits anyone of the interrupt events the nIRQ pin will be set low=0. The Microcontroller can then determine the state of the interrupt by reading the interrupt status. No external resistor pull-up is required
NSEL	I	**Serial Interface Select Input.** 0–VCC V digital input. This pin provides the Select/Enable function for the 4-line serial data bus.
SCK	I	**Serial Clock Input.** 0–VCC V digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the Si4463/62/61 on positive
SDI	I	**Serial Data Input.** 0–VCC V digital input. This pin provides the serial data stream for the 4-line serial data bus.
SDO	O	**0–VCC V Digital Output.** Provides a serial readback function of the internal control registers.

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GPIO_3	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions includ ing: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc.
GPIO_2	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions includ ing: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc.
GPIO_1	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions includ-ing: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc.
GPIO_0	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions includ-ing: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc.
TX-ANT	I	Tx Atenna select input pin ,when RFM24W is in Tx state,the pin should be low,and RX-ANT should be high.
RX-ANT	I	Rx Atenna select input pin ,when RFM24W is in Rx state,the pin should be low,and TX-ANT should be high.
ANT	ANT	RF signal output/input.

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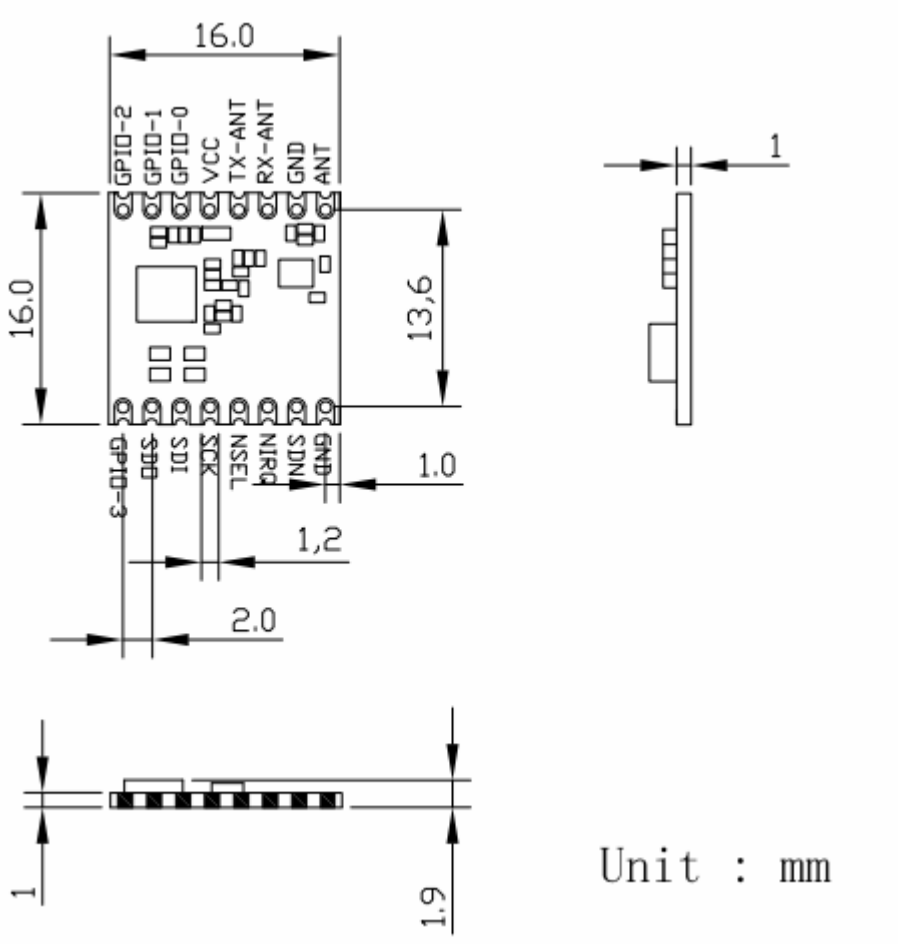
11. Mechanical Dimension:RFM24W

SMD PACKAGE(S2)



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12. Ordering Information

Part Number=module type—operation band—package type

RFM24W—433—S2

module type operation band Package

example：1，RFM24W module at 433MHz band, SMD : RFM24W-433-S2

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