

15A, 50V and 60V, 0.140 Ohm, Logic Level N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA0522.

Ordering Information

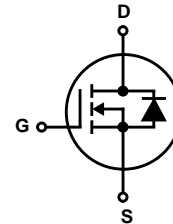
PART NUMBER	PACKAGE	BRAND
RFP15N05L	TO-220AB	RFP15N05L
RFP15N06L	TO-220AB	RFP15N06L

NOTE: When ordering, use the entire part number.

Features

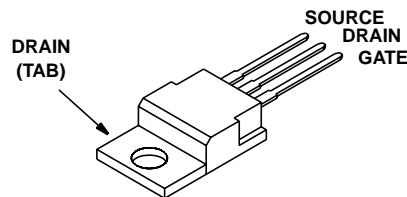
- 15A, 50V and 60V
- $r_{DS(ON)} = 0.140\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



RFP15N05L, RFP15N06L

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFP15N05L	RFP15N06L	UNITS	
Drain to Source Voltage (Note 1)	V_{DSS}	50	60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	50	60	V
Continuous Drain Current	I_D	15	15	A
Pulsed Drain Current (Note 3)	I_{DM}	40	40	A
Gate to Source Voltage	V_{GS}	± 10	± 10	V
Maximum Power Dissipation	P_D	60	60	W
Above $T_C = 25^\circ\text{C}$, Derate Linearly		0.48	0.48	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering				
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFP15N05L	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	50	-	-	V
			RFP15N06L	60	-	-
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 7)	1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48\text{V}, V_{GS} = 50\text{V}$	-	-	1	μA
		$V_{DS} = 48\text{V}, V_{DS} = 50\text{V}$ $T_C = 125^\circ\text{C}$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10\text{V}, V_{DS} = 0\text{V}$	-	-	100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 15\text{A}, V_{GS} = 5\text{V}$ (Figures 5, 6)	-	-	0.140	Ω
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ (Figure 8)	-	-	900	pF
Output Capacitance	C_{OSS}		-	-	450	pF
Reverse-Transfer Capacitance	C_{RSS}		-	-	200	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 30\text{V}, I_D = 7.5\text{A}, R_G = 6.25\Omega$ (Figures 10, 11)	-	16	40	ns
Rise Time	t_r		-	250	325	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	200	325	ns
Fall Time	t_f	$V_{GS} = 5\text{V}$	-	225	325	ns
	$R_{\theta JC}$	RFP15N05L, RFP15N06L	-	-	2.083	$^\circ\text{C}/\text{W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 7.5\text{A}$	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 4\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	225	-	ns

NOTE:

2. Pulsed: pulse duration = $\leq 300\mu\text{s}$ maximum, duty cycle = $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

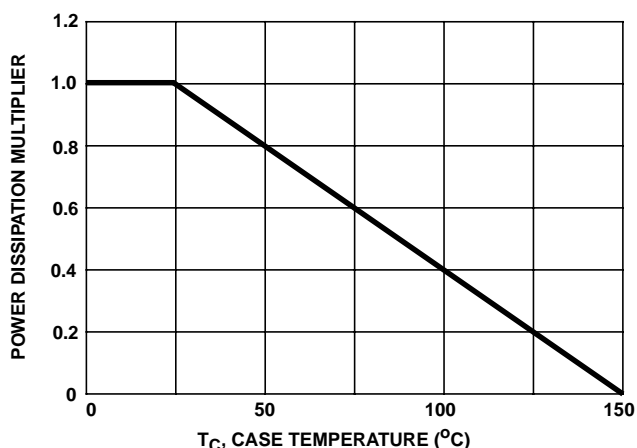


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

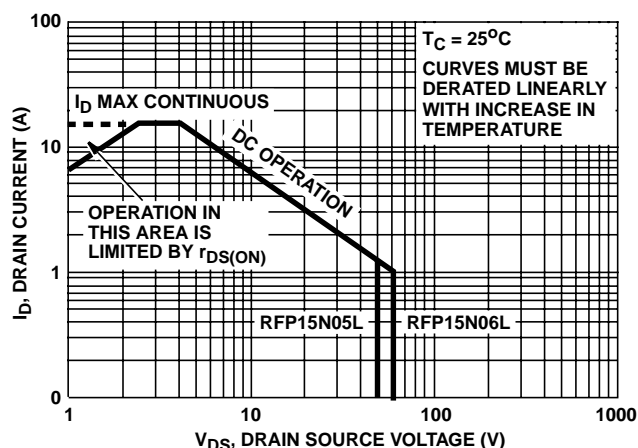


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

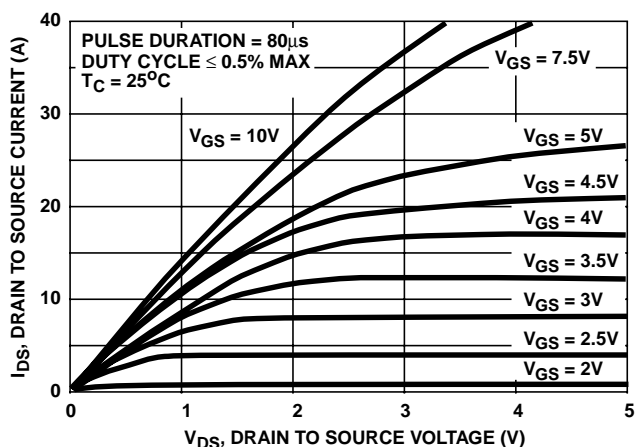


FIGURE 3. SATURATION CHARACTERISTICS

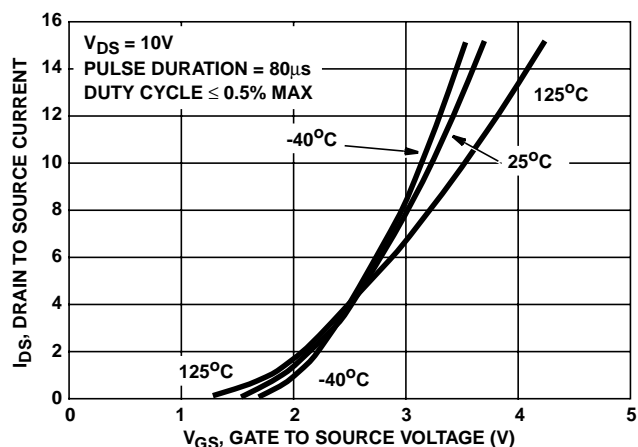


FIGURE 4. TRANSFER CHARACTERISTICS

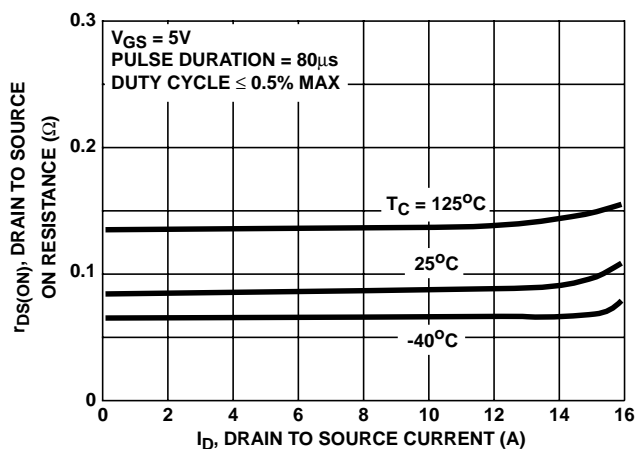


FIGURE 5. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

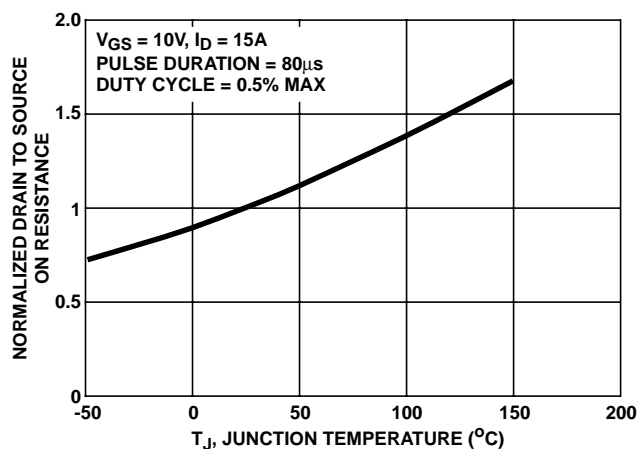


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

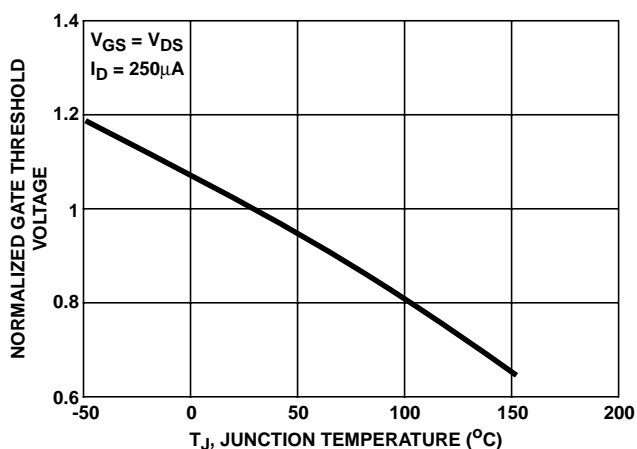


FIGURE 7. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

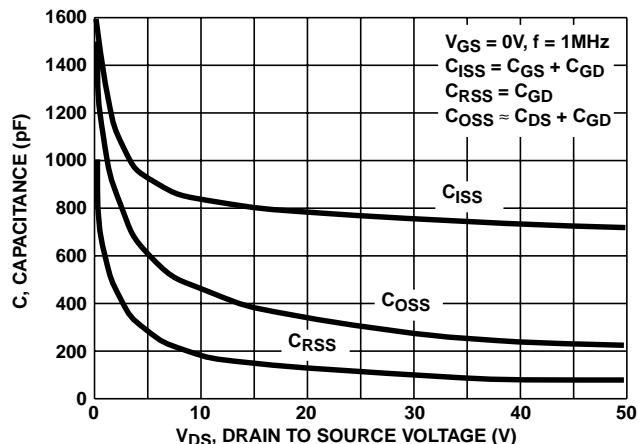
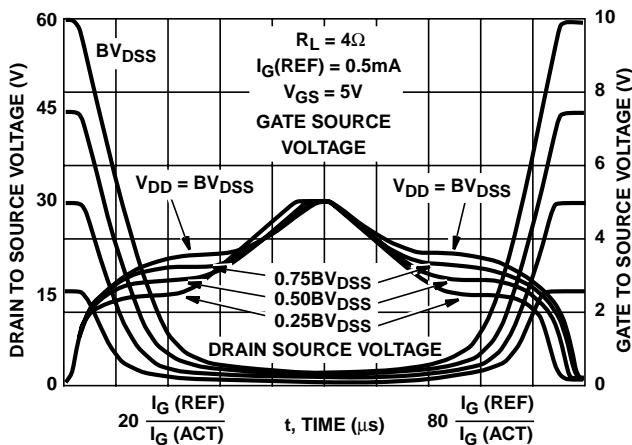


FIGURE 8. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 9. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

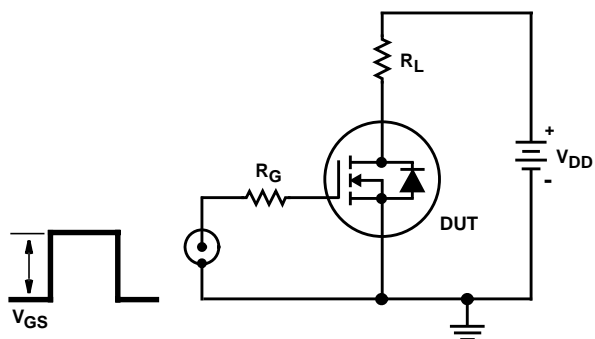


FIGURE 10. SWITCHING TIME TEST CIRCUIT

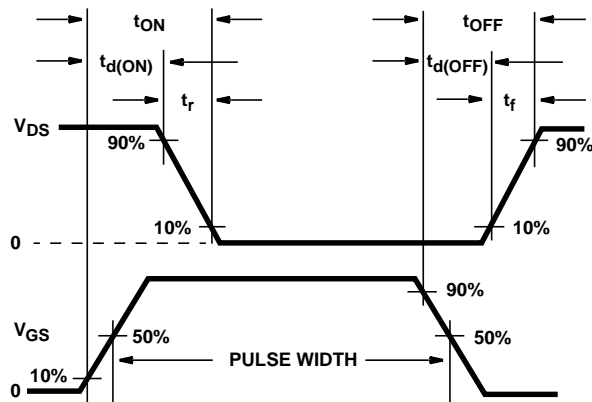


FIGURE 11. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

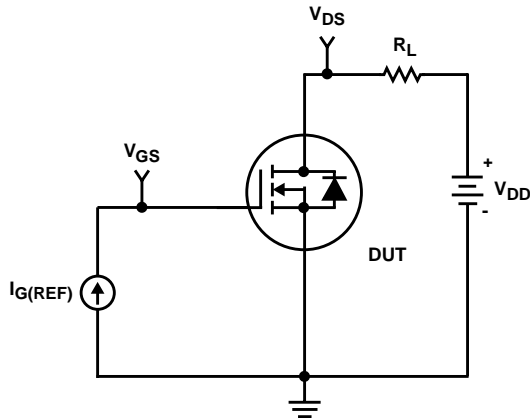


FIGURE 12. GATE CHARGE TEST CIRCUIT

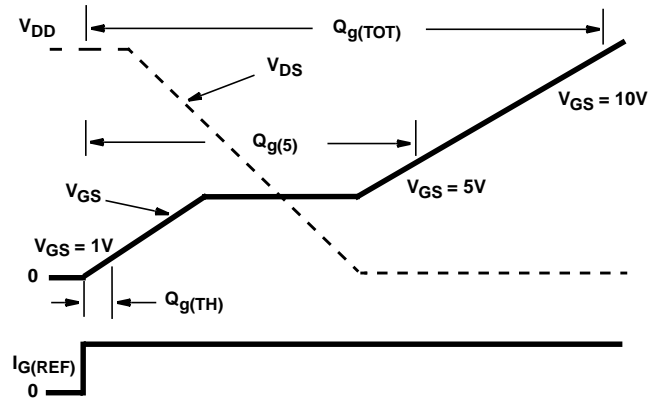


FIGURE 13. GATE CHARGE WAVEFORMS

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Sales Office Headquarters

NORTH AMERICA
 Intersil Corporation
 P. O. Box 883, Mail Stop 53-204
 Melbourne, FL 32902
 TEL: (407) 724-7000
 FAX: (407) 724-7240

EUROPE
 Intersil SA
 Mercure Center
 100, Rue de la Fusee
 1130 Brussels, Belgium
 TEL: (32) 2.724.2111
 FAX: (32) 2.724.22.05

ASIA
 Intersil (Taiwan) Ltd.
 7F-6, No. 101 Fu Hsing North Road
 Taipei, Taiwan
 Republic of China
 TEL: (886) 2 2716 9310
 FAX: (886) 2 2715 3029