RFP70N03, RF1S70N03, RF1S70N03SM

70A, 30V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- **70A, 30V**
- **$r_{DS(ON)}$ = 0.010Ω**
- ***Temperature Compensating* PSPICE Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve (Single Pulse)**
- **+175°C Operating Temperature**

Description

The RFP70N03, RF1S70N03, and RF1S70N03SM N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

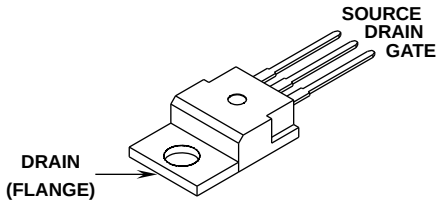
PART NUMBER	PACKAGE	BRAND
RFP70N03	TO-220AB	RFP70N03
RF1S70N03	TO-262AA	F1S70N03
RF1S70N03SM	TO-263AB	F1S70N03

NOTE: When ordering use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, e.g. RF1S70N03SM9A.

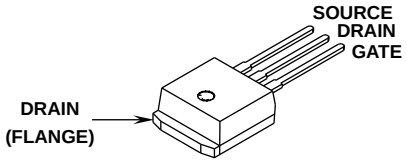
Formerly developmental type TA49025.

Packages

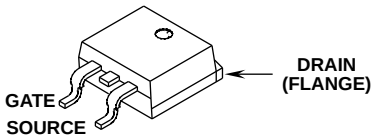
JEDEC TO-220AB



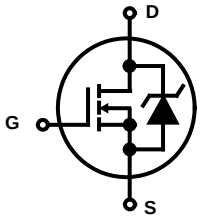
JEDEC TO-262AA



JEDEC TO-263AB



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RFP70N03, RF1S70N03, RF1S70N03SM	UNITS
Drain-Source Voltage	V_{DSS}	30	V
Drain-Gate Voltage	V_{DGR}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current			
RMS Continuous	I_D	70	A
Pulsed Drain Current	I_{DM}	200	A
Single Pulse Avalanche Rating	E_{AS}	(Refer to UIS Curve)	
Power Dissipation			
T_C = +25°C	P_D	150	W
Above T_C = +25°C, Derate Linearly	P_T	1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3404.2**

Electrical Specifications

At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V	T_C = 25°C	-	-	1	μA
		V_{GS} = 0V	T_C = 150°C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 70A, V_{GS} = 10V		-	-	0.010	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D = 70A		-	-	80	ns
Turn-On Delay Time	$t_{D(ON)}$	R_L = 0.214Ω, V_{GS} = +10V		-	20	-	ns
Rise Time	t_R	R_{GS} = 2.5Ω		-	20	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	40	-	ns
Fall Time	t_F			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to 20V	V_{DD} = 24V, I_D = 70A, R_L = 0.343Ω	-	215	260	nC
Gate Charge at 10V	$Q_{G(10)}$	V_{GS} = 0 to 10V		-	120	145	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to 2V		-	6.5	8.0	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V		-	3300	-	pF
Output Capacitance	C_{OSS}	f = 1MHz		-	1750	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	750	-	pF
Thermal Resistance Junction to Case	$R_{θJC}$			-	-	1.0	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{θJA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 70A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 70A, dI_{SD}/dt = 100A/μs	-	-	125	ns

Typical Performance Curves

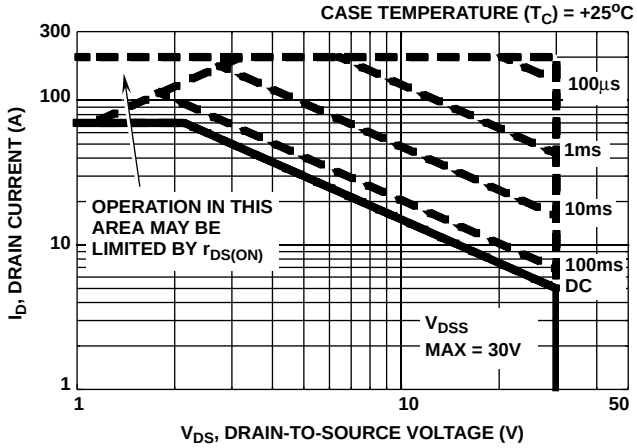


FIGURE 1. SAFE-OPERATING AREA CURVE

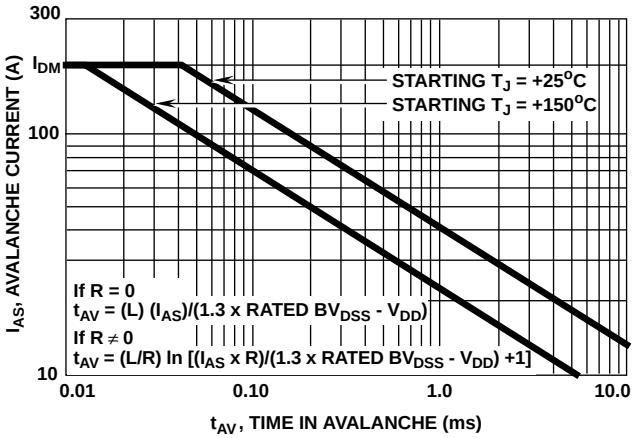


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

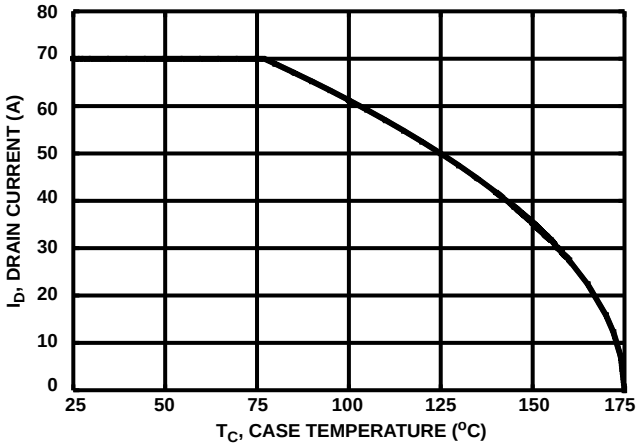


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

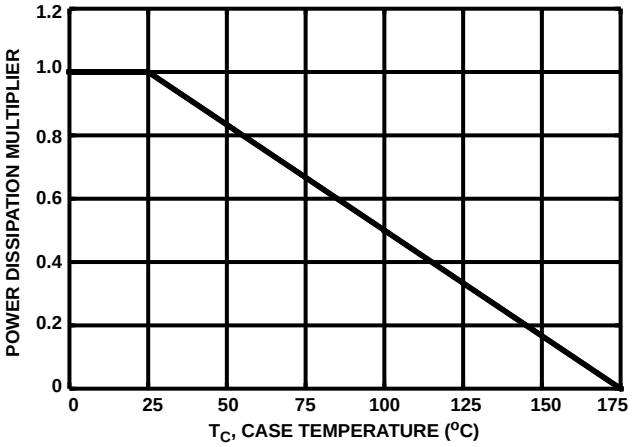


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

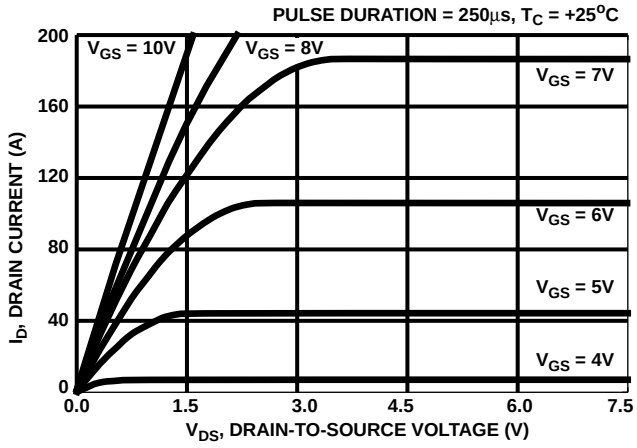


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

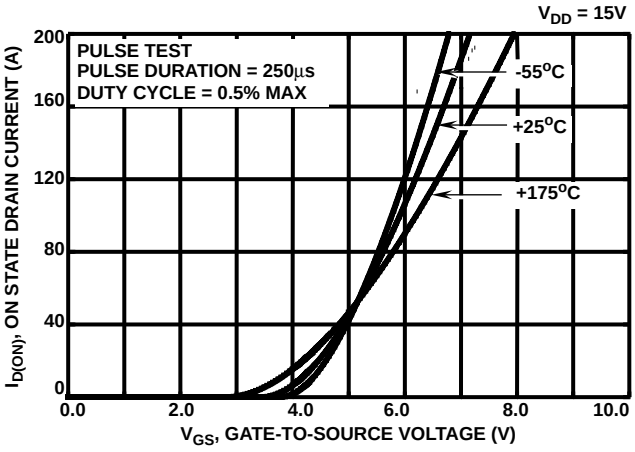


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

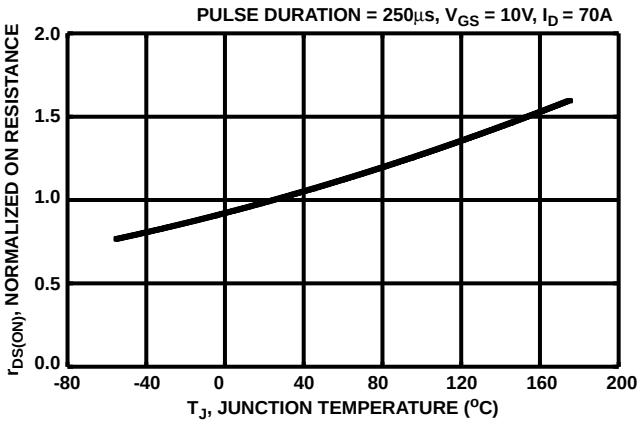


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

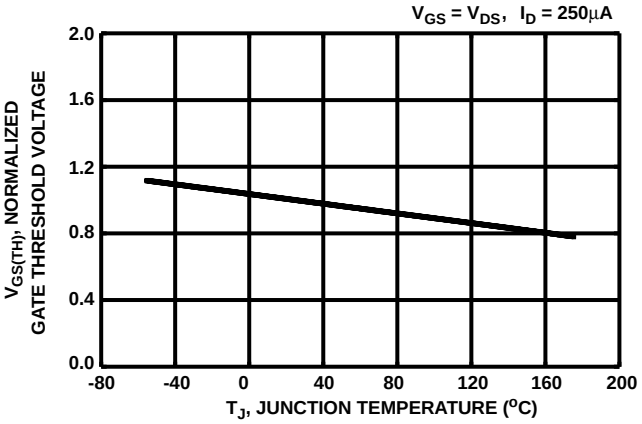


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

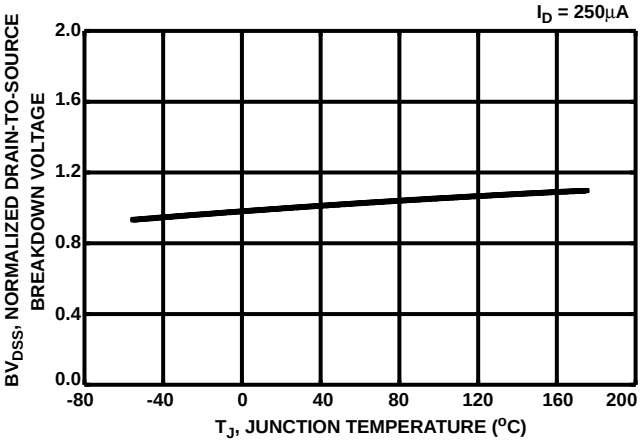


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

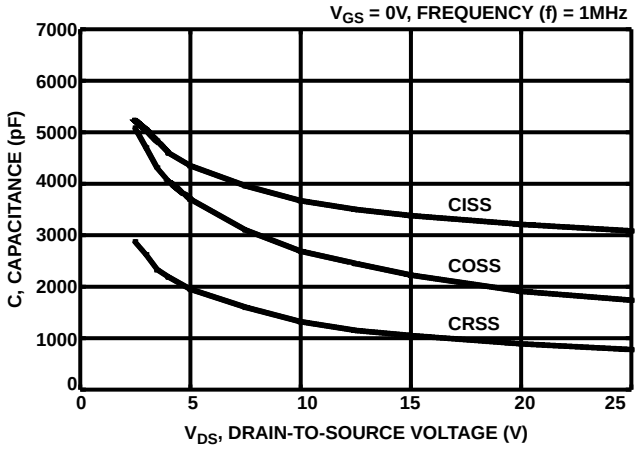


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

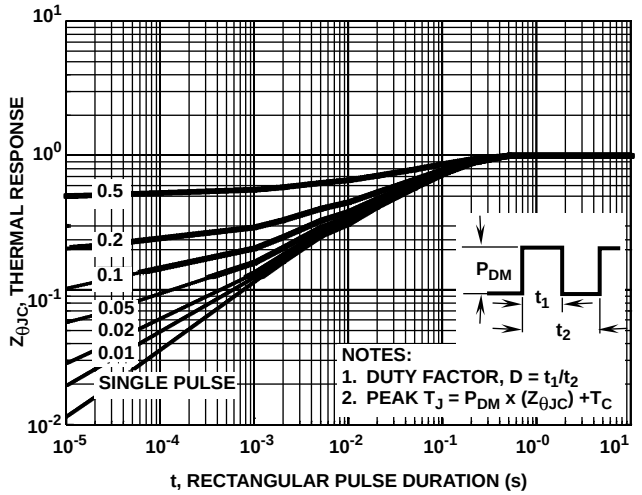


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

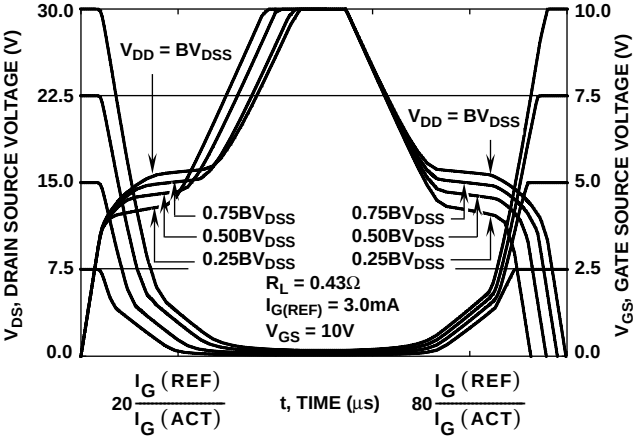


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Test Circuits and Waveforms

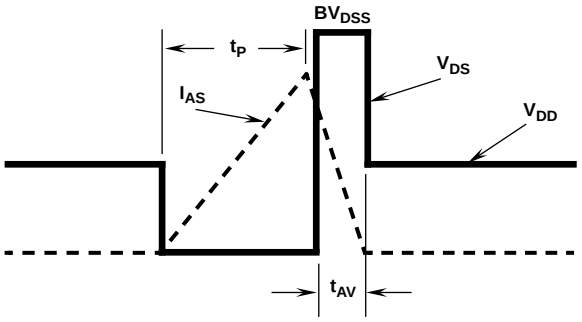


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

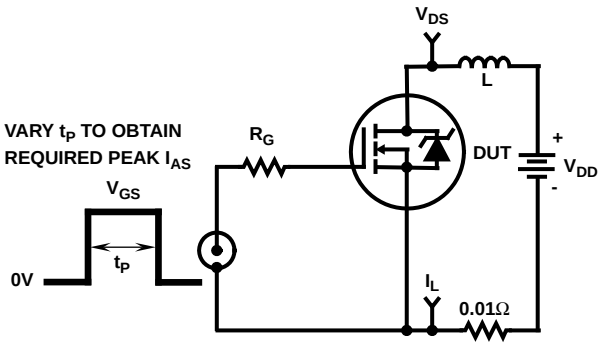


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

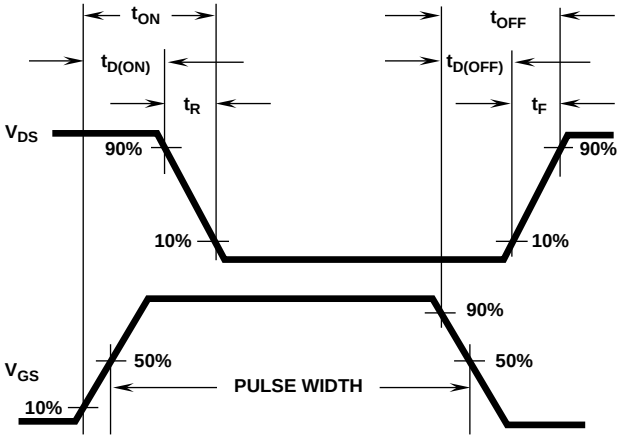


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

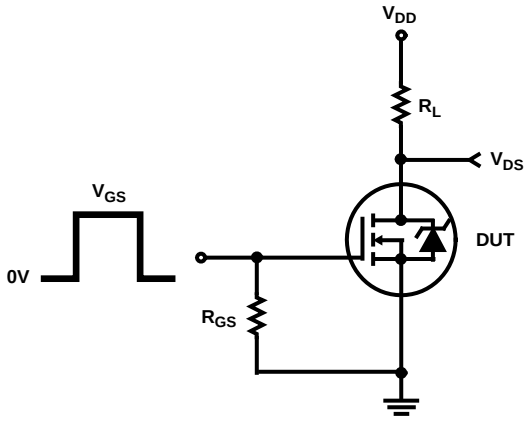


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

PSPICE Model for the RFP70N03, RF1S70N03, RF1S70N03SM

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.SUBCKT RFP70N03 2 1 3 ;          rev 9/16/92
*NOM TEMP = 25°C


CA 12 8 6.09e-9
CB 15 14 6.05e-9
CIN 6 8 3.40e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.10e-9
LSOURCE 3 7 1.82e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 30.7e-6
RGATE 9 20 0.890
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.92e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.605

.MODEL DBDMOD D (IS=7.91e-12 RS=3.87e-3 TRS1=2.71e-3 TRS2=2.50e-7 CJO=4.84e-9 TT=4.51e-8)
.MODEL DBKMOD D (RS=3.9e-2 TRS1=1.05e-4 TRS2=3.11e-5)
.MODEL DPLCAPMOD D (CJO=4.8e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.46 KP=47 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=8.46e-4 TC2=-8.48e-7)
.MODEL RDSMOD RES (TC1=2.23e-3 TC2=6.56e-6)
.MODEL RVTOMOD RES (TC1=-3.29e-3 TC2=3.49e-7)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-8.35 VOFF=-6.35)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.35 VOFF=-8.35)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=3.0)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.0 VOFF=-2.0)

.ENDS
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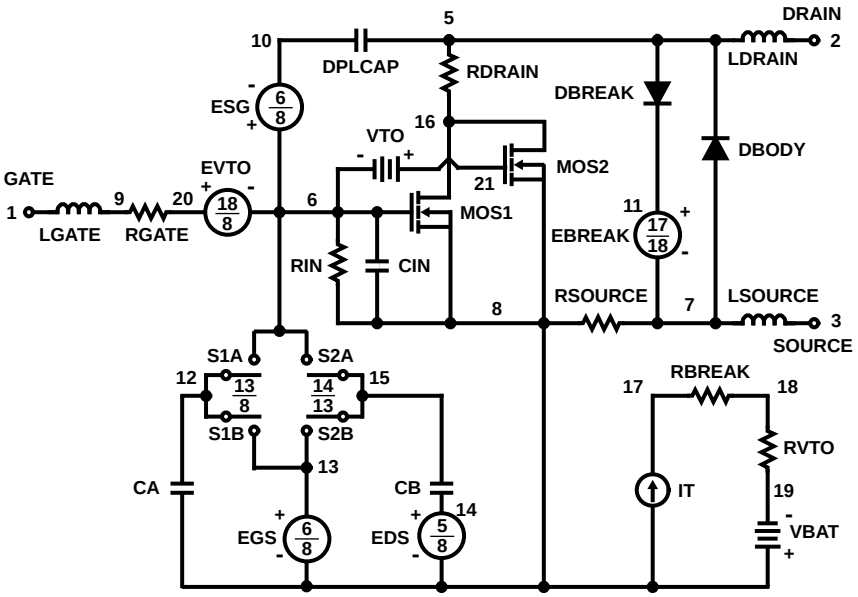

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.