

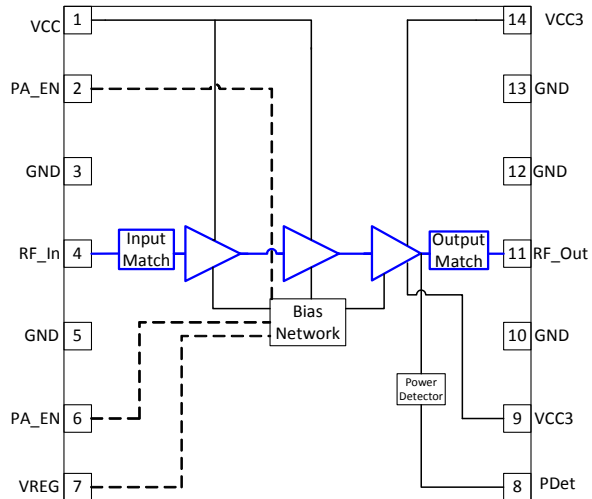


### Features

- $P_{OUT} = 29\text{dBm}$ ; EVM = 3%; 11n MCS7 HT40
- Input and Output Matched to  $50\Omega$
- High Gain: 33.5dB
- Integrated Power Detector
- High Impedance Enable Pin
- High PAE Design

### Applications

- IEEE 802.11b/g/n WiFi Systems
- Customer Premise Equipment (CPE)
- Wireless Access Points, Gateways & Router Applications
- ISM Band Transmitter Applications



Functional Block Diagram

### Product Description

The RFPA5201 is a highly integrated Power Amplifier Module (PAM) designed for high performance WiFi requiring up to +29dBm linear output power. This PAM is manufactured on an advanced RFMD InGaP Hetero-junction Bipolar Transistor (HBT) process.

The PAM is packaged in a 14-pin, 7mm x 7mm Multi-Chip Module (MCM) with an integrated power detector, biasing and input/output matching components. The RFPA5201 is designed to exceed system efficiency targets at +29dBm linear output power while meeting 802.11n dynamic Error Vector Magnitude (EVM) specifications. This solution provides a high performance, highly integrated solution with minimal external components.

### Ordering Information

RFPA5201PCK-410	RFPA5201 Eval Board with 5-piece bag
RFPA5201SB	5-Piece Bag
RFPA5201SR	100-Piece Reel
RFPA5201TR13	2500-Piece Reel
RFPA5201SQ	25-Piece Bag

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF Applied)	-0.5 to +5.5	V
Supply Voltage (No RF Applied)	-0.5 to +6.0	V
DC Supply Current	1800	mA
Input RF Power with 50Ω Output Load	10	dBm
Maximum VSWR with no damage	10:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
MSL	3	



### Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Typical Conditions</b>					$V_{CC} = 5.0V$ , $V_{REG} = 2.9V$ , 11n MCS7 HT20 and HT40 65Mbps, temperature = 25 °C, unless otherwise noted
Tx Performance - 11g/n					Compliance with standard 802.11g/n
Frequency	2412		2484	MHz	
802.11n Output Power		29		dBm	802.11n HT20 and HT40 MCS7
11n Dynamic EVM		2.5	3	%	
Second Harmonic		-20	-16	dBm/MHz	At rated $P_{OUT}$
Third Harmonic		-48	-45	dBm/MHz	
Gain	31.5	33.5		dB	
Gain Variation			+/-1	dB	over frequency
			+/-2.5	dB	Over temperature of -40 °C to +85 °C
Power Detect Range	0.1		2.2	V	$P_{OUT} = 0dBm$ to 30dBm
Power Detect Voltage	1.8	1.9	2.0	V	At rated $P_{OUT}$
Input Return Loss		-15	-12	dB	In specified frequency band
Output Return Loss		-10	-8	dB	
Operating Current		850	975	mA	At rated $P_{OUT}$
Quiescent Current		350	425	mA	$V_{CC} = 5.0$ , $V_{REG} = PA\_EN = 2.9V$ and RF = OFF
PAE (Power Added Efficiency)		18.5		%	At rated $P_{OUT}$ (PA only)
Power Down Current		16		mA	$PA\_EN = 0V$ , $V_{CC} = 5V$ , $V_{REG} = 2.9V$
$I_{REG}$		12	15	mA	$V_{CC} = 5V$ , $PA\_EN = 2.9V$ , $V_{REG} = 2.9V$
Leakage Current		0.5	0.7	mA	$V_{CC} = 5V$ , $V_{REG} = 0V$ , $PA\_EN = 0V$
Power Supply - $V_{CC}$		5	5.25	V	
$V_{REG}$ Voltage (at $V_{REG}$ pin of Eval board)	2.85	2.9	3.0	V	
Turn-on time from setting of $V_{REGS}$			1	μsec	Output stable to within 90% of final gain
Turn-off time from setting of $V_{REGS}$			1	μsec	
Stability	-25		33	dBm	No spurs above -47dBm into 4:1 VSWR
Output P1dB		35		dBm	CW signal

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Generic Performance					Compliance with standard 802.11g/n
ESD					
Human Body Model	500			V	EIA/JESD22-114A all pins
Charge Device Model	1000			V	JESD22-C101C all pins
Thermal Resistance					
Theta_JC		13		°C/W	P <sub>OUT</sub> - 29dBm; duty cycle - 90%; V <sub>CC</sub> = 5V; V <sub>REG</sub> = 2.90V; junction to bottom of laminate package; T <sub>REF</sub> = 85 °C
Theta_J-REF		18		°C/W	P <sub>OUT</sub> - 29dBm; duty cycle - 90%; V <sub>CC</sub> = 5V; V <sub>REG</sub> = 2.90V; junction to bottom of PCB; T <sub>REF</sub> = 85 °C
Maximum Junction Temperature for Long Term Reliability					
T <sub>Jmax</sub>		175		°C	P <sub>OUT</sub> - 29dBm; V <sub>CC</sub> = 5V; V <sub>REG</sub> = 2.90V; T <sub>REF</sub> = 85 °C

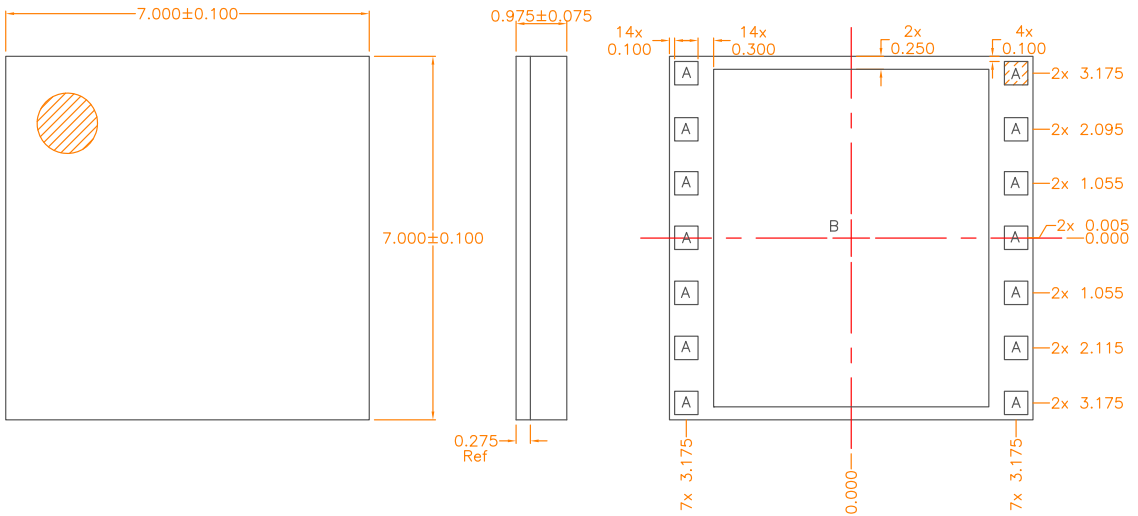
## Pin Names and Descriptions

Pin	Name	Description
1	VCC	This pin is connected internally to the collectors of RF device. To achieve specified performance, the layout of the pin should match the Recommended Land Pattern.
2	PA_EN	High Impedance enable pin, Apply < 0.6VDC to power down the PA. Apply 1.75VDC to 5VDC to enable the PA.
3	GND	Ground connection.
4	RF_IN	RF input, is internally matched to 50Ω. DC Blocked
5	GND	Ground connection.
6	PA_EN	High Impedance enable pin, Apply < 0.6VDC to power down the PA. Apply 1.75VDC to 5VDC to enable the PA.
7	VREG	PA bias voltage. This pin requires regulated supply for best performance.
8	PDET	Power detector provides an output voltage proportional to the RF output power level.
9	VCC3	This pin is connected internally to the collectors of RF device. To achieve specified performance, the layout of the pin should match the Recommended Land Pattern
10	GND	Ground connection.
11	RFOUT	RF output, is internally matched to 50Ω. DC Blocked
12	GND	Ground connection.
13	GND	Ground connection.
14	VCC3	This pin is connected internally to the collectors of RF device. To achieve specified performance, the layout of the pin should match the Recommended Land Pattern
Pkg Base	GND	Ground connection. The back side of the package should be connected to the ground plane through as short connection as possible, e.g., PCB vias under the device are recommended.

**Pin Out**

1	VCC	VCC3	14
2	PA_EN	GND	13
3	GND	GND	12
4	RF_In	RF_Out	11
5	GND	GND	10
6	PA_EN	VCC3	9
7	VREG	PDet	8

## Package Drawing

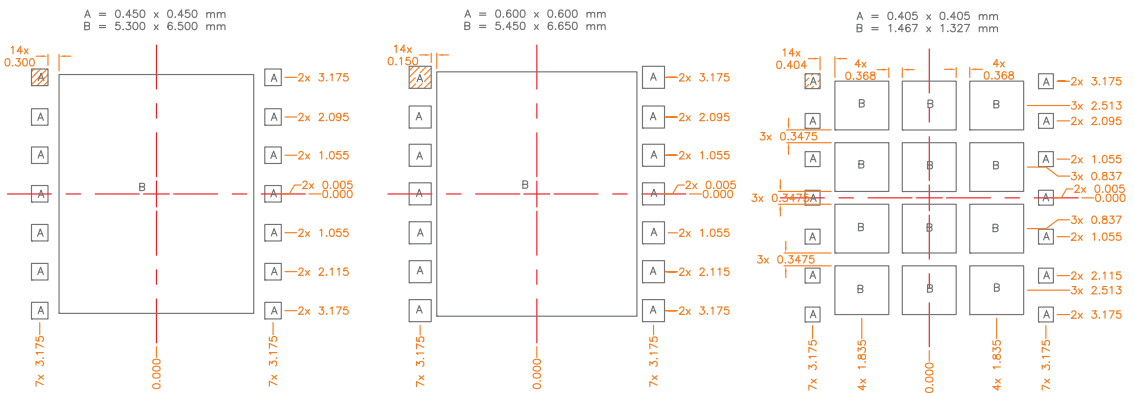


A = 0.450 x 0.450 mm  
B = 5.300 x 6.500 mm

### Notes

1. Shaded area represents Pin 1 location.
2. Thermal vias for center slug "B" should be incorporated into the PCB design. The number and size of thermal vias will depend on the application. Example of the number and size of vias can be found on the RFMD evaluation board layout.

## PCB Pattern



PCB Metal Land Pattern

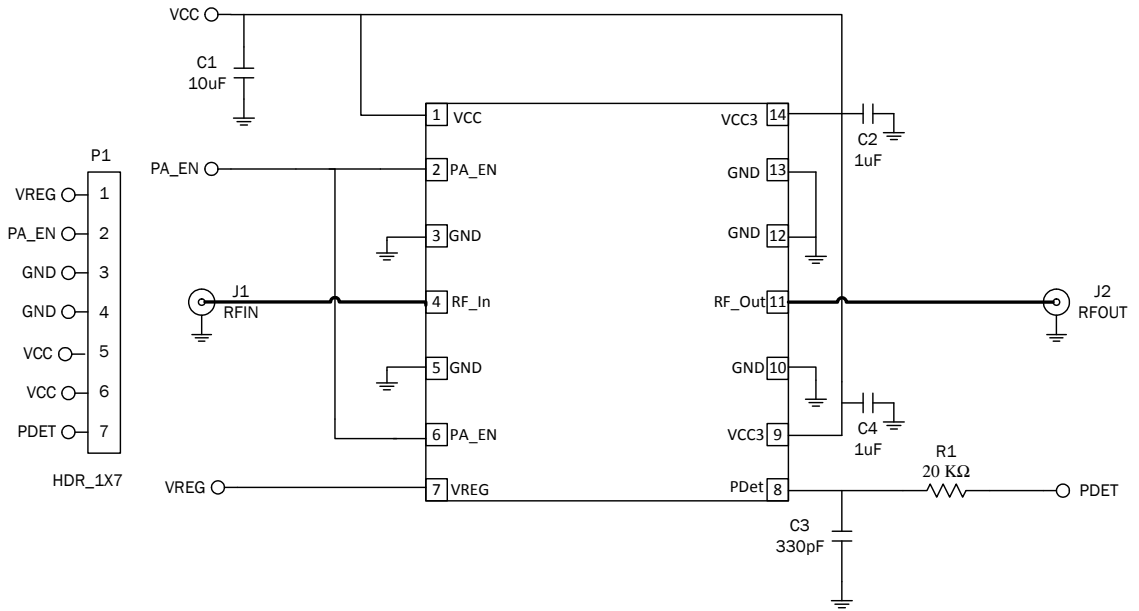
PCB Solder Mask Pattern

PCB Stencil Pattern

### Notes:

1. Shaded area represents Pin 1 location.

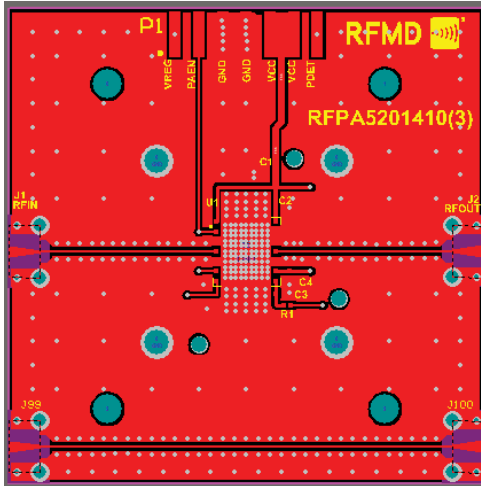
**Evaluation Board Schematic**



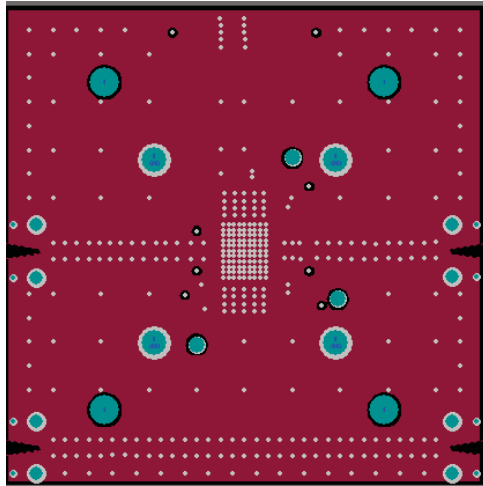
## RFPA5201 Evaluation Board Layers

(2 x 2 x 0.034in ±10%; FR4, 6mils thick top dielectric)

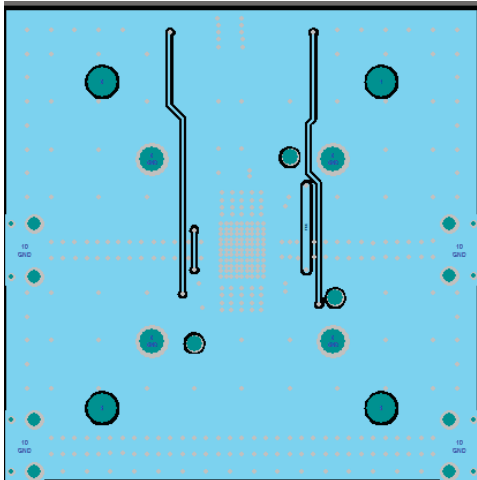
TOP



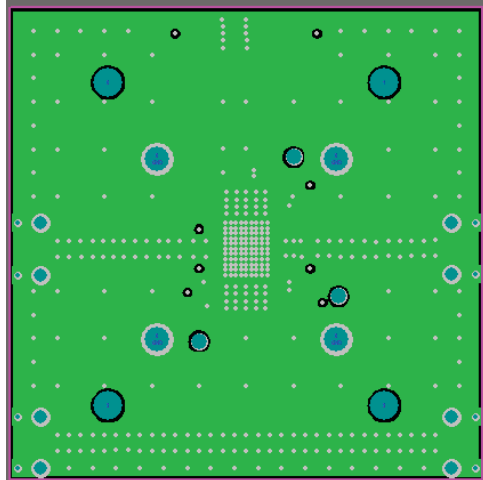
MID-1



MID-2



BOTTOM

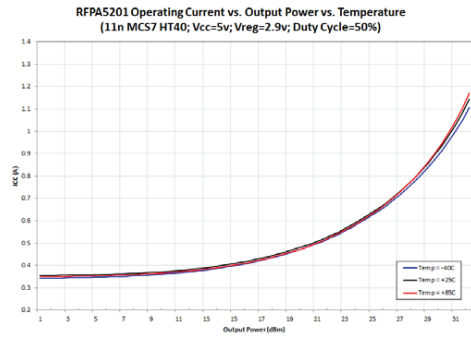
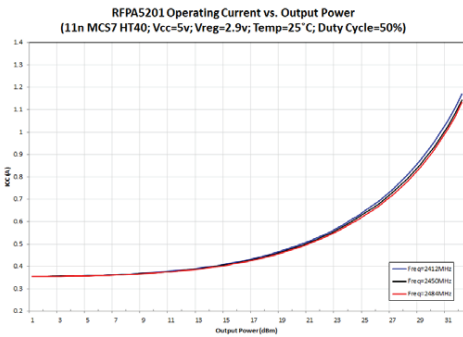
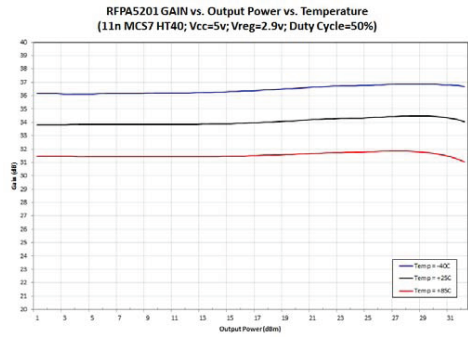
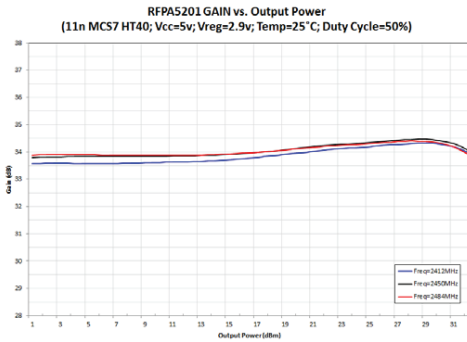
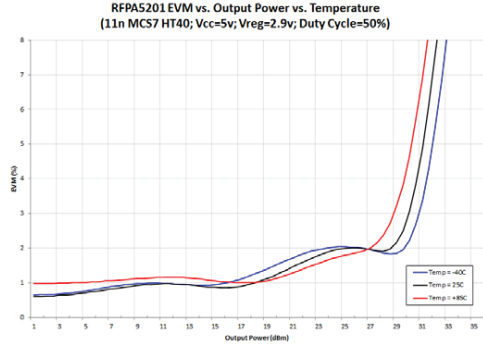
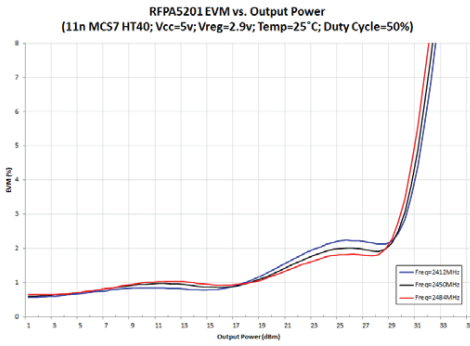


Note: Gerber files available upon request.



**RFP5201 Performance Plots**

(11n MCS& HT40;  $V_{CC} = 5V$ ;  $V_{REG} = 2.9V$ ; Temp = 25°C; Duty Cycle = 50%)



## RFPA5201 Performance Plots (continued)

(1.1n MCS7 HT40;  $V_{CC} = 5V$ ;  $V_{REG} = 2.9V$ ; Temp = 25°C; Duty Cycle = 50%)

