

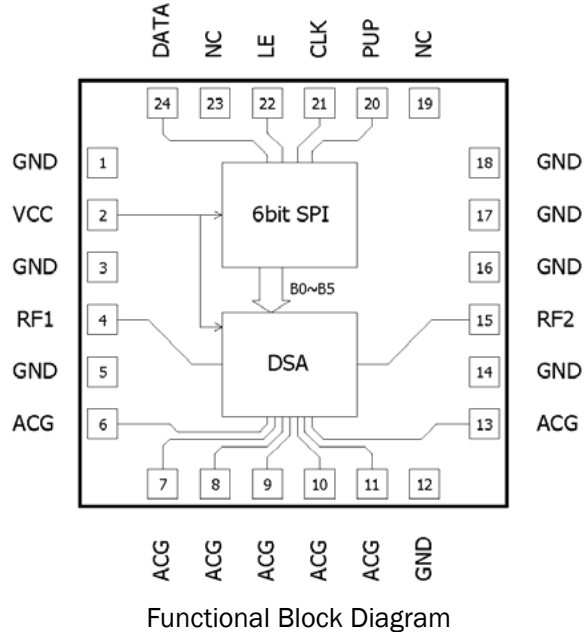


### Features

- Frequency Range 50MHz to 4000MHz
- 6-Bits, 31.5dB Range, 0.5dB Step
- High Linearity, OIP3 > 48dBm through over 700MHz to 2700MHz
- 3V and 5V Logic Compatible
- Serial-to-Parallel Controller
- Serial Programming Interface
- Power-up Programming Modes
- On-chip ESD Protection > 500V HBM
- Single Supply, 3V to 5V Operation
- Footprint compatible with most 24-pin, 4mm QFNs

### Applications

- Transceiver IF Applications
- Cellular, PCS, GSM, UMTS, LTE, WiMax/WLAN
- Wireless Data, Satellite Terminals
- Test Equipment



### Product Description

RFMD's RFSA2624 is a 6-bit Digital Step Attenuator (DSA) that features high linearity over the entire 31.5dB gain control range with excellent step accuracy in 0.5dB steps. The RFSA2624 is programmed via a serial mode control interface that is both 3V and 5V compatible. The RFSA2624 also offers a rugged Class 1B HBM ESD rating via on-chip ESD circuitry. The MCM package is footprint compatible with most 24-pin, 4mm, QFN packages.

### Ordering Information

RFSA2624SR	7" Reel with 100 pieces
RFSA2624SQ	Sample bag with 25 pieces
RFSA2624TR7	7" Reel with 750 pieces
RFSA2624TR13	13" Reel with 2500 pieces
RFSA2624PCK-410	50MHz to 4000MHz PCBA with 5-piece sample bag

### Optimum Technology Matching® Applied

- |                                      |                                      |  |                                    |
|--------------------------------------|--------------------------------------|--|------------------------------------|
| <input type="checkbox"/> GaAs HBT    | <input type="checkbox"/> SiGe BiCMOS | <input checked="" type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT  |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS   | <input checked="" type="checkbox"/> Si CMOS    | <input type="checkbox"/> BiFET HBT |
| <input type="checkbox"/> InGaP HBT   | <input type="checkbox"/> SiGe HBT    | <input type="checkbox"/> Si BJT                | <input type="checkbox"/> LDMOS     |

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	+5.5	V
DC Supply Current	15	mA
Power Dissipation	83	mW
Max RF Input Power	27	dBm
Operating Temperature (T <sub>CASE</sub> )	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Junction Temperature	150	°C
ESD Rating (HBM)	Class 1B	
Moisture Sensitivity Level	MSL3	



**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

The information in this publication is believed to be accurate and reliable. However, no responsibility is assumed by RF Micro Devices, Inc. ("RFMD") for its use, nor for any infringement of patents, or other rights of third parties, resulting from its use. No license is granted by implication or otherwise under any patent or patent rights of RFMD. RFMD reserves the right to change component circuitry, recommended application circuitry and specifications at any time without prior notice.

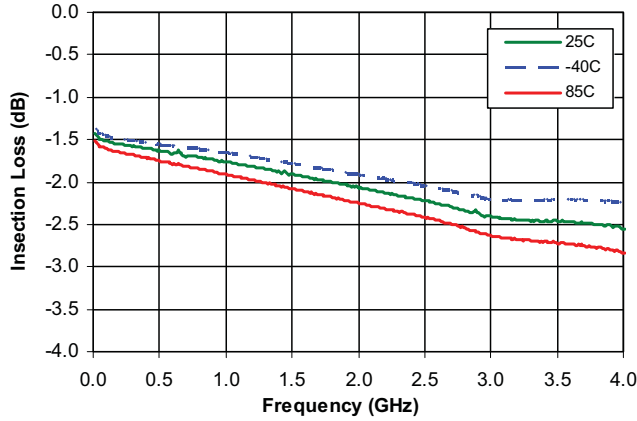
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency Range	50		4000	MHz	
Insertion Loss		1.5		dB	150MHz, 0dB attenuation
		1.7	1.9	dB	850MHz, 0dB attenuation
		2.3		dB	2700MHz, 0dB attenuation
		2.5	2.8	dB	3800MHz, 0dB attenuation
Gain Control Range		31.5		dB	0.5dB step size
Step Accuracy	±(0.15 + 5.0% attenuation setting)			dB	
Input IP3 (0 - 15.5dB states)		48		dBm	700MHz to 2700MHz, all states
Input P1dB		27		dBm	700MHz to 2700MHz, all states
Return Loss		13		dB	700MHz to 2700MHz, all states
Control Interface		6		bit	Serial Interface
Settling Time		250		nS	t <sub>RISE</sub> , t <sub>FALL</sub> (10%/90% RF)
Switching Speed		250		nS	t <sub>ON</sub> , t <sub>OFF</sub> (50% CTL to 10%/90% RF)
Supply Voltage (V <sub>DD</sub> )	4.75	5.0	5.25	V	
Supply Current		5		mA	
Control Voltage (V <sub>CTL</sub> )	0		0.8	V	Low
	2.0		V <sub>DD</sub>	V	High

**Notes:**

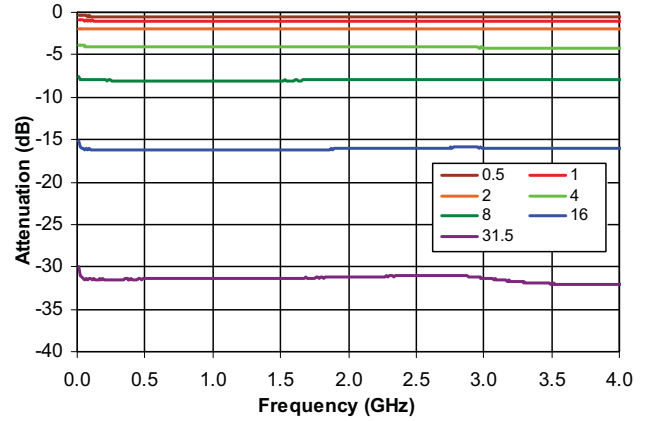
- V<sub>DD</sub> = 5V, V<sub>CTL</sub> = 3V, T = 25 °C
- Broadband Application Circuit (with ACG capacitors)
- IIP3 measured with Pin = +10dBm/tone, 1MHz spacing

**Typical Performance - Broadband Application Circuit (25 °C)**

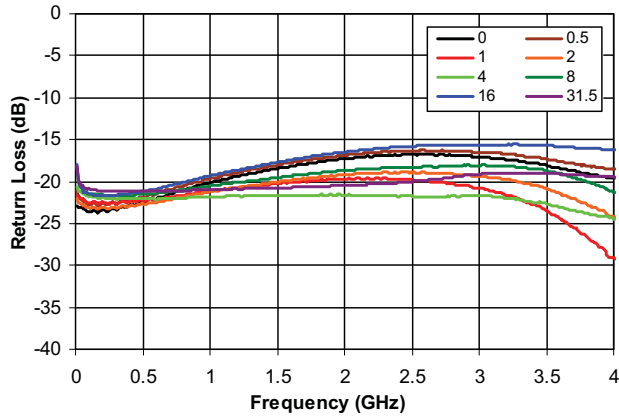
*Insertion Loss (De-embedded)*



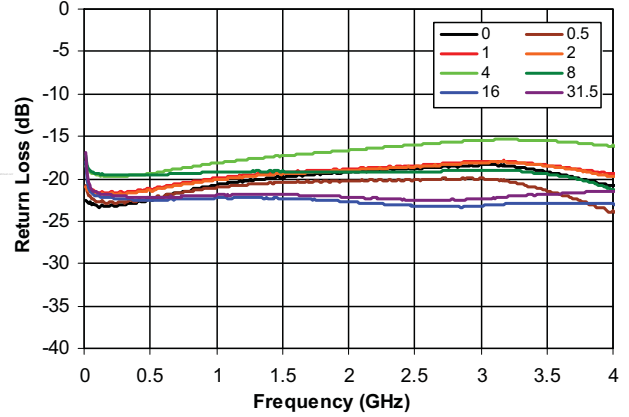
*Normalized Attenuation, MajorStates*



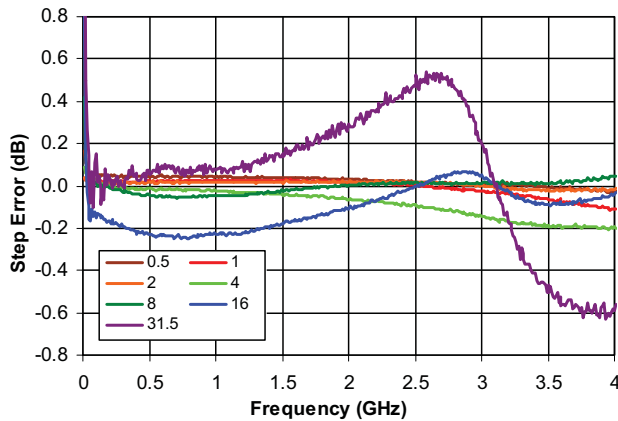
*Return Loss of RF1, MajorStates*



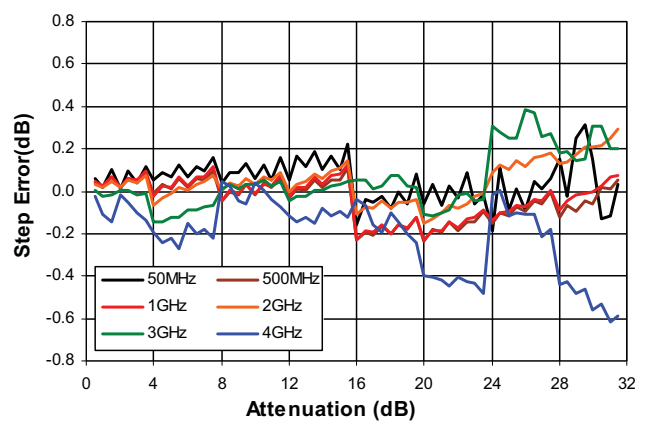
*Return Loss of RF2, MajorStates*



*Step Error, MajorStates*

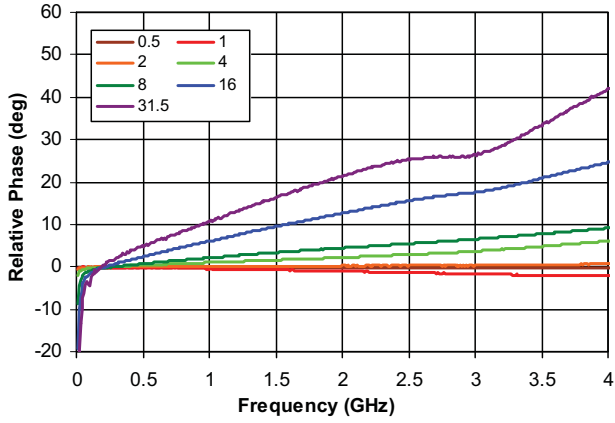


*Step Error vs. Attenuation State*

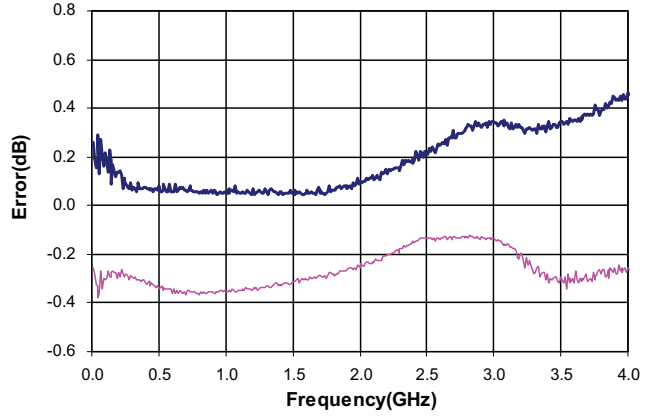


## Typical Performance - Broadband Application Circuit (25 °C) (Continued)

*Relative Phase, MajorStates*



*Worst Case Successive Step Error*

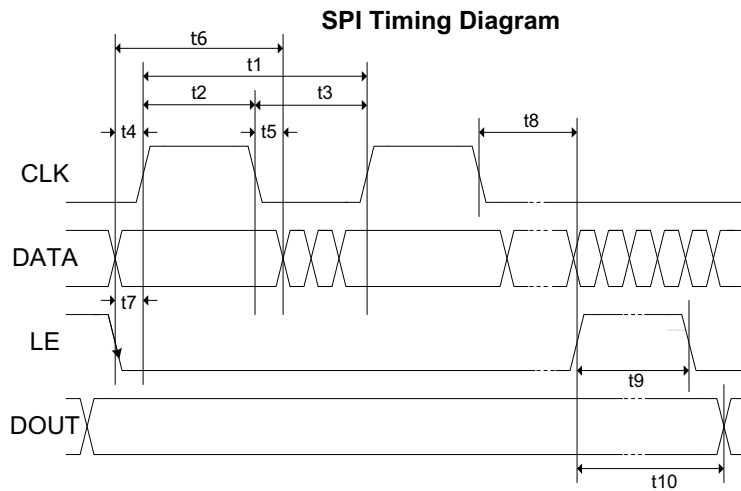


**Truth Table**

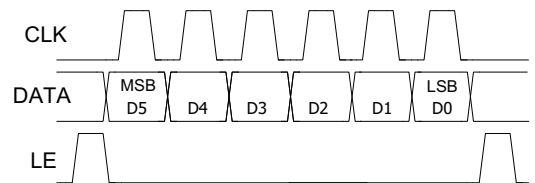
Control Bit						Relative Gain Setting
C16	C8	C4	C2	C1	C0.5	
1	1	1	1	1	1	Max gain
1	1	1	1	1	0	-0.5dB
1	1	1	1	0	1	-1dB
1	1	1	0	1	1	-2dB
1	1	0	1	1	1	-4dB
1	0	1	1	1	1	-8dB
0	1	1	1	1	1	-16dB
0	0	0	0	0	0	-31.5dB

Note: C 0.5=D0, C1=D1, ... C16=D5 (for the purpose of the example below)

**Serial Port Interface**



**Programming example – 6-bit**



**SPI Timing Diagram Specifications**

Parameter	Limit	Unit	Comment
t1	25	MHz max	CLK Frequency
t2	20	ns min	CLK High
t3	20	ns min	CLK Low
t4	5	ns min	DATA to CLK Setup Time
t5	5	ns min	DATA to CLK Hold Time
t6	30	ns min	Data Valid
t7	5	ns min	LE to CLK Setup Time
t8	5	ns min	CLK to LE Setup Time
t9	10	ns min	LE Pulse Width
t10	20	ns min	Output Set

LOGIC Voltage Levels	
State	Logic
Low	0V to 0.8V
High	2.0V to 5.0V

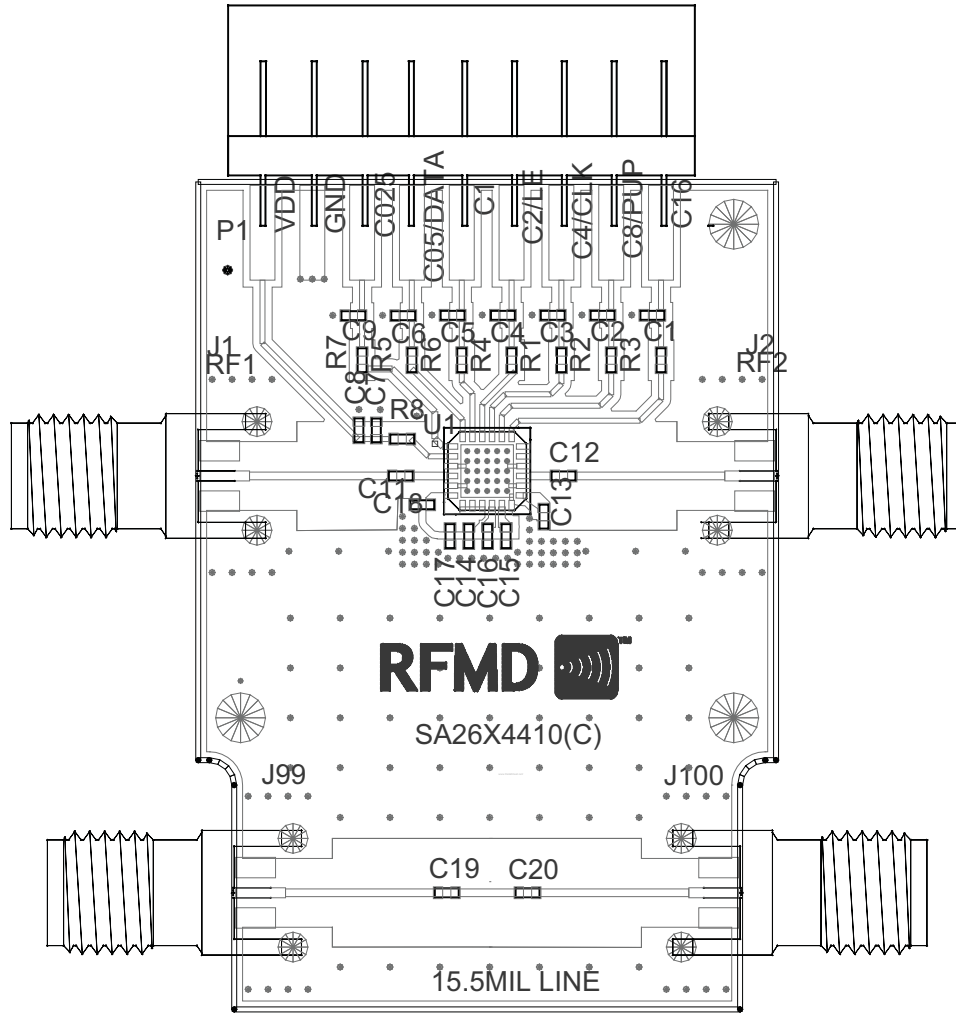
## Pin Names and Description

Pin	Function	Description
1	GND	DC and RF Ground.
2	VDD	Power supply.
3	GND	DC and RF Ground.
4	RF1	RF port. External DC block required.
5	GND	DC and RF Ground.
6	ACG	AC ground for operation below 500MHz; leave unconnected above 500MHz.
7	ACG	AC ground for operation below 500MHz; leave unconnected above 500MHz.
8	ACG	AC ground for operation below 500MHz; leave unconnected above 500MHz.
9	ACG	AC ground for operation below 500MHz; leave unconnected above 500MHz.
10	ACG	AC ground for operation below 500MHz; leave unconnected above 500MHz.
11	ACG	AC ground for operation below 500MHz; leave unconnected above 500MHz.
12	GND	DC and RF Ground.
13	ACG	AC ground for operation below 500MHz; leave unconnected above 500MHz.
14	GND	DC and RF Ground.
15	RF2	RF port. External DC block required.
16	GND	DC and RF Ground.
17	GND	DC and RF Ground.
18	GND	DC and RF Ground.
19	NC	No internal connection. EVB can be ground or no connect.
20	PUP	Power-up Programming pin. Low=max attenuation (31.5dB) at power-up, High=min attenuation (0dB) at power-up.
21	CLK	Serial Clock.
22	LE	Latch Enable.
23	NC	No internal connection. EVB can be ground or no connect.
24	DATA	Serial Data.
EPAD	GND	DC and RF ground. Must be soldered to EVB ground plane over a bed of vias for thermal and RF performance.

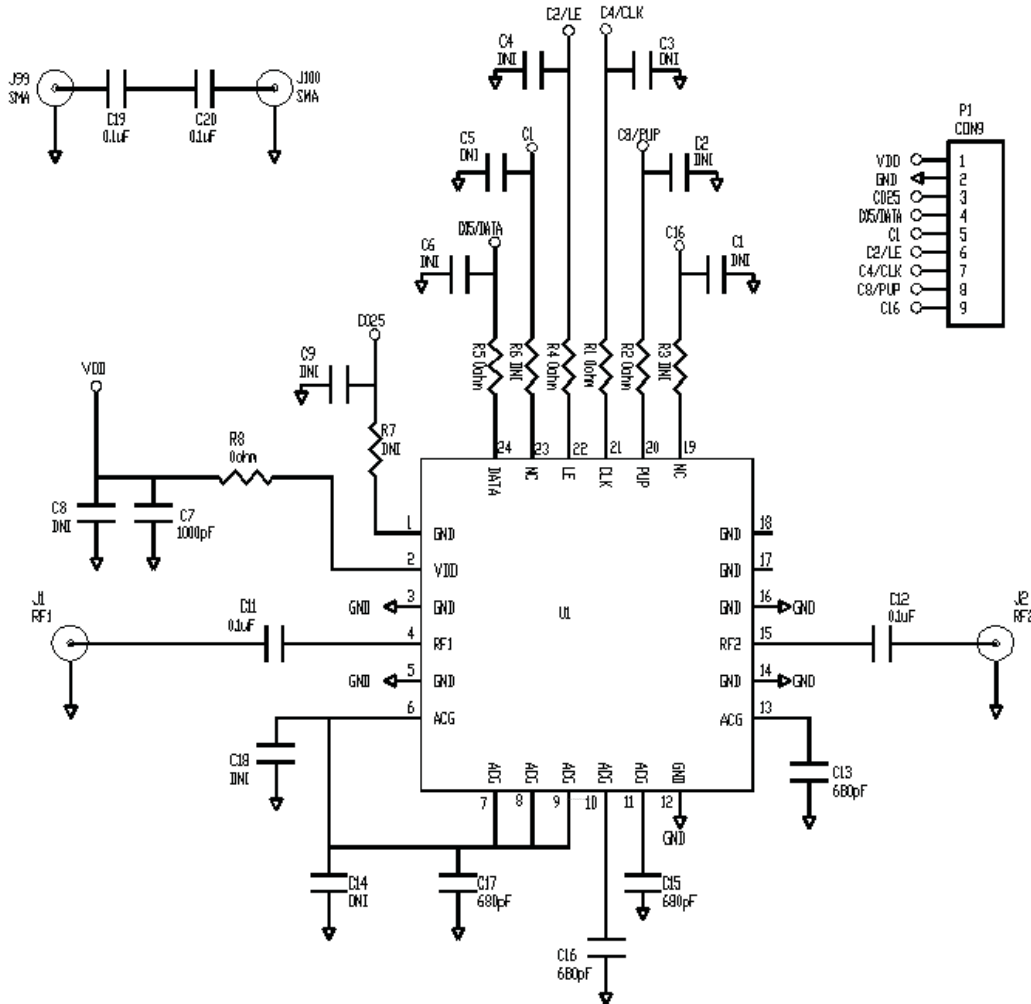
### Power-up Programming Truth Table

PUP	Attenuator Setting
Low	Attenuation at max, 31.5dB
High	Attenuation at min, 0dB

**Evaluation Board Assembly Drawing**



## Evaluation Board Schematic



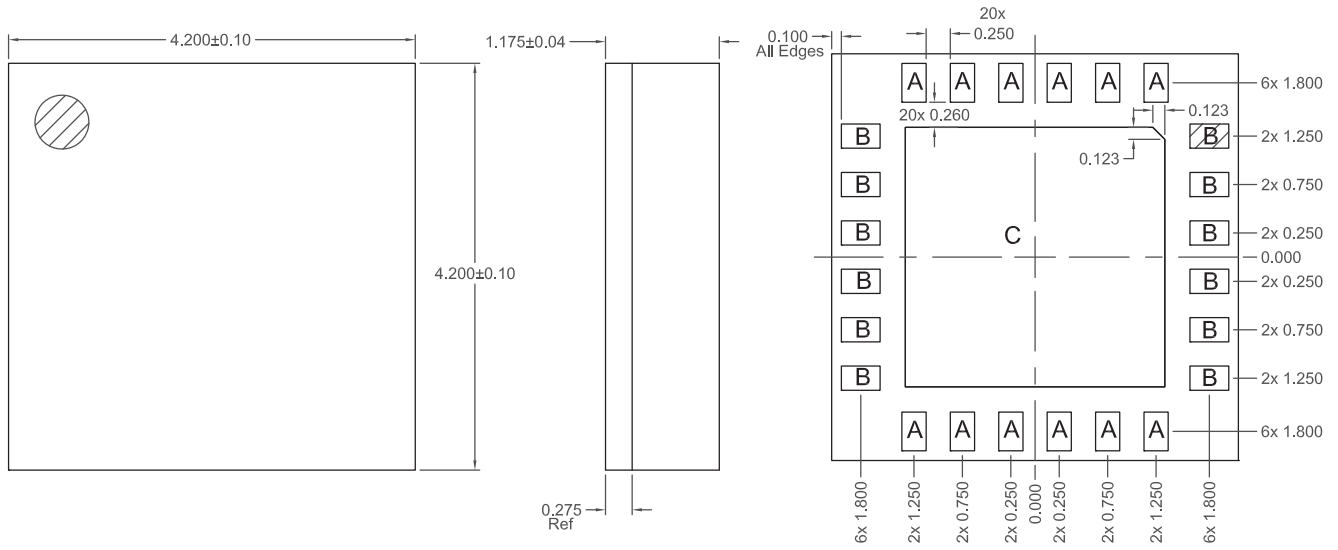
## Evaluation Board Bill of Materials (BOM)

Description	Reference Designator	Manufacturer	Manufacturer's P/N
PCB			RFSA26X4410(B)
CAP, 680pF, 10%, 50V, X7R, 0402	C13, C15, C16, C17	Murata	GRM155R71H681KA01E
CAP, 0.1uF, 10%, 10V, X5R, 0402	C11, C12, C19, C20	Taiyo Yuden (USA), Inc.	RM LMK105BJ104KV
CAP, 1000pF, 10%, 50V, X7R, 0402	C7	Taiyo Yuden (USA), Inc.	RM UMK105BJ102KV-F
RES, 0 OHM, 0402	R1, R2, R4, R5, R8	Kamaya, Inc	RMC1/16SJPTH
DNI	C1-C6, C8, C9, C14, C18, R3, R6-7		
CONN, SMA, END LNCH, UNIV, HYB MNT, FLT	J1, J2, J99, J100	Heilind Electronics	PER MAT-21-1038
CONN, HDR, ST, PLRZD, 9-PIN	P1	ITW Pancon	MPSS100-9-C
RFSA2624SB	U1	RFMD	RFSA2624

**NOTE:** Parts with \* following the Reference Designator should not be populated on PCBA. RFMD devices (DUT) may require baking per IPC/JEDEC J-STD-020 for a minimum of 24 hours at 125 +5/-0 °C. Assembly must take place within 12 hours of bake completion. Manufacturers' P/Ns are subject to change by the manufacturers following the issue of this document and are thereby included for reference only. Contact RFMD Corporate Engineering Materials with questions regarding specific Manufacturers' P/Ns. Shaded lines indicate approved alternate components.



**Package Drawing**



Notes:

1. Shaded area represents Pin 1 location

A =  $0.250 \times 0.400$  mm  
 B =  $0.400 \times 0.250$  mm  
 C =  $2.680 \times 2.680$  mm