

# RFVC1822

## Low Noise MMIC VCO with Buffer Amplifier

RFMD's RFVC1822 is a 3V InGaP MMIC VCO with an integrated buffer amplifier operating over a frequency range of 5.0GHz to 5.5GHz. Its monolithic tuning structure provides excellent temperature, shock, and vibration performance while its integrated buffer amplifier provides an output power of +9dBm from a 3V supply. Phase noise is -103dBc/Hz at 100kHz offset. The RFVC1822 is available in a low cost leadless ceramic 4mm x 4mm surface mount QFN outline.



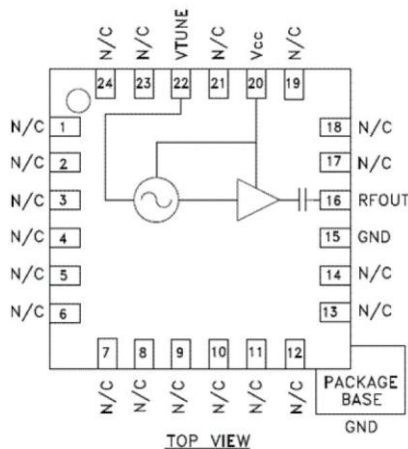
Package: QFN, 24-pin, 4mm x 4mm

### Features

- 5.0GHz to 5.5GHz Operation
- -103dBc/Hz Phase Noise at 100KHz Offset
- +9.0dBm P<sub>OUT</sub>
- No External Resonator or Elements Needed
- 4mm x 4mm QFN Package
- 3V V<sub>CC</sub> Operation

### Applications

- Instrumentation
- Military
- Aerospace
- Point-to-Point Radio
- Test Equipment
- VSAT
- CATV



Functional Block Diagram

### Ordering Information

RFVC1822S2	Sample bag with 2 pieces
RFVC1822SB	Sample bag with 5 pieces
RFVC1822SQ	Bag with 25 pieces
RFVC1822SR	7" Reel with 100 pieces
RFVC1822TR7	7" Reel with 750 pieces
RFVC1822PCK-410	PCBA with 2-piece sample bag

## Absolute Maximum Ratings

Parameter	Rating	Unit
Bias Voltage ( $V_{DD}$ )	+3.25	$V_{DC}$
$V_{TUNE}$ ( $V_T$ )	14	$V_{DC}$
Operating Junction Temperature ( $T_J$ )	99	$^{\circ}C$
Continuous Power Dissipation ( $T = +85^{\circ}C$ )	200	mW
Thermal Resistance (Pad to Die Bottom)	10	$^{\circ}C/W$
Operating Temperature Range	-40 to +85	$^{\circ}C$
Storage Temperature Range	-55 to +150	$^{\circ}C$
ESD JESD22-A114 Human Body Model (HBM)	Class 0, 150V	



**Caution!** ESD sensitive device.



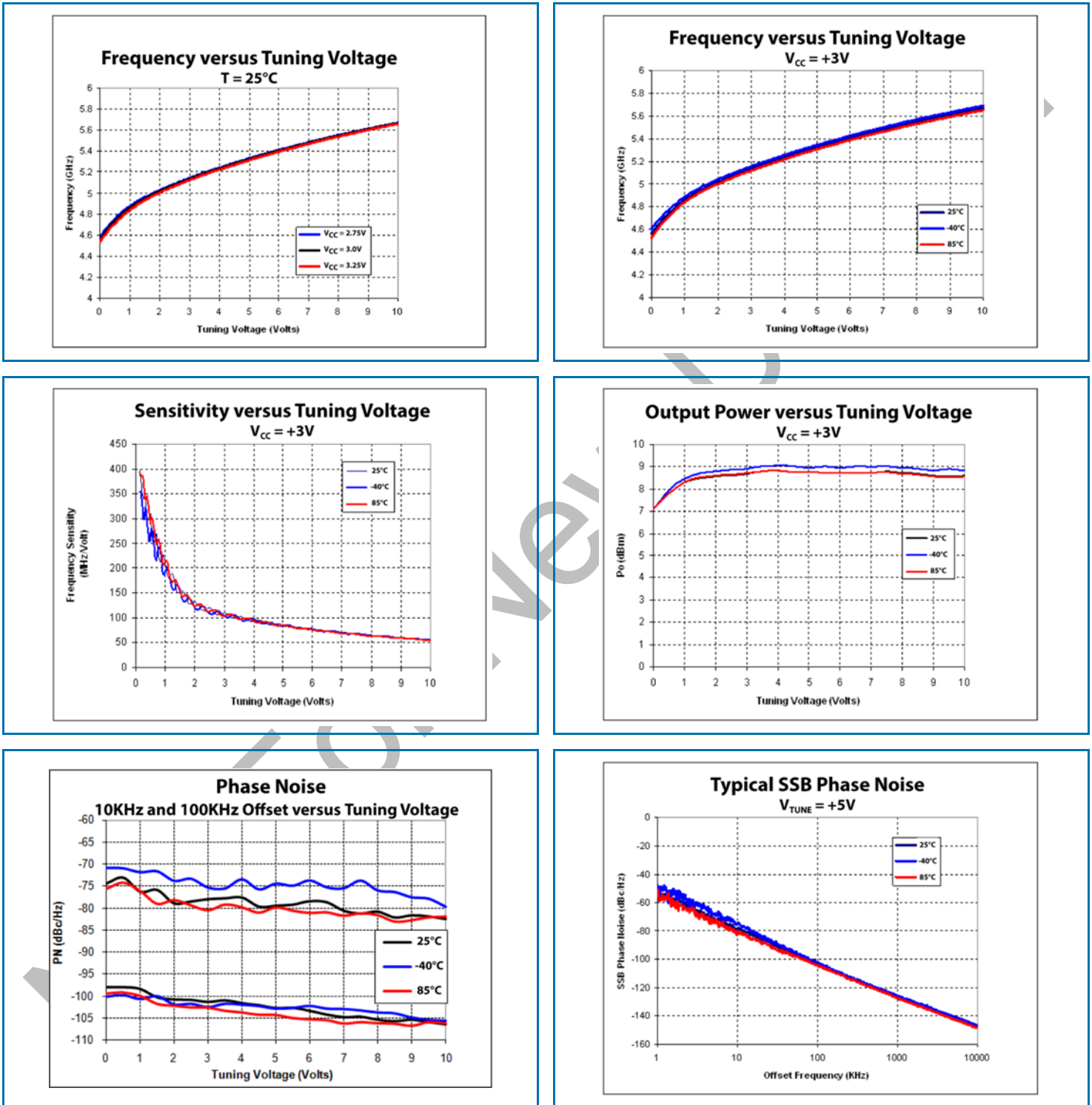
RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

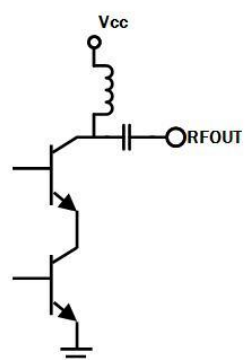
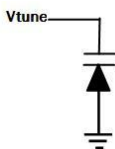
## Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
<b>General Performance</b>					<b><math>T_A = +25^{\circ}C, V_{CC} = +3.0V_{DC}</math></b>
Operating Frequency	5.0		5.5	GHz	
Tuning Voltage ( $V_{TUNE}$ )	0		12	V	
$V_{TUNE}$ Leakage Current		0.34	1.0	$\mu A$	At $V_{TUNE} = 10V$
Output Power	5	9		dBm	At $V_{TUNE} = 5V$
Phase Noise at 10kHz Offset		-80		dBc/Hz	
Phase Noise at 100kHz Offset		-103		dBc/Hz	
Harmonics					
2nd		-14		dBc	At $V_{TUNE} = 5V$
3rd		-37		dBc	
Output Spurious			-70	dBc	
RF Output Return Loss		10		dB	
Supply Current		45	50	mA	At $V_{TUNE} = 5V$
Pushing		5.0		MHz/V	VSWR 2.5:1 all phases
Pulling		2.2		MHz	At $V_{TUNE} = 5V$
Frequency Drift Rate		-0.3		MHz/ $^{\circ}C$	

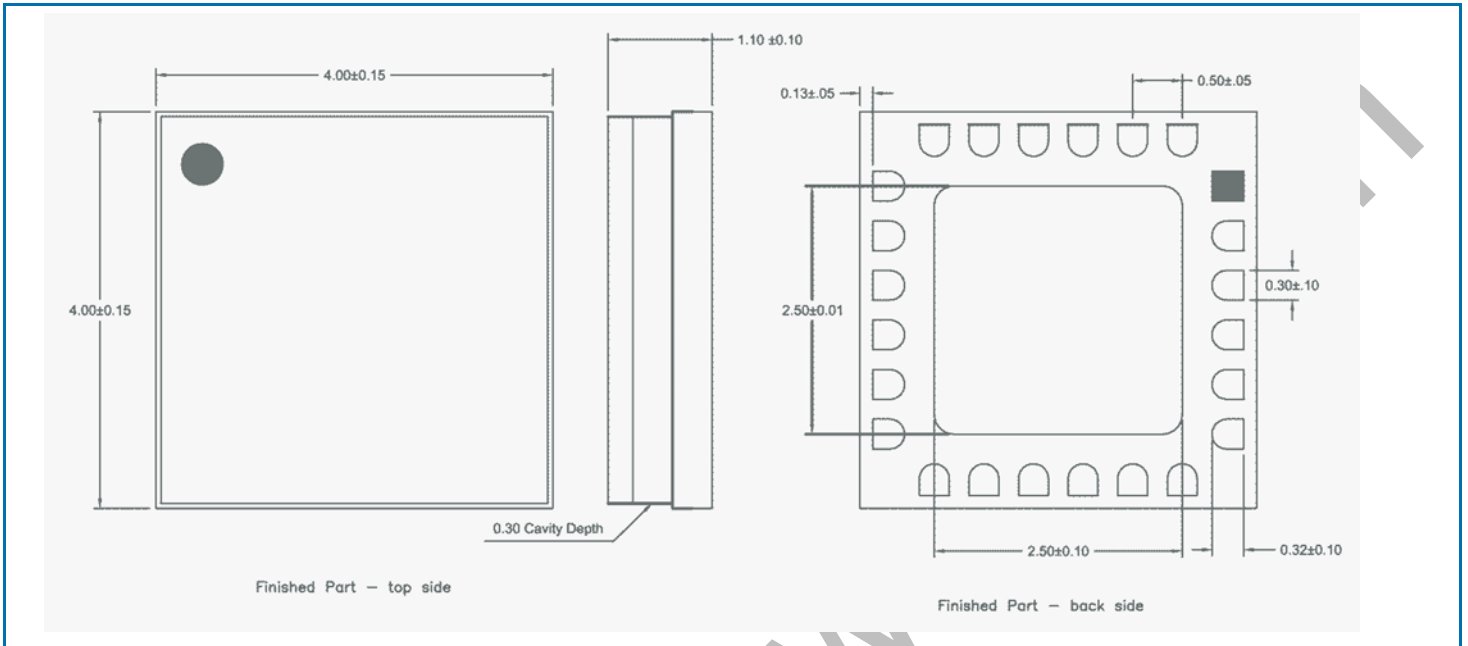
Typical Electrical Performance



## Pin Names and Descriptions

Pin	Name	Description	Interface Schematic
1-14	N/C	No internal connection. Connect to PCB ground.	
15	GND	Connect directly to PCB ground for best performance.	
16	RFOUT	RF out. This pad is AC coupled and matched for optimum $P_{OUT}$ . A 50Ω termination is recommended for this pin.	
17-19	N/C	No internal connection. Connect to PCB ground.	
20	VCC	Connect 3V to power both the oscillator core and the buffer amplifier.	
21	N/C	No internal connection. Connect to PCB ground.	
22	VTUNE	Direct connection to the varactor diodes used to vary the frequency of oscillation.	
23-24	N/C	No internal connection. Connect to PCB ground.	
PKG BASE	GND	Ground connection. Solder package bottom directly to ground plane for best performance.	

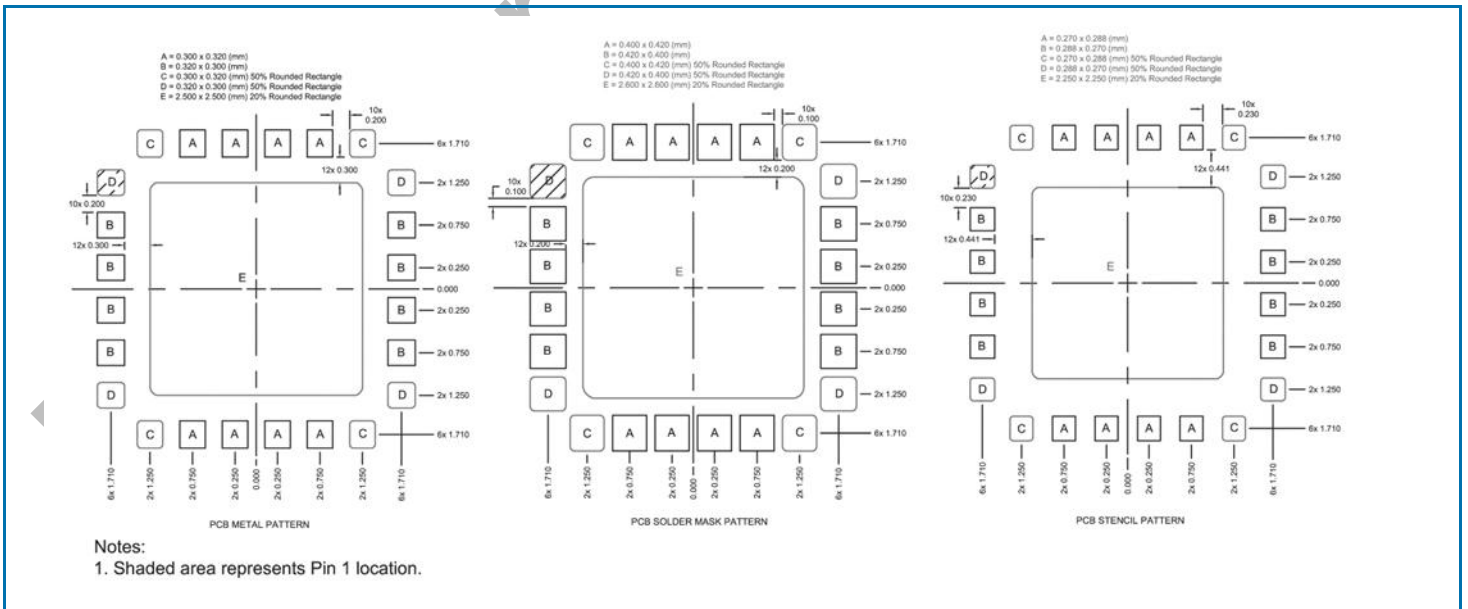
Package Drawing (Dimensions in millimeters)



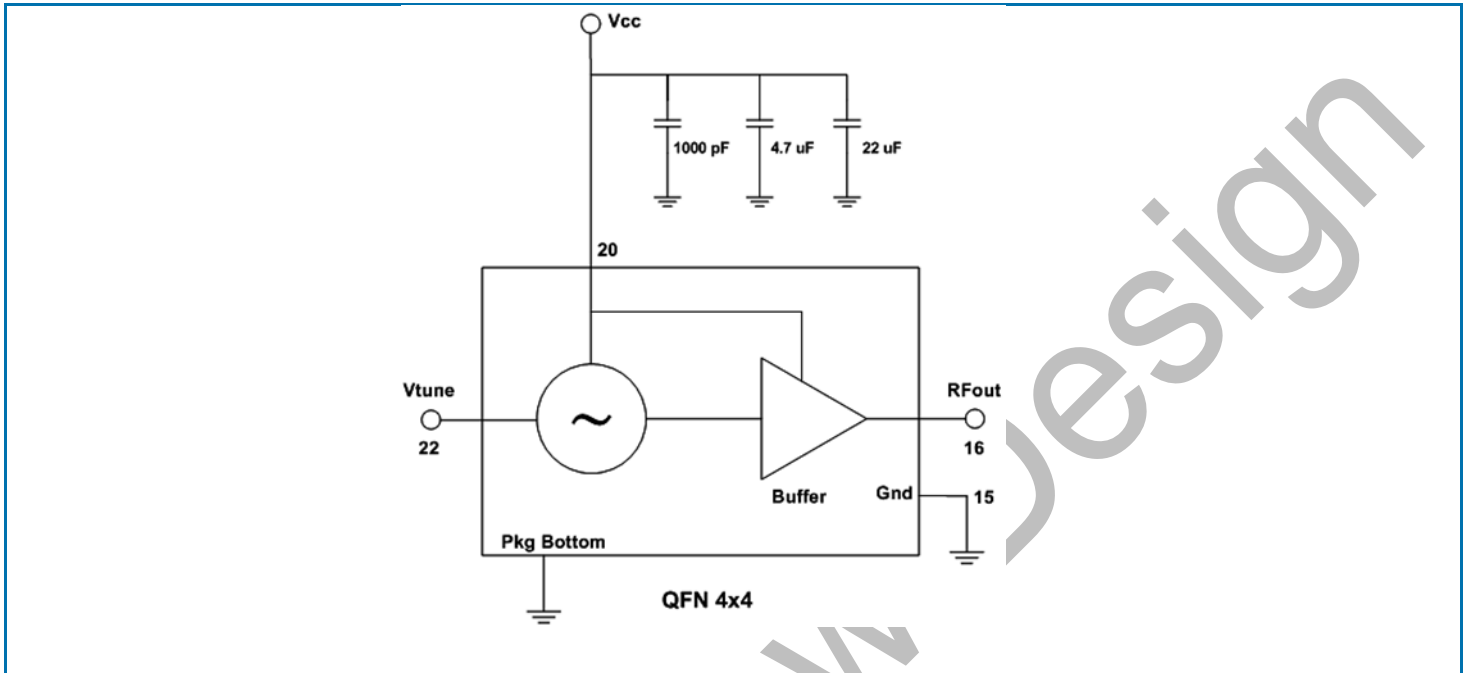
Notes:

1. Dimensions are for reference only.
2. Package body material: Alumina.
3. Lead and paddle plating: Au, 30u" minimum.

Recommended PCB Layout



### Application Circuit Block Diagram



### Evaluation Board Layout

