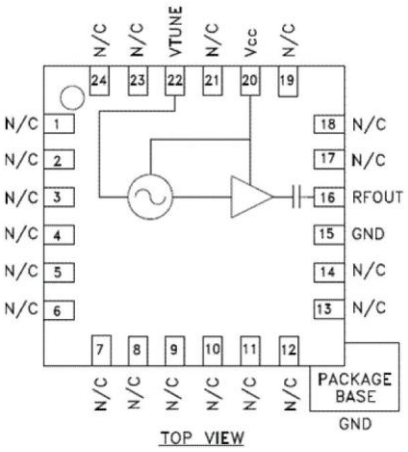
RFVC1825

Low Noise MMIC VCO with Buffer Amplifier

RFMD's RFVC1825 is a 3V InGaP MMIC VCO with an integrated buffer amplifier operating over a frequency range of 7.8GHz to 8.7GHz. Its monolithic tuning structure provides excellent temperature, shock, and vibration performance while its integrated buffer amplifier provides an output power of +11dBm from a 3V supply. Phase noise is -107dBc/Hz at 100kHz offset. The RFVC1825 is available in a low cost leadless ceramic 4mm x 4mm surface mount QFN outline.



Functional Block Diagram

Package: QFN, 24-pin, 4mm x 4mm

Features

- 7.8GHz to 8.7GHz Operation
- -107dBc/Hz Phase Noise at 100kHz Offset
- +11.0dBm P_{OUT}
- No External Resonator or Elements Needed
- 4mm x 4mm QFN Package
- 3V V_{CC} Operation

Applications

- Instrumentation
- Military
- Aerospace
- Point-to-Point Radio
- Test Equipment
- VSAT
- CATV

Ordering Information

RFVC1825S2	Sample bag with 2 pieces
RFVC1825SB	Bag with 5 pieces
RFVC1825SQ	Bag with 25 pieces
RFVC1825SR	7" Reel with 100 pieces
RFVC1825TR7	7" Reel with 750 pieces
RFVC1825PCK-410	PCBA with 2-piece sample bag

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS140502

Absolute Maximum Ratings

Parameter	Rating	Unit
Bias Voltage (V_{DD})	+3.25	V_{DC}
V_{TUNE} (V_T)	14	V_{DC}
Operating Junction Temperature (T_J)	99	°C
Continuous Power Dissipation (T = +85°C)	200	mW
Thermal Resistance (Pad to Die Bottom)	10	°C/W
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-55 to +150	°C
ESD JESD22-A114 Human Body Model (HBM)	Class 0, 150V	

Caution! ESD sensitive device.

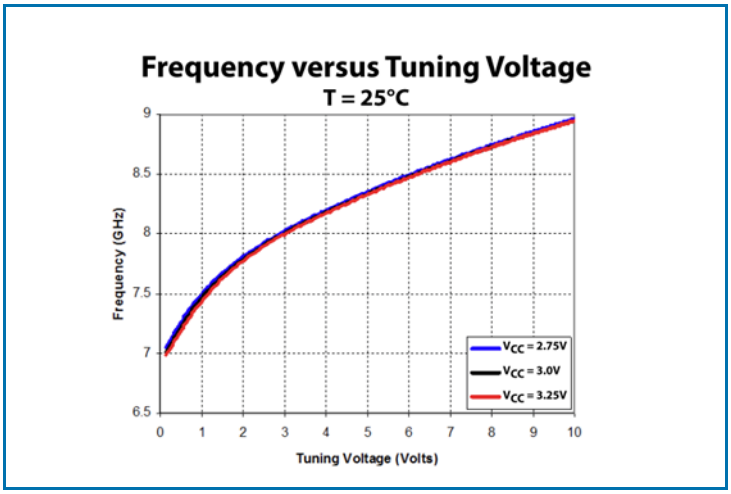
RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

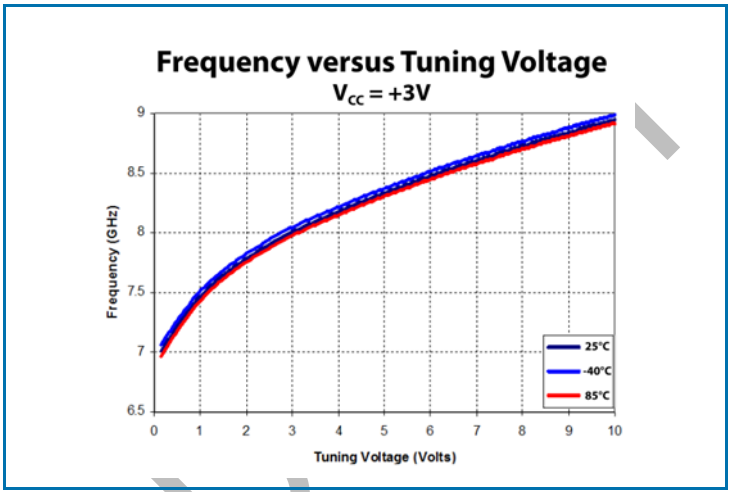
Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

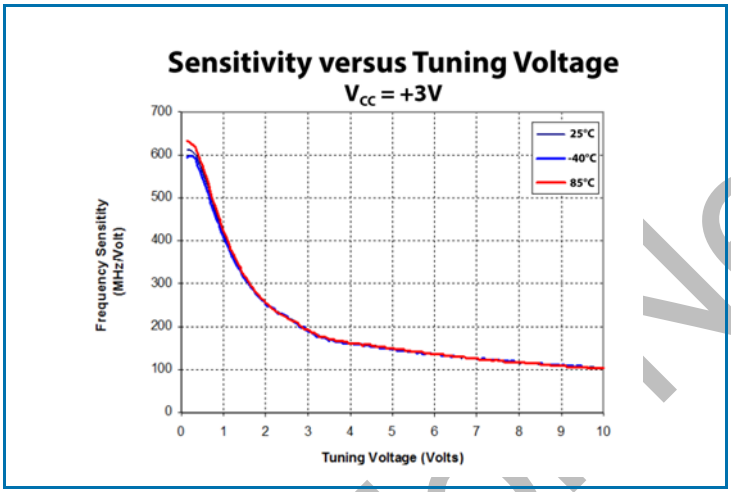
Nominal Operating Parameters

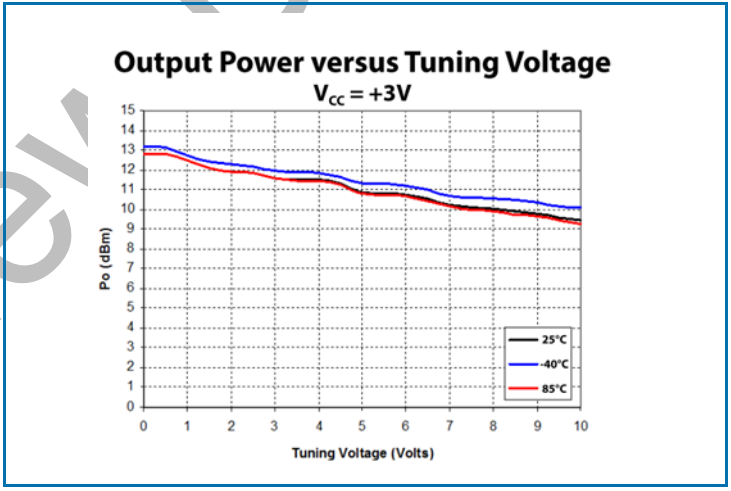
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
General Performance					**T_A = +25°C, V_{CC} = +3.0V_{DC}**
Operating Frequency	7.8		8.7	GHz	
Tuning Voltage (V_{TUNE})	0		12	V	
V_{TUNE} Leakage Current		0.36	1.0	µA	At V_{TUNE} = 10V
Output Power	5	11		dBm	At V_{TUNE} = 5V
Phase Noise at 10kHz Offset		-80		dBc/Hz	
Phase Noise at 100kHz Offset		-107		dBc/Hz	
Harmonics					
2nd		-10		dBc	At V_{TUNE} = 5V
3rd		-25		dBc	
Output Spurious			-70	dBc	
RF Output Return Loss		10		dB	
Supply Current		67	80	mA	At V_{TUNE} = 5V
Pulling		1.6		MHz	VSWR 2.5:1 all phases
Pushing		-47		MHz/V	At V_{TUNE} = 5V
Frequency Drift Rate		-0.53		MHz/°C	

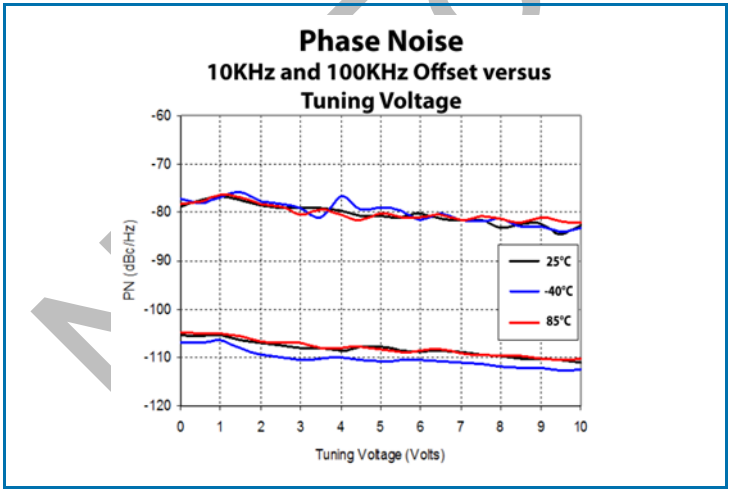
Typical Electrical Performance

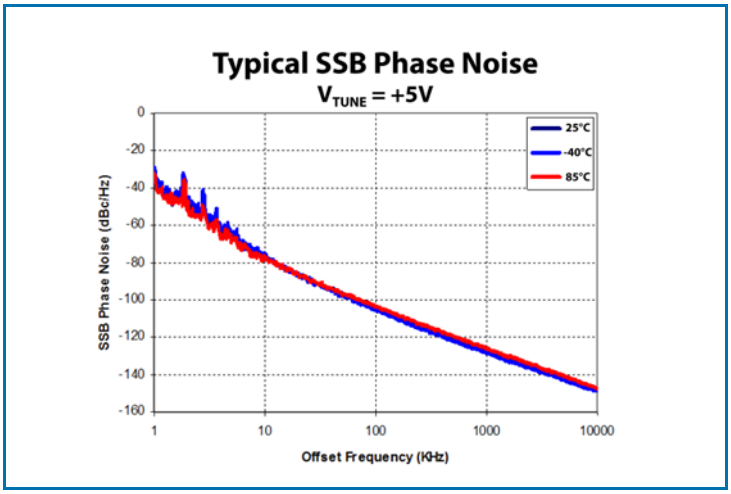




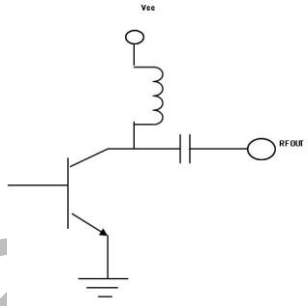
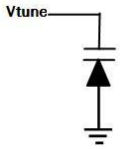




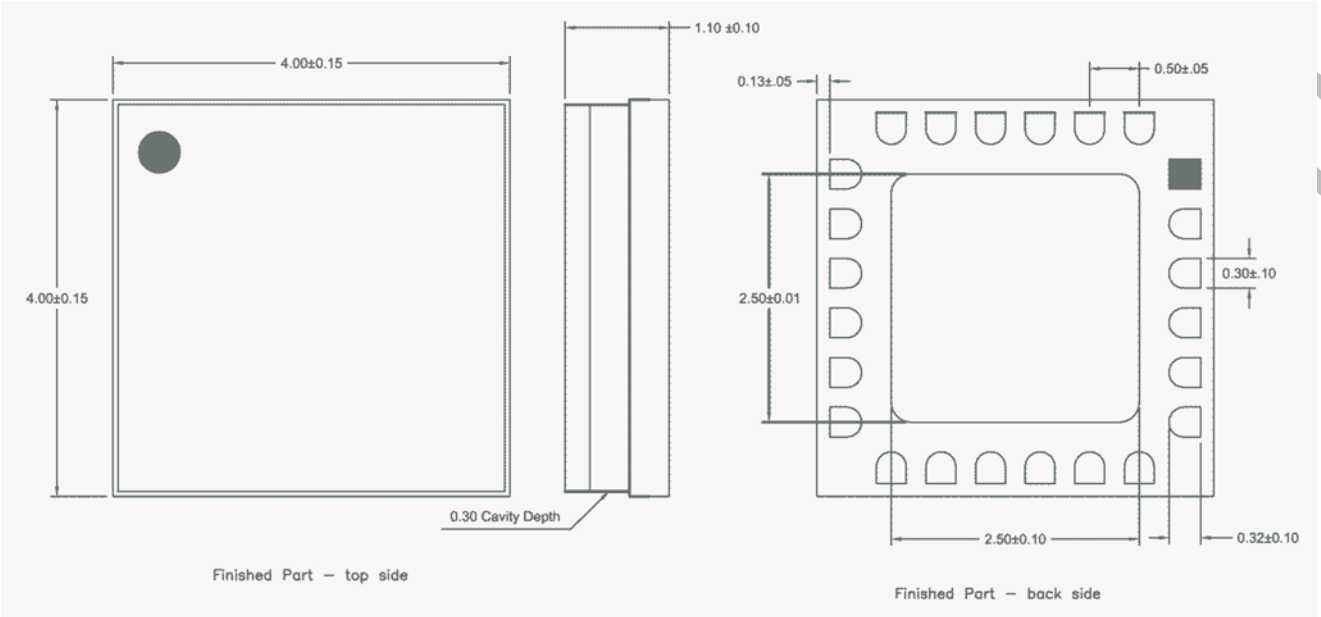




Pin Names and Descriptions

Pin	Name	Description	Interface Schematic
1-14	N/C	No internal connection. Connect to PCB ground.	
15	GND	Connect directly to PCB ground for best performance.	
16	RFOUT	RF out. This pad is AC coupled and matched for optimum P_{OUT}. A 50Ω termination is recommended for this pin.	
17-19	N/C	No internal connection. Connect to PCB ground.	
20	VCC	Connect 3V to power both the oscillator core and the buffer amplifier.	
21	N/C	No internal connection. Connect to PCB ground.	
22	VTUNE	Direct connection to the varactor diodes used to vary the frequency of oscillation.	
23-24	N/C	No internal connection. Connect to PCB ground.	
PKG BASE	GND	Ground connection. Solder package bottom directly to ground plane for best performance.	

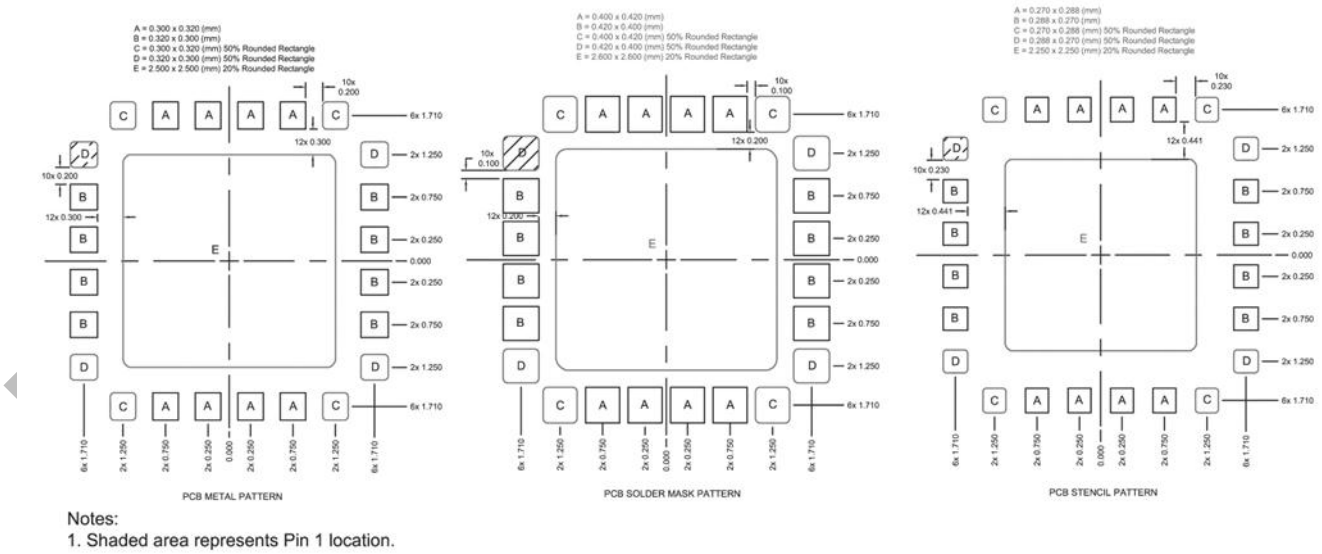
Package Drawing (Dimensions in millimeters)



Notes:

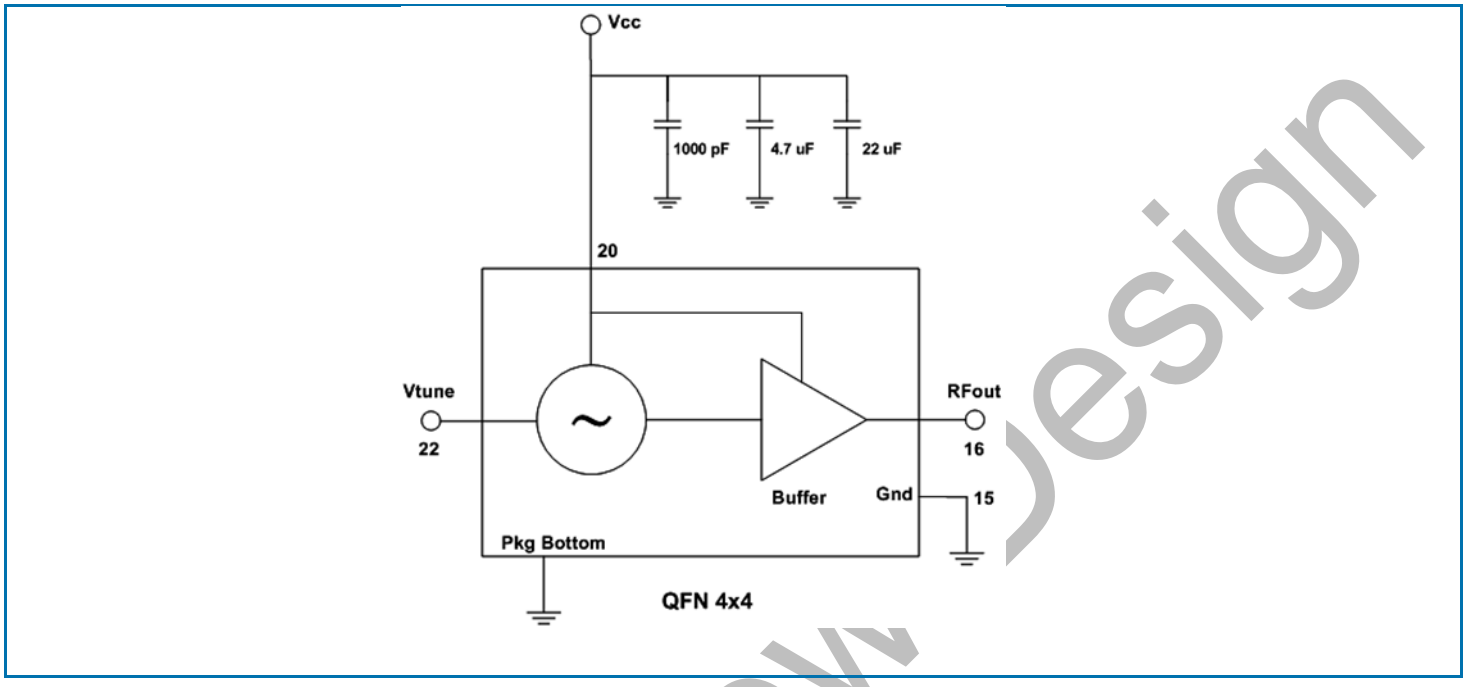
1. Dimensions are for reference only.
2. Package body material: Alumina.
3. Lead and paddle plating: Au, 30µm minimum.

Recommended PCB Layout



Notes:
1. Shaded area represents Pin 1 location.

Application Circuit Block Diagram



Evaluation Board Layout