Intel® 865G/865GV Chipset

Specification Update

Intel® 82865G/82865GV Graphics Memory Controller Hub (GMCH)

January 2004

Notice: The Intel® 82865G/Intel® 82865GV GMCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 252515-003

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release.	May 2003
-002	Added 82865GV GMCH. Added Erratum #4.	September 2003
-003	Added Errata #5, AGP ATTBase Translation Erratum Added Errata #6, DDC Slave Stall during Acknowledge Phase or Short Slave Stall Errata Added Specification Clarification #1, Package Dimensions (Bottom View) Corrected the Device ID in the Component Identification via Programming Interface table	January 2004

Preface

This public document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 865G/865GV Chipset: Intel® 82865G/82865GV Graphics and Memory Controller Hub (GMCH) Datasheet	252514-004

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the Intel 82865G/82865GV GMCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The 82865G/82865GV GMCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	2560h	02h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The 82865G/82865GV GMCH may be identified by the following component markings:

Stepping	Q-Spec	S-Spec	Top Marking	Notes
A2	QE40	SL743	RG82865G	82865G GMCH
A2	QE59	SL77X	RG82865GV	82865GV GMCH

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed 82865G/82865GV GMCH steppings. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Errata that applies to this stepping.
Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Shaded: This item is either new or modified from the previous version of the document

NO.	A2	PLANS	ERRATA
1	X	NoFix	VGA Timing
2	X	Doc	DDR400 Write to Read Turnaround Latency Erratum
3	X	NoFix	FSB800 / DDR333 Running at 320 MHz Refresh Timing Erratum
4	A2	Doc	CKE Memory Glitch
5	X	Doc	AGP ATTBase Translation Erratum
6	X	NoFix	DDC Slave Stall during Acknowledge Phase or Short Slave Stall Errata

NO.	SPECIFICATION CHANGES
	There are no specification changes in this Specification Update revision.

NO.	SPECIFICATION CLARIFICATIONS
1	Package Dimensions (Bottom View)

NO.	DOCUMENTATION CHANGES
	There are no documentation changes in this Specification Update revision.

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Errata

1. VGA Timing

Problem: Some VGA applications, running in 40-column modes, that use a non-black border color, may experience color/visual issues on systems configured with certain monitors

Implication: 40-column VGA modes may experience visual color anomalies on some CRT monitors. This was observed using VGA focused Intel test software. With certain monitors, colors in active areas may change as the border color changes. As observed while using the test software, visual color anomalies can range from a slight color change difference to a blank screen. Based on the lack of customer or end user reported issues related to this erratum, the number of VGA applications that run in 40-column modes and also use non-black border colors is low. Based on Intel's validation and compatibility testing, the number of CRT monitors that exhibit this color anomaly is also low.

Workaround: No workaround exists.

Status: This will not be fixed in future steppings.

2. DDR400 Write to Read Turnaround Latency Erratum

Problem: Under a specific read / write sequence with DDR400 memory, the chipset waits only 1 tCK between issuing memory write to read cycles to the same rank which violates the DDR400 device internal write to read command delay spec of 2 tCKs.

Note: DDR333/266 JEDEC device internal write to read command spec is 1 tCK.

Implication: No system or memory failures have been observed during extensive testing. However, the DDR400 device write to read spec is violated which may result in unpredictable memory device operation depending on the memory device being used.

Workaround: Contact your Intel Field Representative for the latest BIOS information.

Status: No silicon fix planned.

3. FSB800 / DDR333 Running at 320 MHz Refresh Timing Erratum

Problem: When a system is configured with an 800 MHz FSB processor and DDR333 DIMM(s), the chipset's memory interface operates at 320 MHz. At this specific memory frequency, the chipset issues refresh cycles at a slower rate than the DDR333 JEDEC specification documents.

Chipset, with memory frequency at 320 MHz, issues refresh cycles every:
8.1 µs with 256-Mb and 512-Mb memory technology
16.2 µs with 64-Mb and 128-Mb memory technology

JEDEC spec for DDR333 devices is:
7.8 µs with 256-Mb and 512-Mb memory technology
15.6 µs with 64-Mb and 128-Mb memory technology

Implication: None

Workaround: None

Status: No silicon fix planned. Intel has contacted the major memory suppliers about this issue and has modified the DDR validation specification that Intel uses to test memory. Feedback from memory suppliers is that they can meet Intel's updated DDR validation specification

4. CKE Memory Glitch

Problem: After PCI_RST is driven low, the (G)MCH may tri-state CKE for approximately 1ns. When tri-stated, CKE may glitch up to VTERM.

Implication: When entering S3, a glitch on CKE greater than VIL may cause the DDR devices to wake from self-refresh causing system lockup upon resume from S3.

Workaround: Contact your Intel Field Representative for the latest BIOS information.

Status: No silicon fix planned.

5. AGP ATTBase Translation Erratum

Problem: Under heavy AGP traffic, if an AGP request is made while an Aperture Translation Table Base address change occurs, then the AGP request may be translated incorrectly.

Implication: When using the Microsoft Windows* 98/SE/ME operating system, and running applications that change the ATTBase often, the system may experience unpredictable system behavior. All other operating systems do not allow changing of the ATTBase address while AGP transactions are occurring.

Workaround: Please contact your local Field Representative for workaround details.

Status: There is no silicon fix planned for this erratum.

6. DDC Slave Stall during Acknowledge Phase or Short Slave Stall Errata

Problem: Under specific conditions, a slave stall on the DDC interface during the acknowledge phase or a very short slave stall (less than 1 DDC clock) during reads on the DDC interface, may cause the stall to be ignored and not seen by the MCH resulting in unpredictable system behavior.

Implication: These issues have only been seen in a synthetic test environment and may result in unpredictable system behavior. No system failures have been observed during normal system operation

Workaround: None

Status: No silicon fix planned.

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Specification Changes

There are no specification changes in this Specification Update revision.

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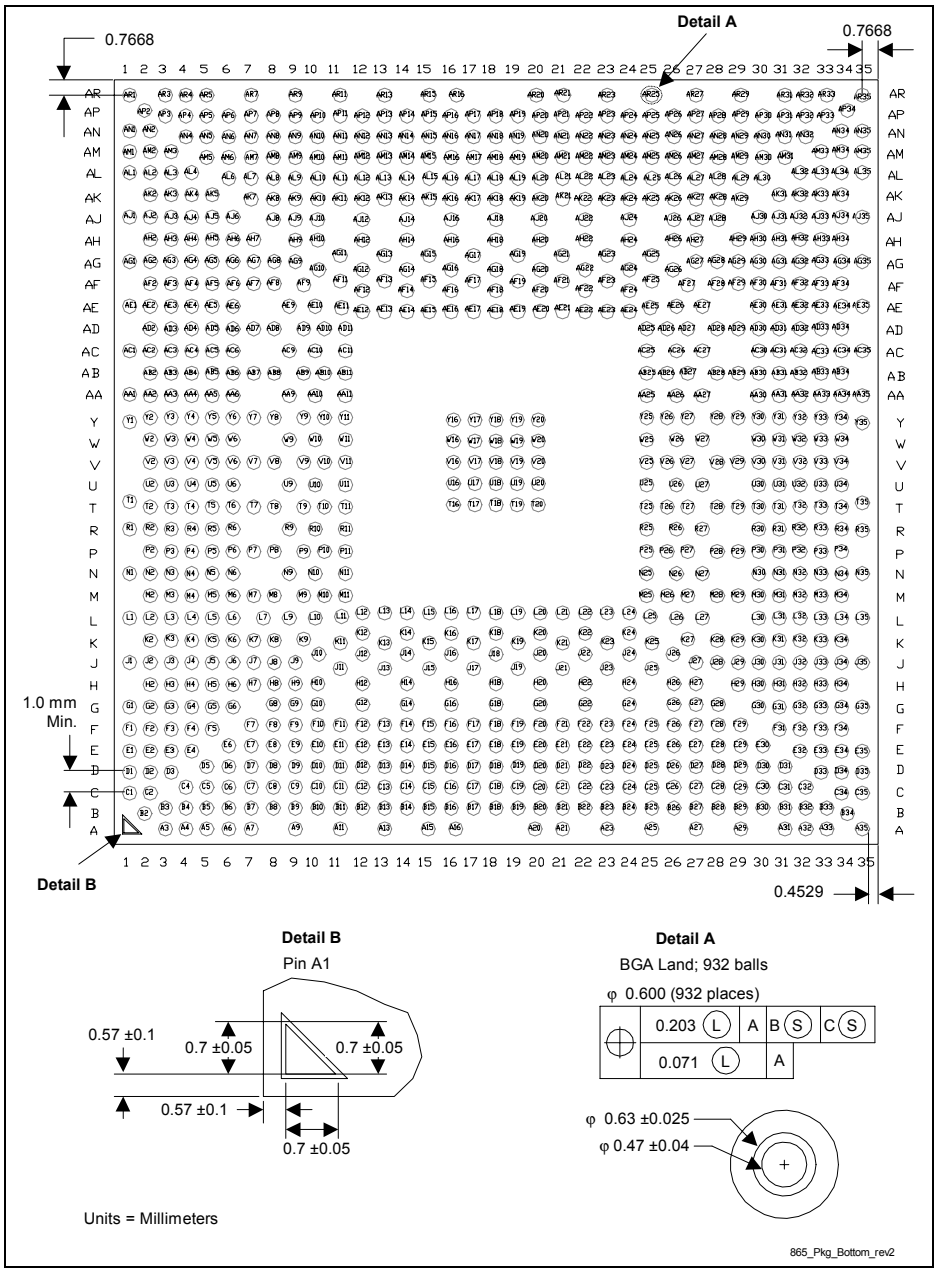
Specification Clarifications

1. Package Dimensions (Bottom View)

Figure 19, "Intel® 82865G GMCH Package Dimensions (Bottom View)" is replaced with the following, corrected figure:



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Documentation Changes

There are no documentation changes in this Specification Update revision.