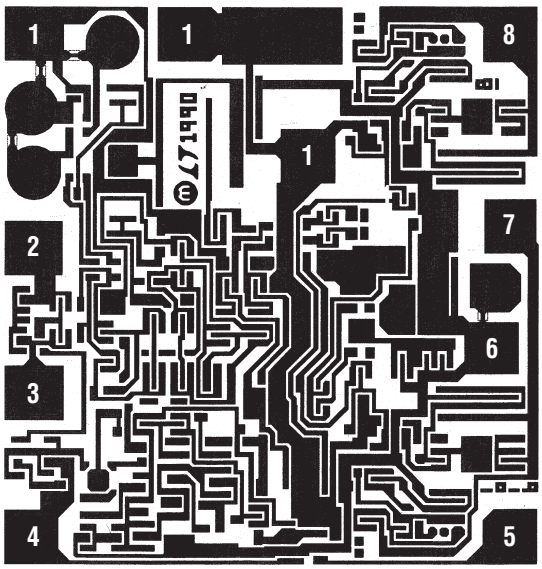
DICE/DWF SPECIFICATION

RH1016
UltraFast™ Precision 10ns Comparator



56mils × 58mils
Backside Connection is V^-

PAD FUNCTION

1. V^+
2. +IN
3. –IN
4. V^-
5. LATCH ENABLE
6. GND
7. $\overline{Q}$ OUT
8. Q OUT

DIE CROSS REFERENCE

LTC Finished Part Number	Order Part Number
RH1016M	RH1016 DICE
RH1016M	RH1016 DWF*

***DWF = DICE in wafer form.**

DICE ELECTRICAL TEST LIMITS

T_A = 25°C. V^+ = 5V, V^- = –5V, $V_{OUT(Q)}$ = 1.4V, V_{LATCH} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$ (Note 1)		±3	mV
I_{OS}	Input Offset Current	(Note 1)		1	µA
I_B	Input Bias Current	(Note 2)		10	µA
	Input Voltage Range	(Note 3) Single 5V Supply (Note 3)	–3.75 1.25	3.5 3.5	V V
CMRR	Common Mode Rejection	$-3.75V \le V_{CM} \le 3.5V$	80		dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \le V^+ \le 5.4V$ Negative Supply $-7V \le V^- \le -2V$	60 80		dB dB
A_V	Small-Signal Voltage Gain	$1V \le V_{OUT} \le 2V$	1400		V/V
V_{OH}	Output High Voltage	$V^+ \ge 4.6V$, I_{OUT} = 1mA I_{OUT} = 10mA	2.80 2.60		V V
V_{OL}	Output Low Voltage	I_{SINK} = 4mA		0.5	V
I^+	Positive Supply Current			35	mA
I^-	Negative Supply Current			5	mA
V_{IH}	Latch Pin High Input Voltage		2.0		V
V_{IL}	Latch Pin Low Input Voltage			0.8	V
I_{IL}	Latch Pin Current	V_{LATCH} = 0V		500	µA

Note 1: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 2: Input bias current (I_B) is defined as the average of the two input currents.

Note 3: Input voltage range is guaranteed in part by CMRR testing and in part by design and characterization. See the LT1016 data sheet for discussion of input voltage range for supplies other than ±5V or 5V.

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Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much “softer” than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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