

OKAYA Electric America. Inc.

SPECIFICATIONS

DRAWING CODE

LMD-PH320240T-006-I03Q (VER: 001)

SAMPLE CODE

PH320240T-006-I03Q

(This Code will be changed while mass production)

MASS PRODUCTION CODE

-RH320240T-3X5WN-A3

Customer Approved

Date:

Sales Sign	QC Confirmed	Checked By	Designer
		•	C

Approval For Specifications Only.

* This specification is subject to change without notice.

Approval For Specifications and Sample.



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History of Version

Date	Ver.	Edi.	Description	Page	Design by
Date	V C1.	Lui.	Description	ı aye	Design by
03/11/2008	0	-	New drawing	-	LIUJIN
04/24/2008	0	-	New Sample	-	LIUJIN
05/28/2008	Α	-	Modify the Module's Supply Current ,Power Consumption and Uniformity	-	LIUJIN
05/30/2008	01	001	Mass Production	-	LIUJIN

Total: 26 Page



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1. SPECIFICATIONS

1.1 Features

Main LCD panel

<u> </u>	
Item	Standard Value
Display Type	320(R · G · B) * 240 Dots
LCD Type	Normally white , Transmissive type
Screen size(inch)	3.5 inch
Viewing Direction	6 O'clock
Color configuration	RGB-Strip
Backlight	LED
Interface	Digital 24-bits RGB
Other(controller/driver IC)	Himax: HX8238-A
ROHS	THIS PRODUCT CONFORMS THE ROHS

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	76.9(W) * 63.9 (L) * 3.5 (H)(MAX)	mm

LCD panel

Item	Standard Value	Unit
Viewing Area	72.88 (W) * 55.36 (L)	mm
Active Area	70.08 (W) * 52.56 (L)	mm

Note: For detailed information please refer to LCM drawing



1.3 Absolute Maximum Ratings

Module

Item	Symbol	Condition	Min.	Max.	Unit
System Power Supply Voltage	VDDIO	VSS=0	-0.3	4.0	V
Input Voltage	VIN	-	-0.3	5.0	V
Operating Temperature	T _{OP}	-	-20	70	°C
Storage Temperature	T _{ST}	-	-30	80	°C
Storage Humidity	HD	Ta=<40°C	20	90	%RH

1.4 DC Electrical Characteristics

Module VSS = 0V, Ta = 25°C

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Power Supply Voltage1	VDDIO	-	3.0	3.3	3.6	V
V _{COM} High Voltage	V_{COMH}	-	-	-	5.54	V
V _{COM} Low Voltage	V_{COML}	-	-2.8	-	-	V
Input High Voltage	VIH	-	0.8×VDDIO	-	VDDIO	٧
Input Low Voltage	VIL	-	0	-	0.2×VDDIO	٧
Output High Voltage	VOH	-	0.9xVDDIO	-	VDDIO	V
Output Low Voltage	VOL	-	-	-	0.1xVDDIO	٧
		VDDIO=3.3 V		7.6		mA
Supply Current	t IDD	Pattern=full display	-	7.0	-	IIIA
Supply Current	IDD	VDDIO=3.3 V		8.5	13	mA
		Pattern= black *1	-	0.0	13	ША
Power Consumption	PW	-	-	28.1	-	mW

Note1:Maximum current display



1.5 Optical Characteristics

TFT LCD Module

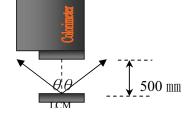
VDDIO=3.3V, Ta=25°C

Item		Symbol	Condition	Min.	Тур.	Max.	unit	-
Response time		Tr+ Tf	Ta = 25° C θ X, θ Y = 0°	ı	35	53	ms	Note2
	Тор	θΥ+		ı	45	-		
Viewing angle	Bottom	θΥ-	CR ≥ 10	ı	50	-	Deg.	Note4
viewing angle	Left	θΧ-	CR 2 10	ı	50	-	Deg.	NOIE4
	Right	θX+		-	50	-		
Contrast rati	0	CR		200	250	-	-	Note3
	White	Х	Ta = 25°C θX , θY = 0°	0.24	0.29	0.34		
	vviile	Υ		0.26	0.31	0.36		
	Red	Х		0.57	0.62	0.67		
Color of CIE Coordinate		Υ		0.31	0.36	0.41		
(With B/L)	Croon	Х	0,7,01 - 0	0.27	0.32	0.37	_	
(*************************************	Green	Υ		0.56	0.61	0.66		
	Dluc	Х		0.09	0.14	0.19		Note1
	Blue			0.03	0.08	0.13		
Average Brightness Pattern=white display (With B/L) *1		IV	IF=20 mA	240	280	-	cd/m ²	
Uniformity (With B/L)*1		∆В	IF=20 mA	70	-	-	%	

Note1:

- 1: $\triangle B=B(min) / B(max)$
- 2 : Measurement Condition for Optical Characteristics:3 :
 - a : Environment: 25°C±5°C / 60±20%R.H → no wind → dark room below 10 Lux at typical lamp current and typical operating frequency.
 - b : Measurement Distance: 500 \pm 50 mm \rightarrow (θ = 0°)
 - c: Equipment: TOPCON BM-7 fast, (field 1°), after 10 minutes operation.
 - d: The uncertainty of the C.I.E coordinate measurement ±0.01, Average Brightness ± 4%





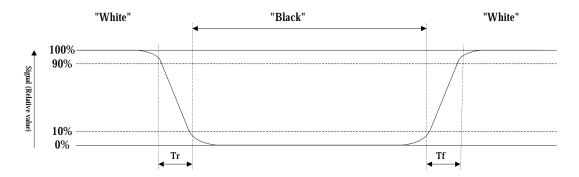
Colorimeter=BM-7 fast



Note2: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of Amplitudes.

Refer to figure as below:



Note3: Definition of contrast ratio:

Contrast ratio is calculated with the following formula

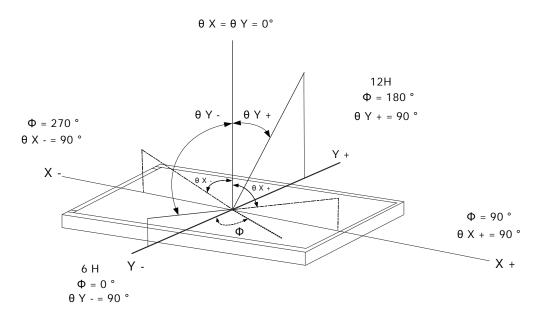
Photo detector output when LCD is at "White" state

Contrast ratio (CR) =

Photo detector output when LCD is at "Black" state

Note4: Definition of viewing angle:

Refer to figure as below:





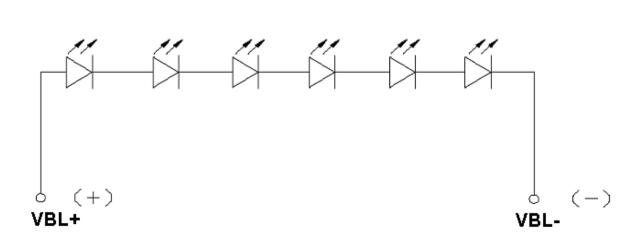
1.6 Backlight Characteristics

Maximum Ratings

Maximan Ratingo					
Item	Symbol	Conditions	Min.	Max.	Unit
Forward Current	IF	Ta =25°ℂ	-	30	mA
Reverse Voltage	VR	Ta =25°ℂ	-	30	V
Forward Voltage	VF	Ta =25°ℂ	-	24	V
Power Dissipation	PD	Ta =25°ℂ	-	720	mW

Electrical / Optical Characteristics

Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
Forward Voltage	VF		18.6	19.8	21.6	V
Average Brightness (without LCD)	IV	IF= 20 mA	3500	4300	-	cd/m ²
CIE Color Coordinate	X		-	0.29	-	
(Without LCD)	Y		-	0.29	-	_
Color			White			





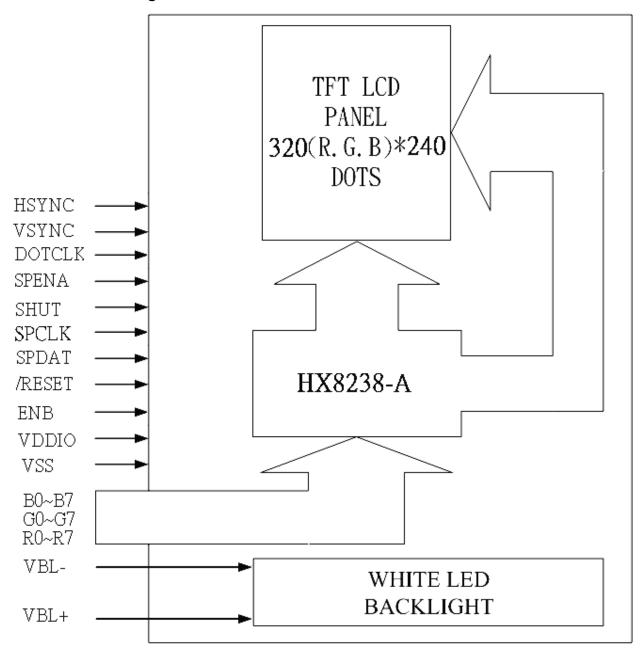
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

2.1.2 Block Diagram





2.2 Interface Pin Description

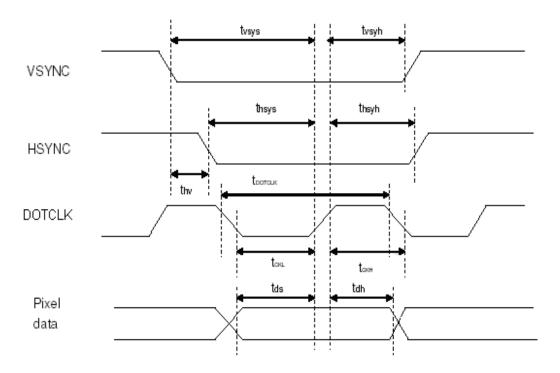
1 VBL- 2 VBL- 3 VBL+ 4 VBL+ 5 NC 6 /RESET 7 NC	Power supply for LED Backlight cathode input Power supply for LED Backlight cathode input Power supply for LED Backlight anode input Power supply for LED Backlight anode input Not used , Must be open Hardware reset
3 VBL+ 4 VBL+ 5 NC 6 /RESET 7 NC	Power supply for LED Backlight anode input Power supply for LED Backlight anode input Not used , Must be open
4 VBL+ 5 NC 6 /RESET 7 NC	Power supply for LED Backlight anode input Not used , Must be open
5 NC 6 /RESET 7 NC	Not used , Must be open
6 /RESET 7 NC	•
7 NC	Hardware reset
	Not used , Must be open. (Output Pin ,POL output.)
8 Y1	Not used
9 X1	Not used
10 Y2	Not used
11 X2	Not used
12 B0	Blue data bit 0
13 B1	Blue data bit 1
14 B2	Blue data bit 2
15 B3	Blue data bit 3
16 B4	Blue data bit 4
17 B5	Blue data bit 5
18 B6	Blue data bit 6
19 B7	Blue data bit 7
20 G0	Green data bit 0
21 G1	Green data bit 1
22 G2	Green data bit 2
23 G3	Green data bit 3
24 G4	Green data bit 4
25 G5	Green data bit 5
26 G6	Green data bit 6
27 G7	Green data bit 7
28 R0	Red data bit 0
29 R1	Red data bit 1
30 R2	Red data bit 2



31 R3 Red data bit 3 32 R4 Red data bit 4 33 R5 Red data bit 5 34 R6 Red data bit 6 35 R7 Red data bit 7 36 HSYNC Horizontal sync input 37 VSYNC Vertical sync input 38 DOTCLK Dot data clock 39 VDDIO Digital power 40 VDDIO Digital power 41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 48 SHUT 48 SHUT 48 SHUT 51 NC Not USED , Was be provided to such pin when IC power on. Internal pull low. 52 Connect to VSS for normal operating mode (Refer to Power Up Sequence) 53 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground			
33 R5 Red data bit 5 34 R6 Red data bit 6 35 R7 Red data bit 7 36 HSYNC Horizontal sync input 37 VSYNC Vertical sync input 38 DOTCLK Dot data clock 39 VDDIO Digital power 40 VDDIO Digital power 41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 48 SHUT 48 SHUT 48 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	31	R3	Red data bit 3
34 R6 Red data bit 6 35 R7 Red data bit 7 36 HSYNC Horizontal sync input 37 VSYNC Vertical sync input 38 DOTCLK Dot data clock 39 VDDIO Digital power 40 VDDIO Digital power 41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 48 SHUT 48 SHUT 48 SHUT 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	32	R4	Red data bit 4
35 R7 Red data bit 7 36 HSYNC Horizontal sync input 37 VSYNC Vertical sync input 38 DOTCLK Dot data clock 39 VDDIO Digital power 40 VDDIO Digital power 41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 48 SHUT 48 SHUT 48 SHUT 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	33	R5	Red data bit 5
36 HSYNC Horizontal sync input 37 VSYNC Vertical sync input 38 DOTCLK Dot data clock 39 VDDIO Digital power 40 VDDIO Digital power 41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 48 SHUT 48 SHUT 48 SHUT 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	34	R6	Red data bit 6
37 VSYNC Vertical sync input 38 DOTCLK Dot data clock 39 VDDIO Digital power 40 VDDIO Digital power 41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	35	R7	Red data bit 7
38 DOTCLK Dot data clock 39 VDDIO Digital power 40 VDDIO Digital power 41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	36	HSYNC	Horizontal sync input
39 VDDIO Digital power 40 VDDIO Digital power 41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 48 Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. 48 Internal pull low. 49 Connect to VDDIO for sleep mode 49 CONNECT (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	37	VSYNC	Vertical sync input
40 VDDIO Digital power 41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low. - Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	38	DOTCLK	Dot data clock
41 VDDIO Digital power 42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low. - Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	39	VDDIO	Digital power
42 VDDIO Digital power 43 SPENA Serial port data enable signal 44 NC Not used, Must be open 45 NC Not used, Must be open (Output Pin, VGL, Gate off power.) 46 NC Not used, Must be open (Output Pin, VGH, Gate on power.) 47 NC Not used, Must be open (Output Pin, VGH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low. - Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used, Must be open (Output Pin, VCOM power.) 52 ENB Data enable control 53 VSS Ground	40	VDDIO	Digital power
43 SPENA Serial port data enable signal 44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low. - Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	41	VDDIO	Digital power
44 NC Not used , Must be open 45 NC Not used , Must be open (Output Pin ,VGL ,Gate off power.) 46 NC Not used , Must be open 47 NC Not used , Must be open (Output Pin ,VGH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	42	VDDIO	Digital power
NC Not used, Must be open (Output Pin, VGL, Gate off power.) NC Not used, Must be open (Output Pin, VGH, Gate on power.) NC Not used, Must be open (Output Pin, VGH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low. Connect to VDDIO for sleep mode Connect to VSS for normal operating mode (Refer to Power Up Sequence) SPCLK Serial data clock SPDAT Serial data NC Not used, Must be open (Output Pin, VCOM power.) ENB Data enable control VSS Ground	43	SPENA	Serial port data enable signal
46 NC Not used, Must be open 47 NC Not used, Must be open (Output Pin, VgH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used, Must be open (Output Pin, VCOM power.) 52 ENB Data enable control 53 VSS Ground	44	NC	Not used, Must be open
NC Not used , Must be open (Output Pin ,VGH, Gate on power.) Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	45	NC	Not used , Must be open (Output Pin ,V _{GL} ,Gate off power.)
Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low. - Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	46	NC	Not used, Must be open
falling edge must be provided to such pin when IC power on. Internal pull low Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence) 49 SPCLK Serial data clock 50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	47	NC	Not used , Must be open (Output Pin ,Vgн, Gate on power.)
50 SPDAT Serial data 51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	48	SHUT	falling edge must be provided to such pin when IC power on. Internal pull low Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode
51 NC Not used , Must be open (Output Pin ,VCOM power.) 52 ENB Data enable control 53 VSS Ground	49	SPCLK	Serial data clock
52 ENB Data enable control 53 VSS Ground	50	SPDAT	Serial data
53 VSS Ground	51	NC	Not used , Must be open (Output Pin ,VCOM power.)
	52	ENB	Data enable control
54 VSS Ground	53	VSS	Ground
	54	VSS	Ground



2.3 Timing Characteristics



Pixel timing

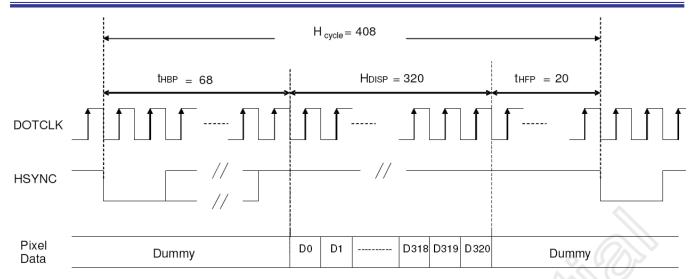
Characteristics	Symbol	M	in	Ty	/p	Max		Unit
Characteristics	Symbol	24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	Ollit
DOTCLK Frequency	fDOTCLK	-		6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33,3	154	51.3	-		ns
Vertical Sync Setup Time	tvsys	20	10	,		•		ns
Vertical Sync Hold Time	tvsyh	20	10	-		-		ทร
Horizontal Sync Setup Time	thsys	20	10			•		ns
Horizontal Sync Hold Time	thsyh	20	10					ns
Phase difference of Sync Signal Falling Edge	thv		1			240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-		-		ns
DOTCLK High Period	tCKH	50	15	٠		•		ns
Data Setup Time	tds	12	10	-		-		ns
Data hold Time	tdh	12	10	•		•		ns
Reset pulse width	tRES	1	0					us

Note: External clock source must be provided to DOTCLK pin of HX8238-A. The driver will not operate if absent of the clocking signal.

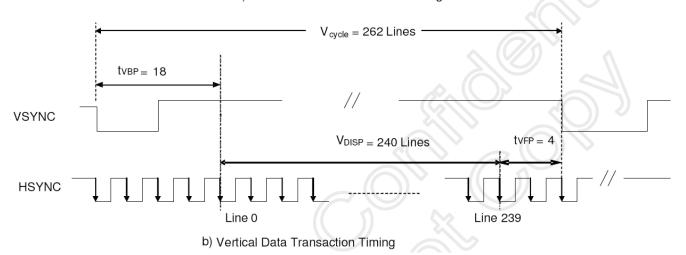
Pixel timing

Note: The interface of this module can drive by digital 24-bit data.





a) Horizontal Data Transaction Timing

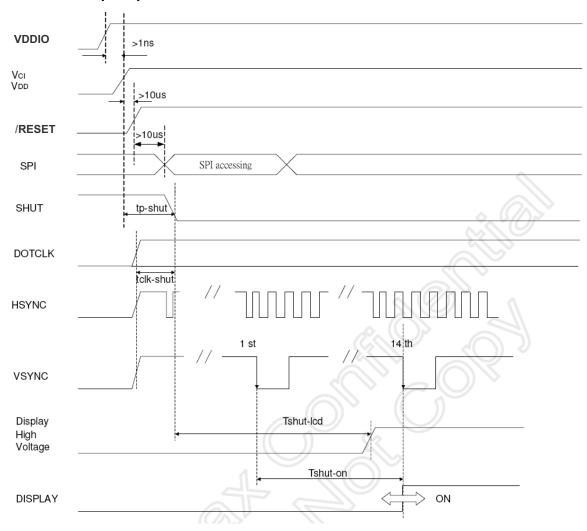


Data transaction timing in parallel RGB(24 bit)interface (SYNC mode)



2.4 Power Sequence

2.4.1 Power up sequence



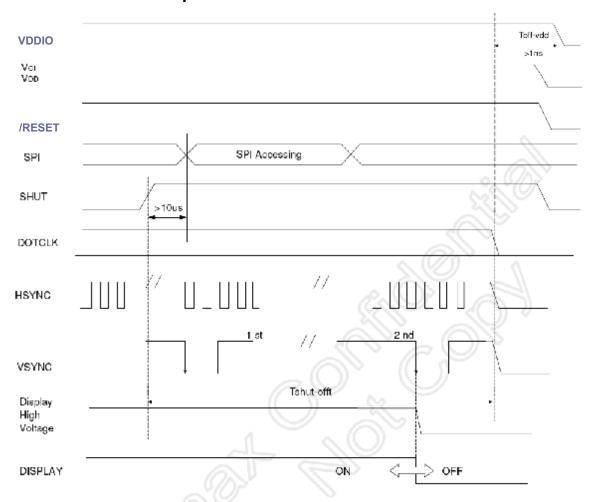
Characteristics	Symbol	Min	Тур	Max	Units
VDDD / VDDIO on to falling edge of SHUT	tp-shut	1	-	-	us
DOTCLK	tclk-shut	1	•	-	clk
Falling edge of SHUT to LCD power on	tshut-lcd	-	1	128	ms
Falling edge of SHUT to display start		-	ı	14	frame
- 1 line: 408 clk - 1 frame: 262 line -DOTCLK = 6.5MHz	tshut-on	-	166	232.4	ms

Note: It is necessary to input DOTCLK before the falling edge of SHUT.

Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.



2.4.2 Power down sequence



Characteristics	Symbol	Min	Тур	Max	Uni
Rising edge of SHUT to display off		2	-	-	frame
- 1 line: 408 clk	tshut-off				
- 1 frame: 262 line	torial on	33.4	-	-	ms
- DOTCLK = 6.5MHz					
Input-signal-off to VDDD / VDDIO off	toff-vdd	1	-	-	us

Note: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

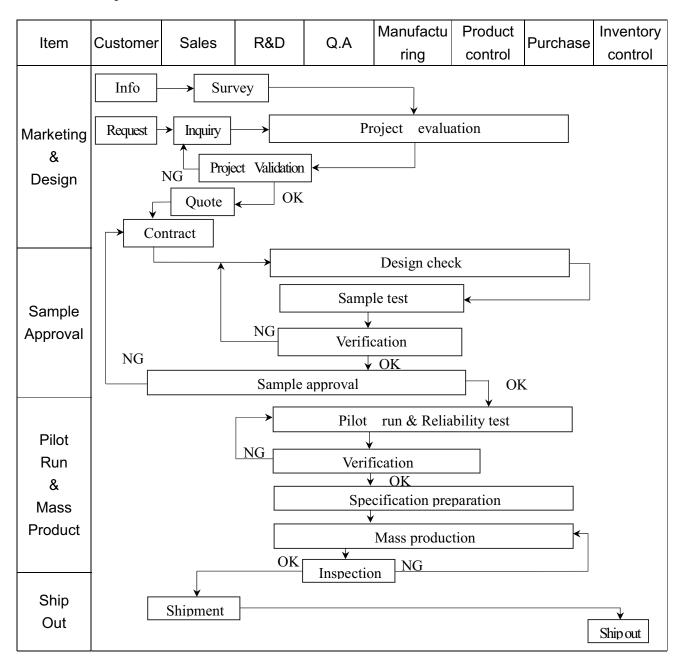
Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

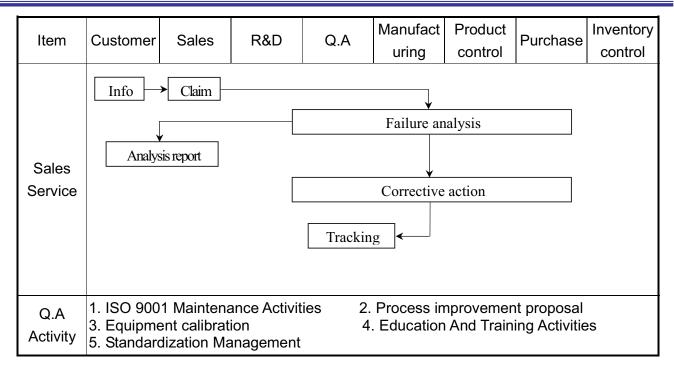


3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart





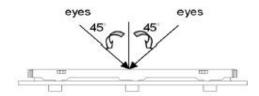




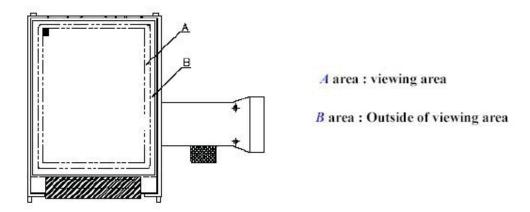
3.2 Inspection Specification

1. Inspection Specification

- ◆Scope : The document shall be applied to TFT-LCD Module for 3. 5" ~10" (Ver. 02).
- ◆Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.
- ◆Equipment: Gauge · MIL-STD · Powertip Tester · Sample
- ◆Defect Level: Major Defect AQL: 0.4 ; Minor Defect AQL: 1.5
- **♦**OUT Going Defect Level: Sampling.
- Standard of the product appearance test:
 - a. Manner of appearance test:
 - (1). The test best be under 20W×2 fluorescent light, and distance of view must be at 30 cm.
 - (2). The test direction is base on about around 45° of vertical line.



(3). Definition of area.



(4). Standard of inspection: (Unit: mm)



◆Specification For TFT-LCD Module 3, 5" ~10":

NO	Item			Criteri	on		Level
		I	1. 1The part number is inconsistent with work order of production.				
01	Product condition	1. 2 Mix	ked prod	uct types.			Major
		1. 3 Asse	embled i	n inverse direction.			Major
02	Quantity	2. 1The	quantity	y is inconsistent with	work order of producti	ion.	Major
03	Outline dimension		duct dir gram.	mension and structu	ure must conform to st	ructure	Major
		4. 1 Mis	4. 1 Missing line character and icon.				Major
		4, 2 No function or no display.					Major
04	Electrical Testing	4. 3 Display malfunction.					Major
		4. 4 LCD viewing angle defect.					Major
		4. 5 Current consumption exceeds product specifications.					Major
				Item	Acceptance (Q'ty)		
	Dot defect			Bright Dot	≦ 4		
	Dotacie		Dot	Dark Dot	≦ 5		
	(Bright dot \		Defect	Joint Dot	≦ 3		
05	Dark dot)			Total	≦ 7		Minor
	On -display	5. 1 Inspection pattern: full white, full black, Red, Green an				een and	
	blue screens.						
			5. 2 It is defined as dot defect if defect area $>1/2$ dot.				
		5. 3 The	distanc	e between two dot d	efect ≧5 mm.		



◆ Specification	For'	TET.	CD	Modulo	2 5"	-10"	
 Specification 	For	1 1 1-1	LCD	Module	3.5	~ [[] "	٠

NO	Item		Cr	iterion		Level
06	Black or white dot \ scratch \ contamination Round type \[\begin{array}{c} \ X & \ \ \ Y & \ \ \ \ \ \ \ \ \ \ \ \ \ \		$\Phi \leq 0.25$ $\Phi \leq 0.50$ $\Phi > 0.50$ Total Width $\Phi = 0.05$ $\Phi = 0.50$ $\Phi = 0.50$ $\Phi = 0.50$	isplay): (W) ≤ 0.03 ≤ 0.05	Acceptance (Q'ty) Ignore 5 0 5 Acceptance (Q'ty) Ignore 4 2 As round type 5	Minor
07	Polarizer Bubble	0. 25 < 0. 50 <	Dimension (diameter : Φ) $Φ \le 0.25$ $0.25 < Φ \le 0.50$ $0.50 < Φ \le 0.80$ $Φ > 0.80$ Total		eptance (Q'ty) Ignore 4 1 0 5	Minor



◆Specification For TFT-LCD Module 3, 5" ~10":

NO	Item	Criterion	Level
08	The crack of glass	Symbols: X: The length of crack Z: The thickness of crack t: The thickness of glass 8.1 General glass chip: 8.1.1 Chip on panel surface and crack between panels: SP Y IOK Seal width X: The width of crack. W: terminal length a: LCD side length ING ING ING Seal width X Y: The width of crack. W: terminal length a: LCD side length ING ING ING ING ING ING ING IN	Minor
		X Y Z	
		≤ a Crack can't enter viewing area ≤1/2 t	
		\leq a Crack can't exceed the half of SP width. 1/2 t < Z \leq 2 t	



◆Specification For TFT-LCD Module 3, 5" ~10": (Ver.						
NO	Item	Criterion				
		Symbols: X: The length of crack Z: The thickness of crack t: The thickness of glass 8.1.2 Corner crack:				
		X Y Z				
		$\leq 1/5$ a Crack can't enter viewing area $Z \leq 1/2$ t				
		$\leq 1/5$ a Crack can't exceed the half of SP width. $1/2$ t $<$ Z ≤ 2 t				
08	The crack of glass	8.2 Protrusion over terminal: 8.2.1 Chip on electrode pad: X Y Z	Minor			
		W Y W				
		$\begin{array}{c cccc} X & Y & Z \\ \hline Front & \leq a & \leq 1/2 \text{ W} & \leq t \end{array}$				
		Back $\leq a$ $\leq W$ $\leq 1/2 t$				



igspaceSpecification For TFT-LCD Module 3. 5" ~10":

NO	Item	Criterion			
		Symbols: X: The length of crack Z: The thickness of crack t: The thickness of glass 8.2.2 Non-conductive portion:	Level		
08	The crack of glass	X Y Z ≤ 1/3 a ≤ W ≤t O If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode towning laws if instance.	Minor		
		terminal specifications. 8, 2, 3 Glass remain: Y Pitch			
		$\begin{array}{c cccc} X & Y & Z \\ & \leq a & \leq 1/3 \text{ W} & \leq t \end{array}$	5		



◆Specification For TFT-LCD Module 3. 5" ~10":

NO	Item	Criterion	Level
		9, 1 Backlight can't work normally.	Major
09	Backlight elements	9. 2 Backlight doesn't light or color is wrong.	Major
		9, 3 Illumination source flickers when lit.	Major
		10. 1 Pin type \quantity \quantity \dimension must match type in structure diagram.	Major
	General appearance	10, 2 No short circuits in components on PCB or FPC .	Major
		10.3 Parts on PCB or FPC must be the same as on the production characteristic chart .There should be no wrong parts , missing parts or excess parts.	Major
10		10. 4 Product packaging must the same as specified on packaging specification sheet.	Minor
		10.5 The folding and peeled off in polarizer are not acceptable.	Minor
		10. 6 The PCB or FPC between B/L assembled distance(PCB or FPC) is ≤ 1.5 mm.	Minor



4. RELIABILITY TEST

Ver.02

4.1 Reliability Test Condition

NO.	TEST ITEM	TEST CONDITION				
1	High Temperature Storage Test	Keep in +80 ±2°C 96 hrs Surrounding temperature, then storage at normal condition 4hrs.				
2	Low Temperature Storage Test	Keep in -30 ±2°C 96 hrs Surrounding temperature, then st	orage at normal condition 4hrs.			
3	High Temperature / High Humidity Storage Test	Keep in +60°C / 90% R.H duration Surrounding temperature, then state (Excluding the polarizer)				
		Air Discharge: Apply 2 KV with 5 times Discharge for each polarity +/- Contact Discharge: Apply 250 V with 5 times discharge for each polarity				
4	ESD Test	 Temperature ambiance: 15°C ~35°C Humidity relative: 30%~60% Energy Storage Capacitance(Cs+Cd): 150pF±10% Discharge Resistance(Rd): 330Ω±10% Discharge, mode of operation: Single Discharge (time between successive discharges at least 1 sec) (Tolerance if the output voltage indication: ±5%) 				
5	Temperature Cycling Storage Test	$-20^{\circ}\text{C} \rightarrow +25^{\circ}\text{C} \rightarrow +70^{\circ}\text{C} \rightarrow +25^{\circ}\text{C}$ $(30\text{mins}) (5\text{mins}) (5\text{mins})$ 10 Cycle Surrounding temperature, then storage at normal condition 4hrs.				
6	Vibration Test (Packaged)	 Sine wave 10~55 Hz frequence The amplitude of vibration :1. Each direction (X \ Y \ Z) du 	5 mm			
		Packing Weight (Kg)	Drop Height (cm)			
		0 ~ 45.4	122			
7	Drop Test	45.4 ~ 90.8	76			
	(Packaged)	90.8 ~ 454	61			
		Over 454	46			
		Drop direction: 1 corner / 3 edg	ges / 6 sides each 1times			



5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

- 5.1.1 If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
- 5.1.2 If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

5.2 HANDLING

- 5.2.1 Avoid any strong mechanical shock which can break the glass.
- 5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module, be sure to ground your body and any electrical equipment you may be using.
- 5.2.3 Do not remove the panel or frame from the module.
- 5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully ,do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)
- 5.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
- 5.2.6 Do not touch the display area with bare hands, this will stain the display area.
- 5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.
- 5.2.8 To control temperature and time of soldering is 320±10°C and 3-5 sec.
- 5.2.9 To avoid liquid (include organic solvent) stained on LCM.

5.3 STORAGE

- 5.3.1 Store the panel or module in a dark place where the temperature is 25° C $\pm 5^{\circ}$ C and the humidity is below 65% RH.
- 5.3.2 Do not place the module near organics solvents or corrosive gases.
- 5.3.3 Do not crush, shake, or jolt the module.

5.4 TERMS OF WARRANTY

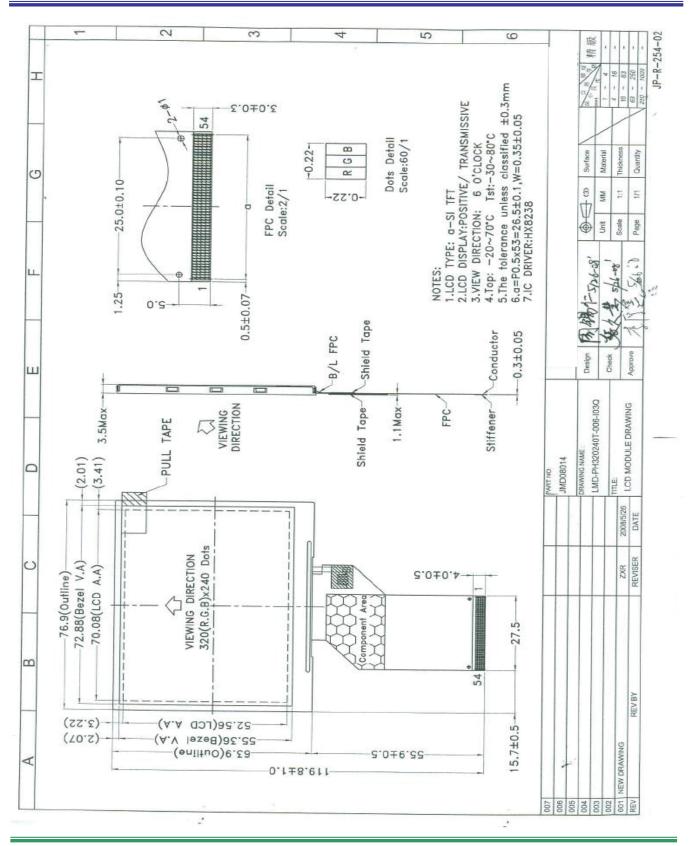
5.4.1 Applicable warrant period

The period is within thirteen months since the date of shipping out under normal using and storage conditions.

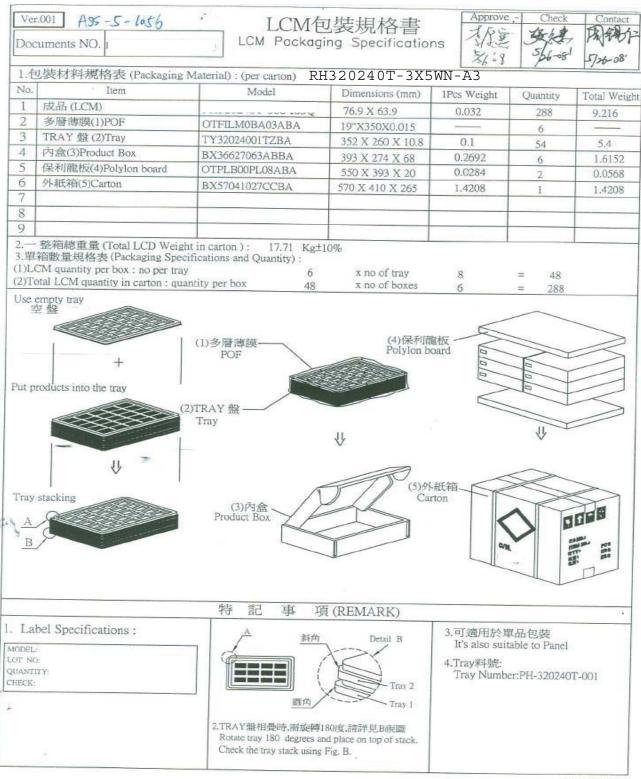
5.4.2 Unaccepted responsibility

This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment, fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.









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