RadHard-by-Design Analog

RHD5912

Quad Comparator, Open Drain Outputs
Released Datasheet
Cobham.com/HiRel
March 28, 2016

The most important thing we build is trust

FEATURES

- ❑ Single power supply operation at 3.3V or 5.0V
- ❑ Radiation performance
  - Total dose: > 1 Mrad(Si); Dose rate = 50-300 rad(Si)/s
  - ELDRS Immune
  - SEL Immune > 100 MeV-cm^2/mg
  - Neutron Displacement Damage > 10^{14} neutrons/cm^2
- ❑ Short Circuit Tolerant
- ❑ Full military temperature range
- ❑ Designed for aerospace and high reliability space applications
- ❑ Packaging – Hermetic ceramic SOIC
  - 16-pin, .417"L x .300"W x .120"Ht
  - Weight - 0.8 grams max
- ❑ **Radiation Hardness Assurance Plan: DLA Certified to MIL-PRF-38534, Appendix G.**

GENERAL DESCRIPTION

The RHD5912 is a radiation hardened, single supply, quad comparator with open drain outputs in a 16-pin SOIC package. The RHD5912 design uses specific circuit topology and layout methods to mitigate total ionizing dose effects and single event latchup. These characteristics make the RHD5912 especially suited for the harsh environment encountered in Deep Space missions. It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD5912 is ideal for demanding military and space applications.

ORGANIZATION AND APPLICATION

The RHD5912 quad comparator is intended for operation with dynamic signals on either or both inputs. Comparison is 'continuous', that is, the circuit functions as high gain open loop amplifiers with a digital output. For slow input signals with small input differences the comparators can be expected to respond to small noise signals at the inputs. Although there is internal hysteresis, feedback hysteresis is the responsibility of the user to avoid 'chattering' on system noise.

The comparator will accept signals anywhere in the included power supply range. The circuit delay is specified for a half-volt single ended or differential input step of either polarity ending in an input polarity reversal of 10mV. See Switching Diagrams.

CMOS device drive has a negative temperature coefficient and the devices are therefore inherently tolerant to momentary shorts, although on chip thermal shutdown is not provided. All inputs and outputs are diode protected

The devices will not latch with SEU events above 100 Mev-cm^2/mg. Total dose degradation is minimal to above 1 Mrad(Si). Displacement damage environments to neutron fluence equivalents in the mid 10^{14} neutrons per cm^2 range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependent.

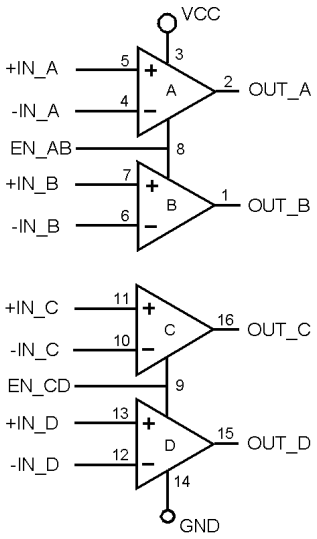
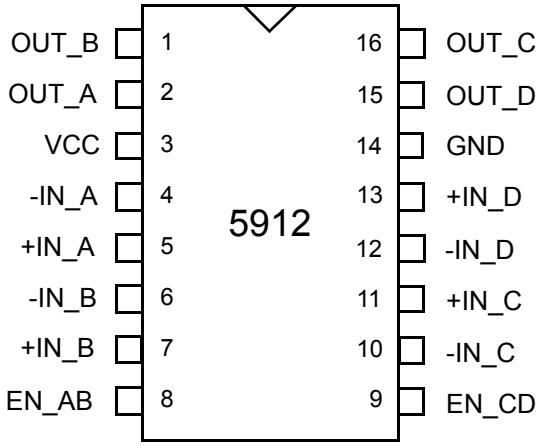


FIGURE 1: BLOCK DIAGRAM



16-Pin SOIC

FIGURE 2: PACKAGE PIN-OUT

Notes:

1. Package and Lid are electrically isolated from signal pads.
2. It is recommended that the Lid be grounded to prevent any ESD or static buildup.
3. EN_AB enables Comparators A & B. EN_CD enables Comparators C & D.

Pin	Signal Name	Definition
1	OUT_B	Output of Comparator B.
2	OUT_A	Output of Comparator A.
3	VCC	DC Supply Voltage.
4	-IN_A	Inverting input of Comparator A.
5	+IN_A	Non-Inverting input of Comparator A.
6	-IN_B	Inverting input of Comparator B.
7	+IN_B	Non-Inverting input of Comparator B.
8	EN_AB	A Logic Low will disable Comparator A & B so that the outputs are high impedance.
9	EN_CD	A Logic Low will disable Comparator C & D so that the outputs are high impedance.
10	-IN_C	Inverting input of Comparator C.
11	+IN_C	Non-Inverting input of Comparator C.
12	-IN_D	Inverting input of Comparator D.
13	+IN_D	Non-Inverting input of Comparator D.
14	GND	DC Supply Return.
15	OUT_D	Output of Comparator D.
16	OUT_C	Output of Comparator C.

FIGURE 3: PIN-OUT DESCRIPTION

ABSOLUTE MAXIMUM RATINGS

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	+150	°C
Supply Voltage (+VCC)	+7.0	V
Input Voltage	VCC +0.4 GND -0.4	V V
Lead Temperature (soldering, 10 seconds)	300	°C
Thermal Resistance, Junction-to-Case ΘJC	7	°C/W
Power @ 25°C	250	mW

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Typical	Units
+VCC	Power Supply Voltage	3.3 to 5.0	V
VCM	Input Common Mode Range	(VCC - 1.5) to GND	V

ELECTRICAL PERFORMANCE CHARACTERISTICS

(TC = -55°C TO +125°C, +VCC = +5.0V -- UNLESS OTHERWISE SPECIFIED)

Parameter	Symbol	Conditions	Min	Max	Units
Quiescent Supply Current 1/	ICCQ	EN = 1, NO LOAD		3	mA
		EN = 0 2/		300	nA
Input Offset Voltage 1/	VOS		-20	20	mV
Input Offset Current 1/, 3/	IOS	TC = +25°C, +125°C	-10	10	nA
Input Bias Current 1/, 3/	IB	TC = +25°C, +125°C	-10	10	nA
Common Mode Rejection Ratio 1/	CMRR		50		dB
Power Supply Rejection Ratio 1/	PSRR		70		dB
Output Voltage Low 1/	VOL	IOUT = 5mA		0.25	V
		IOUT = 10mA		0.44	V
		IOUT = 20mA		1.00	V
Gain 1/	A		5		V/mV
Output Leakage Current 1/, 3/	ILKOUT	VOUT = VCC, TC = +25°C, +125°C		100	nA
Short Circuit Output Current 2/	IO(SINK)		-35	-60	mA
Input Voltage - Enable (EN_AB, EN_CD)	VHI	High (Enabled)	3.5		V
	VLO	Low (Disabled)		1.5	V
Input Current - Enable (EN_AB, EN_CD) 3/	IEN	TC = +25°C, +125°C		10	nA

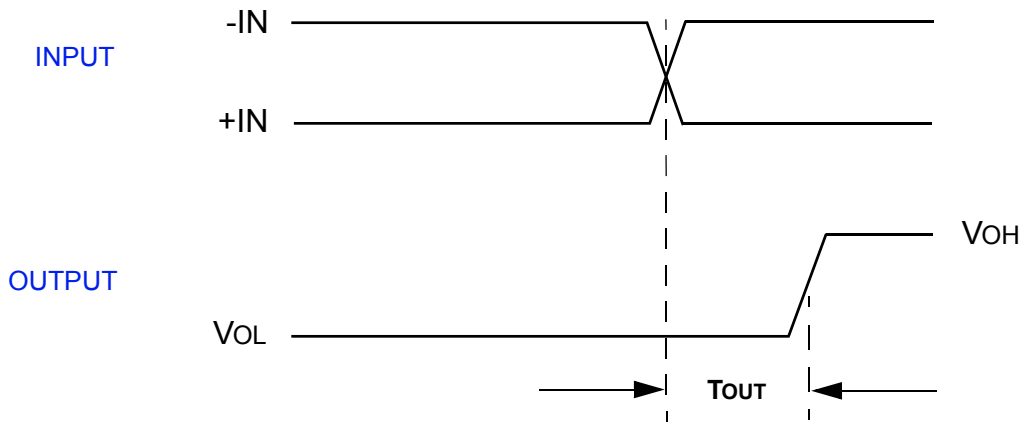
Notes: 1/ Specification derated to reflect Total Dose exposure to 1 Mrad(Si) @ 25°C.
2/ Not tested. Shall be guaranteed by design, characterization or correlation to other test parameters.
3/ Subgroup 3 for these parameters is guaranteed, but not production tested.

SWITCHING CHARACTERISTICS

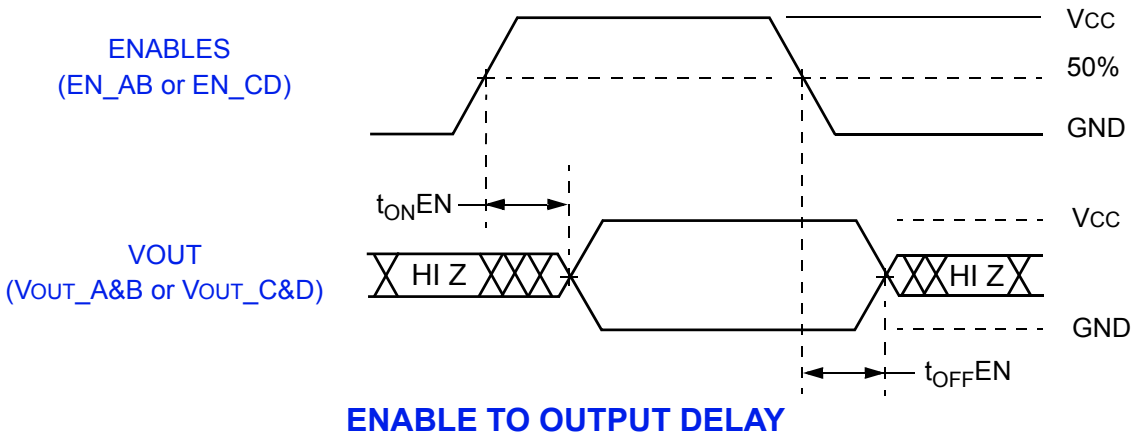
(TC = -55°C TO +125°C, +VCC = +5.0V -- UNLESS OTHERWISE SPECIFIED)

Parameter	Symbol	Conditions	Min	Max	Units
Output Delay (Switching)	TOUT	1/		300	ns
Output Delay (Enabled)	$t_{ON}EN$			500	ns
Output Delay (Disabled)	$t_{OFF}EN$			100	ns

Note:
1/ The circuit delay is specified for a half-volt single ended or differential input step, of either polarity, ending in an input polarity reversal of 10mV.



INPUT TO OUTPUT DELAY



ENABLE TO OUTPUT DELAY

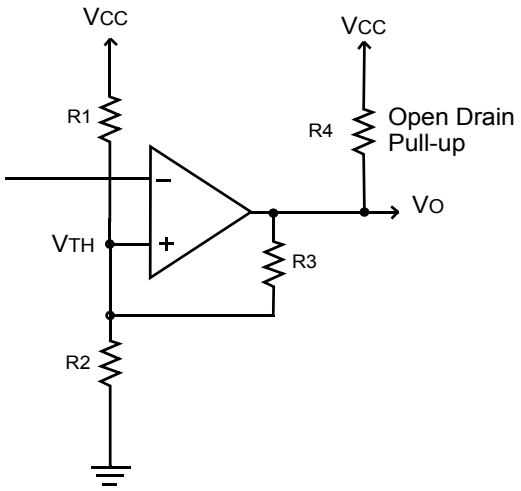
FIGURE 4: RHD5912 SWITCHING DIAGRAMS

Threshold Voltage

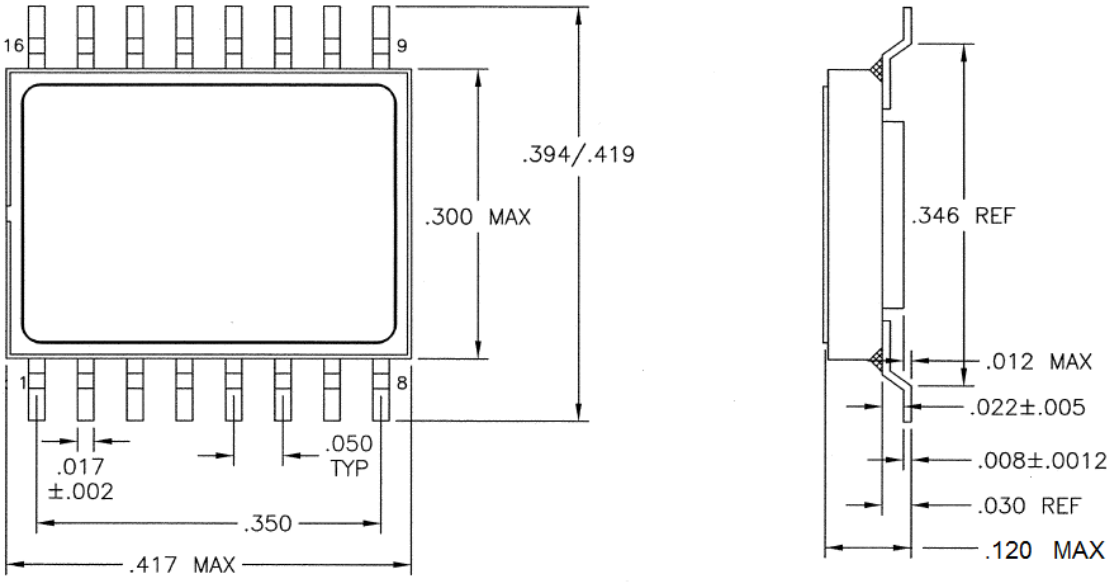
$$V_{TH} = Vcc\frac{R2}{R1+R2}$$

Hysteresis Calculation

$$HYS = V_O\frac{R2}{R2+R3}$$



APPLICATION NOTE 1: HYSTERESIS



Note: Package and lid are electrically isolated from signal pads.

FIGURE 5: PACKAGE OUTLINE

ORDERING INFORMATION

Model	DLA SMD #	Screening	Package
RHD5912-7	-	Commercial Flow, +25°C testing only	16-pin SOIC Package
RHD5912-S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RHD5912-201-1S	5962-1024203KXC	In accordance with DLA SMD	
RHD5912-201-2S	5962-1024203KXA		
RHD5912-901-1S	5962H1024203KXC	In accordance with DLA Certified RHA Program Plan to RHA Level "H", 1 Mrad(Si)	
RHD5912-901-2S	5962H1024203KXA		

REVISION HISTORY

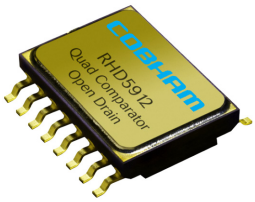
Date	Revision	Change Description
03/28/2016	D	Import into Cobham format

Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel



EXPORT CONTROL:

This product is controlled for export under the Export Administration Regulations (EAR), 15 CFR Parts 730-774.
A license from the Department of Commerce may be required prior to the export of this product from the United States.

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