Standard Products

*Datasheet*

# RadHard-by-Design RHD5958 8-Channel Multiplexed 14-Bit Analog-to-Digital Converter

**www.aeroflex.com/RHDseries**

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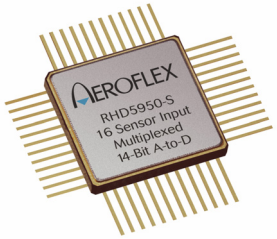



## FEATURES

- Single power supply operation 5.0V or Dual power supply for 3.3V I/O
- Radiation performance
  - Total dose: > 1 Mrad(Si); Dose rate = 50 - 300 rads(Si)/s
  - ELDRS Immune
  - SEL Immune > 100 MeV-cm$^2$/mg
  - Neutron Displacement Damage > $10^{14}$ neutrons/cm$^2$
- 8-Channel Input Multiplexer
- Successive Approximation A-to-D
- Level Shifting Digital Output Drivers allow interfaces to 5.0 or 3.3 volt logic
- Tri-State digital outputs
- Power Down (Sleep) mode
- Single or continuous conversion
- 20us conversion period (20 clocks @ 1MHz Clock rate)
- Multiplexer address is latched on first clock rising edge of a cycle
- Busy and End-of-Conversion status outputs
- 2000V Input/Output ESD protection
- Full military temperature range
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic Ceramic
  - 40 leads, 0.600"Sq x 0.120"Ht quad flat pack
  - Weight - 6 grams max

- **Aeroflex Plainview's Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

## GENERAL DESCRIPTION

Aeroflex's RHD5958 is a radiation hardened, single supply, 8-Channel Multiplexed Analog-to-Digital converter in a 48-pin Ceramic Quad Flat Package. The RHD5958 design uses specific circuit topology and layout methods to mitigate total ionizing dose effects and single event latchup. These characteristics make the RHD5958 especially suited for the harsh environment encountered in Deep Space missions. It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD5958 is ideal for demanding military and space applications.

## ORGANIZATION AND APPLICATION

The RHD5958 takes 8 analog sensor signals and using 3 address inputs and an enable input, selects one of the 8 analog inputs and performs a 14-bit successive approximation analog-to-digital conversion in a nominal period of 20uS. The 14-bit digital output has a tri-state control allowing the connection of multiple RHD5958s. This provides the ability to interface many sensor voltage readings to the digital processor data bus. The full-scale range is determined by reference input voltages. The input impedance of the reference/span terminals is typically a constant 4K ohms.

Gain compression will occur near either power supply extremes but can be avoided if the references are more than 200mV away from the respective supply terminals. The input span can be less than 4 volts at the expense of ultimate resolution

The analog channels input impedance is primary capacitance (20pF typical). The input voltage charges a track-and-hold hold capacitor through transmission gates. The input bandwidth is determined by the slew rate of the hold amplifier and is adequate to allow input sampling in three clock periods (3uS nominal). The ultimate bandwidth is determined by the aperture uncertainty associated with the closing of the sample gate (approximately 5nS). The converter bandwidth is then determined by the sampling Nyquist frequency rather than the input signal; change rate (dv/dt) and the LSB weight in volts as would be the case if there were no sample and hold.

Start-Convert (STCNV_H), Busy (BUSY_L) and End-Of-Convert (EOC_H) status and control line are provided. The converter will operate in either continuous or single conversion modes. To operate in continuous mode, STCNV_H should be tied to BUSY_L. The digital output register changes at the end of a conversion and is available when EOC_H is asserted High. The output circuitry operates from a voltage independent of the remainder of the chip such that I/O is compatible with digital systems from, less than 3.3 volts, to 5 volts.

The converter divides the reference voltage into 16 segments with a linear weighted resistor network. The voltage on any segment is passed to a linear 10-bit DAC for interpolation. The architecture is inherently capable of monotonic operation. Typically INL is 0.12% FSR and DNL is < 0.03% FSR. The sampled input voltage is compared to the output of the two stage DAC for a 14-bit successive approximation conversion.

All inputs are protected to both power supply rails by semiconductor diodes. Inputs should be constrained to $V_{CC}$ +0.4 and GND-0.4 to avoid forward biasing protection paths.

The devices will not latch with SEU events to above 100 MeV-cm$^2$/mg. Total dose degradation is minimal to above 1 Mrad(Si). Displacement damage environments to neutron fluence equivalents in the mid $10^{14}$ neutrons per cm$^2$ range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependent.

Notes:
- The STCNV_H is a dynamic input (positive edge triggered) and should not be tied to a static voltage.
- The input signals should be low pass filtered to reduce high frequency noise
- If Sleep mode is enabled (EN_H=0), when waking up (EN_H=1), the unit has to complete an entire conversion cycle so the digital logic is in the proper state.

  Ex. If using a 1MHz clock; after EN_H=1 and 20us after STCNV_H is applied.

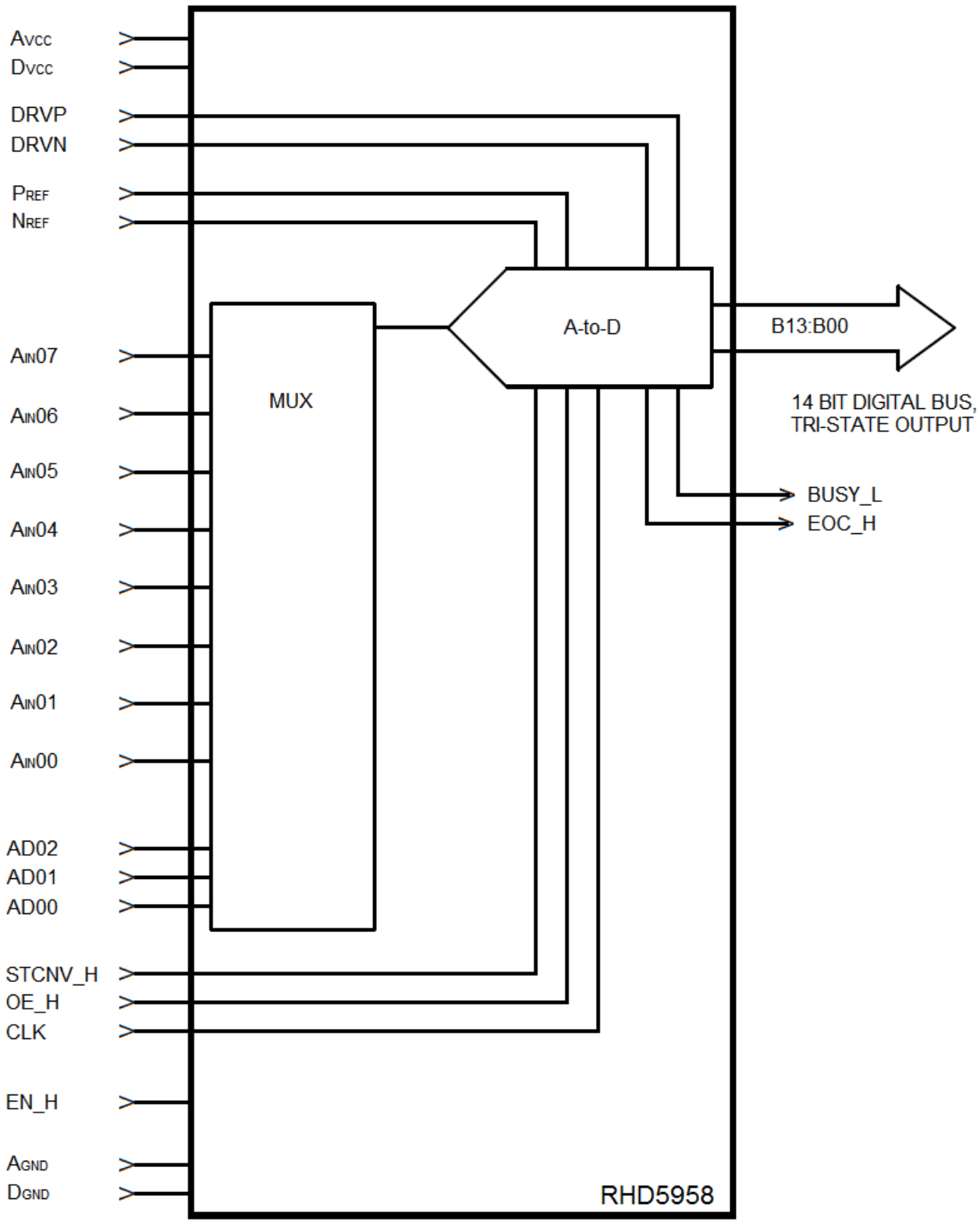



**FIGURE 1: BLOCK DIAGRAM**

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Range | Units |
|---|---|---|
| Case Operating Temperature Range | -55 to +125 | °C |
| Storage Temperature Range | -65 to +150 | °C |
| Junction Temperature | +150 | °C |
| Supply Voltage<br>VCC - GND | +6.0 | V |
| Input Voltage, PREF, NREF | VCC +0.4<br>GND -0.4 | V |
| Lead Temperature (soldering, 10 seconds) | 300 | °C |
| Thermal Resistance, Junction to Case, Θjc | 3.5 | °C/W |
| ESD Rating (per MIL-STD-883, Method 3015, Class 2) | 2,000 - 3,999 | V |

NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress rating only; functional operation beyond the “Operation Conditions” is not recommended and extended exposure beyond the “Operation Conditions” may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Typical | Units |
|---|---|---|---|
| +AVCC | Analog Power Supply Voltage | 5.0 | V |
| +DVCC | Digital Power Supply Voltage | 5.0 | V |
| DRVP | Digital Output High Reference Level | 3.3 to 5.0 | V |
| DRVN | Digital Output Low Reference Level | 0 | V |
| PREF | High Analog Reference Voltage | 4.5 | V |
| NREF | Low Analog Reference Voltage | 0.5 | V |

## ELECTRICAL PERFORMANCE CHARACTERISTICS

(TC = -55°C TO +125°C, +AVCC = +5.0V, +DVCC = +5.0V, +DRVP = +5.0V)

| Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Analog Supply Current Quiescent | AICCQ | VEN = DVCC, CLK = 0V | - | 10 | mA |
| Analog Supply Current Active | AICCA | VEN = DVCC | - | 10 | mA |
| Analog Supply Current Sleep | AICCS | VEN = DGND | - | 4 | mA |
| Digital Supply Current Quiescent | DICCQ | VEN = DVCC, CLK = 0V | - | 1 | mA |
| Digital Supply Current Active | DICCA | VEN = DVCC | - | 2 | mA |
| Digital Supply Current Sleep | DICCS | VEN = DGND | - | 1 | mA |
| Digital Output Supply Current Quiescent | IDRVPQ | VEN = DVCC, CL = 50pF, CLK = 0V | - | 0.1 | mA |
| Digital Output Supply Current Active | IDRVPA | VEN = DVCC, CL = 50pF | - | 1 | mA |
| Digital Output Supply Current Sleep | IDRVPS | VEN = DGND, CL = 50pF | - | 1 | mA |
| Full-scale Input Range | VIN | | VNREF | VPREF | V |
| Input Capacitance 2/ | CIN | TC = +25°C | - | 50 | pF |
| Analog Reference Impedance | ZREF | PREF to NREF | 2 | 6 | KΩ |
| High Analog Reference Current | IPREF | PREF - NREF = 4V | 0.67 | 2 | mA |
| High Analog Reference Voltage | VPREF | DVRP = 5.0 V | VNREF | 5.0 | V |
| | | DVRP = 3.3 V | VNREF | 5.0 | |
| Low Analog Reference Voltage | VNREF | DVRP = 5.0 V | 0 | VPREF | |
| | | DVRP = 3.3 V | 0 | VPREF | |

# ELECTRICAL PERFORMANCE CHARACTERISTICS

(TC = -55°C TO +125°C, +AVCC = +5.0V, +DVCC = +5.0V, +DRVP = +5.0V)

| Parameter | Symbol | Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| Integral Nonlinearity | INL | PREF-NREF = 4.5V | | - | 0.25 | %FSR |
| Differential Nonlinearity | DNL | PREF-NREF = 4.5V | | - | 0.05 | %FSR |
| Offset Error | OE | PREF-NREF = 4.5V | | - | 0.012 | %FSR |
| Gain Error | AE | PREF-NREF = 4.5V | | -0.006 | 0.006 | %FSR |
| Channel Isolation 2/ | ISO | TC = +25°C | | 80 | - | dB |
| Clock Frequency | fC | PREF-NREF = 4.5V | | - | 1 | MHz |
| Maximum Sampling Rate | fSAMPLE (MAX) | fC = 1 MHz, 20 clocks per conversion | | - | 50 | kSPS |
| High Input Leakage Current (AIN00-AIN07) 3/ | $I_{INLK_{HI}}$ | Input under test = AVCC, VEN = DVCC | +25°C | -5 | 5 | nA |
| | | | +125°C | -50 | 50 | |
| Low Input Leakage Current (AIN00-AIN07) 3/ | $I_{INLK_{LO}}$ | Input under test = AGND, VEN = DVCC | +25°C | -5 | 5 | |
| | | | +125°C | -50 | 50 | |
| Digital High Level Input Voltage EN_H, STCNV_H, OE_H, CLK, (AD00-AD02) | VIH | DVRP = 5.0 V | | 3.0 | - | V |
| | | DVRP = 3.3 V | | 2.2 | - | |
| Digital Low Level Input Voltage EN_H, STCNV_H, OE_H, CLK, (AD00-AD02) | VIL | DVRP = 5.0 V | | - | 2.0 | |
| | | DVRP = 3.3 V | | - | 1.2 | |
| Digital High Level Input Current EN_H, STCNV_H, OE_H, CLK, (AD00-AD02) 3/ | IIH | DVRP = 5.0 V<br>Digital input under test = 5.0 V<br>All other digital inputs = DGND | +25°C | -5 | 5 | nA |
| | | | +125°C | -50 | 50 | |
| Digital Low Level Input Current EN_H, STCNV_H, OE_H, CLK, (AD00-AD02) 3/ | IIL | DVRP = 5.0 V<br>All digital inputs = DGND | +25°C | -5 | 5 | |
| | | | +125°C | -50 | 50 | |
| Digital High Level Output Voltage (B00-B13) | VOH | DVRP = 5.0 V, VEN = DVCC, IOH = -1.0mA | | 4.6 | - | V |
| | | DVRP = 5.0 V, VEN = DVCC, IOH = -4.0mA | | 4.2 | - | |
| | | DVRP = 3.3 V, VEN = DVCC, IOH = -1.0mA | | 3.0 | - | |
| | | DVRP = 3.3 V, VEN = DVCC, IOH = -4.0mA | | 2.7 | - | |
| Digital Low Level Output Voltage (B00-B13) | VOL | DVRP = 5.0 V, VEN = DVCC, IOH = +1.0mA | | - | 0.4 | |
| | | DVRP = 5.0 V, VEN = DVCC, IOH = +4.0mA | | | 0.6 | |
| | | DVRP = 3.3 V, VEN = DVCC, IOH = +1.0mA | | | 0.4 | |
| | | DVRP = 3.3 V, VEN = DVCC, IOH = +4.0mA | | | 0.6 | |
| Digital High Level Output Current (B00-B13) | IOH (SOURCE) | DVRP = 5.0 V, VEN ≥ 3.0 V | | - | -4.0 | mA |
| | | DVRP = 3.3 V, VEN ≥ 2.2 V | | - | -4.0 | |
| Digital Low Level Output Current (B00-B13) | IOL (SINK) | DVRP = 5.0 V, VEN ≥ 3.0 V | | - | 4.0 | |
| | | DVRP = 3.3 V, VEN ≥ 2.2 V | | - | 4.0 | |
| High Output Leakage Current (B00-B13) 3/ | $I_{OUTLK_{HI}}$ | VOE = DGND | +25°C | -5 | 5 | nA |
| | | | +125°C | -50 | 50 | |
| Low Output Leakage Current (B00-B13) 3/ | $I_{OUTLK_{LO}}$ | VOE = DGND | +25°C | -5 | 5 | |
| | | | +125°C | -50 | 50 | |

Notes:

1/ Specification derated to reflect Total Dose exposure to 1 Mrad(Si) @ +25°C.

2/ Not tested. Shall be guaranteed by design, characterization, or correlation to other test parameters.

3/ These parameters for Tc = -55°C are guaranteed by design, characterization, or correlation to other test parameters.

| Pin # | Signal | Definition | Pin # | Signal | Definition |
|---|---|---|---|---|---|
| 1 | AVCC | Analog Supply Voltage | 21 | B10 | Digital Output 10 |
| 2 | DVCC | Digital Supply Voltage | 22 | B11 | Digital Output 11 |
| 3 | AD02 | Multiplexer Address 02 | 23 | B12 | Digital Output 12 |
| 4 | AD01 | Multiplexer Address 01 | 24 | B13 | Digital Output 13 |
| 5 | AD00 | Multiplexer Address 00 | 25 | EOC_H | End of Convert |
| 6 | CASE | Case Ground | 26 | BUSY_L | Busy |
| 7 | STCNV_H | Start Conversion | 27 | DRVN | Digital Output Low Reference Level |
| 8 | EN_H | Multiplexer Enable | 28 | DRVP | Digital Output High Reference Level |
| 9 | OE_H | Output Enable | 29 | DGND | Digital Supply Return |
| 10 | CLK | Clock Input | 30 | AGND | Analog Supply Return |
| 11 | B00 | Digital Output 00 | 31 | PREF | High Analog Reference Voltage |
| 12 | B01 | Digital Output 01 | 32 | AIN07 | Analog Multiplexer Input 07 |
| 13 | B02 | Digital Output 02 | 33 | AIN06 | Analog Multiplexer Input 06 |
| 14 | B03 | Digital Output 03 | 34 | AIN05 | Analog Multiplexer Input 05 |
| 15 | B04 | Digital Output 04 | 35 | AIN04 | Analog Multiplexer Input 04 |
| 16 | B05 | Digital Output 05 | 36 | AIN03 | Analog Multiplexer Input 03 |
| 17 | B06 | Digital Output 06 | 37 | AIN02 | Analog Multiplexer Input 02 |
| 18 | B07 | Digital Output 07 | 38 | AIN01 | Analog Multiplexer Input 01 |
| 19 | B08 | Digital Output 08 | 39 | AIN00 | Analog Multiplexer Input 00 |
| 20 | B09 | Digital Output 09 | 40 | NREF | Low Analog Reference Voltage |

**FIGURE 2: PACKAGE PIN-OUT AND SIGNAL DEFINITION**

## TRUTH TABLE (AIN00 – AIN07)

| AD02 | AD01 | AD00 | EN_H | "ON" CHANNEL |
|---|---|---|---|---|
| X | X | X | L | NONE |
| L | L | L | H | AIN00 |
| L | L | H | H | AIN01 |
| L | H | L | H | AIN02 |
| L | H | H | H | AIN03 |
| H | L | L | H | AIN04 |
| H | L | H | H | AIN05 |
| H | H | L | H | AIN06 |
| H | H | H | H | AIN07 |

**FIGURE 3: TRUTH TABLE**

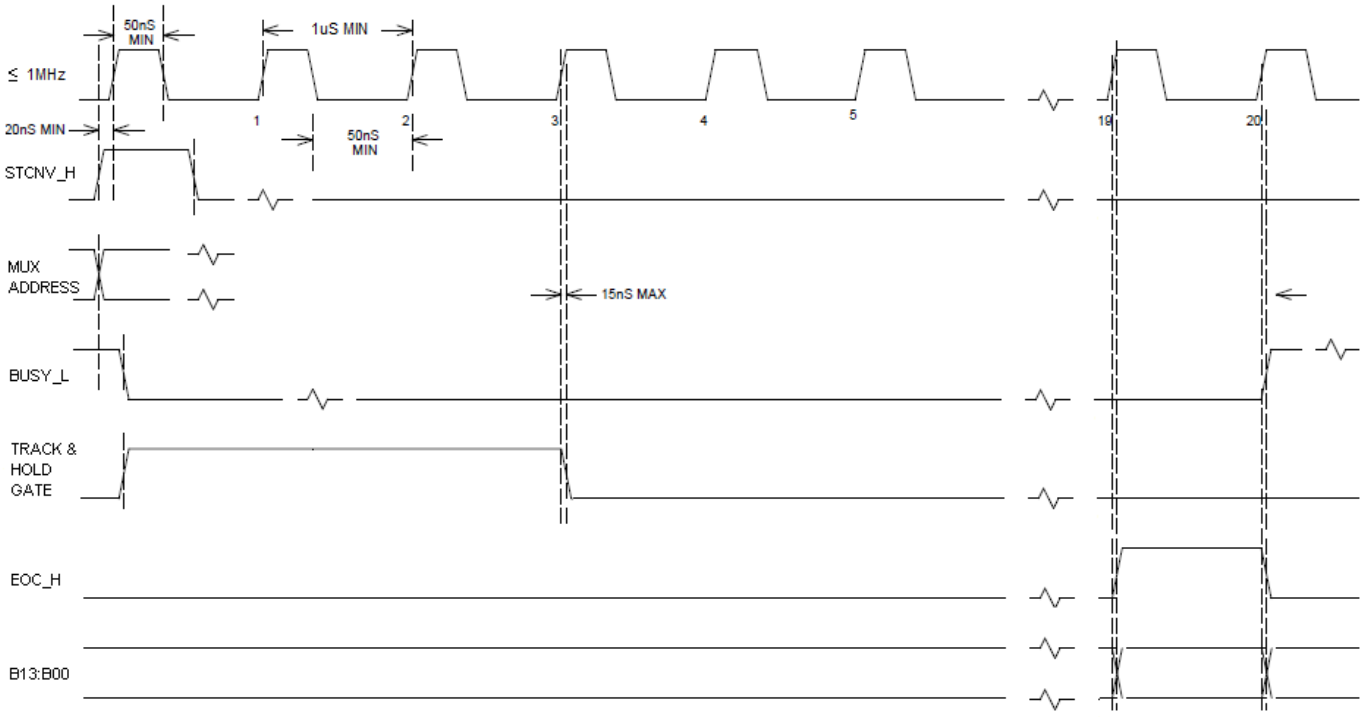
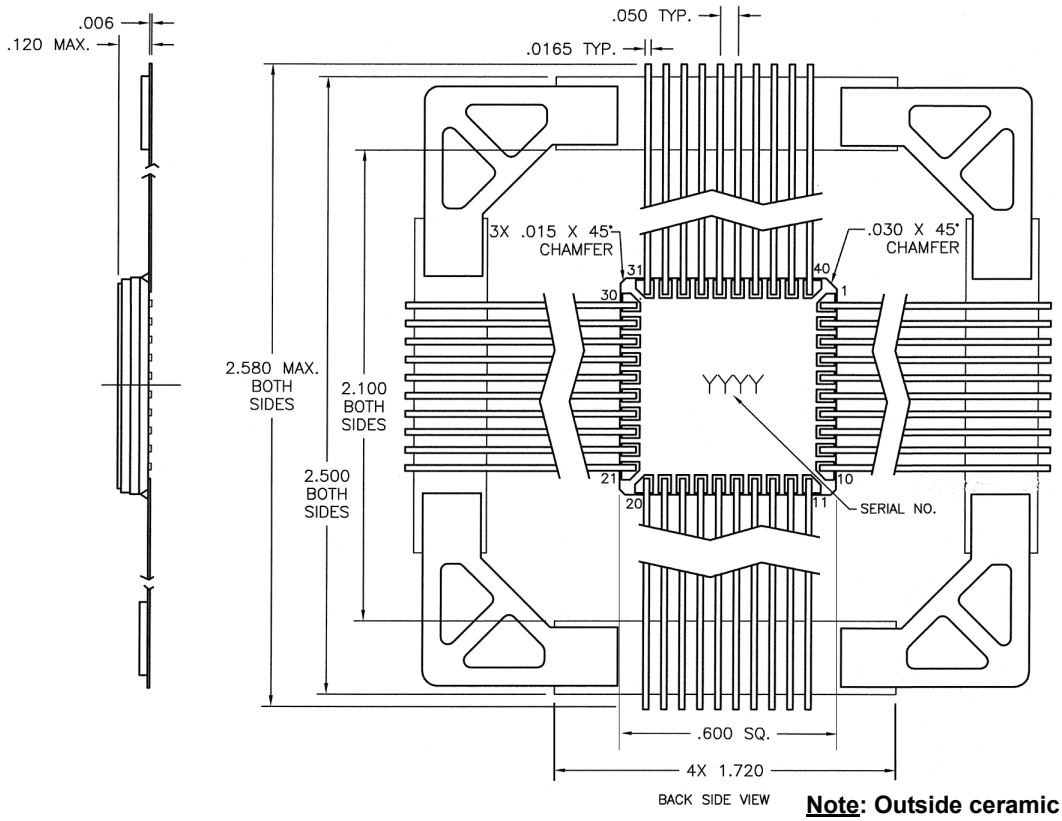



**FIGURE 4: BASIC TIMING DIAGRAM**




**Note: Outside ceramic tie bars not shown for clarity. Contact factory for details.**

**FIGURE 5: PACKAGE OUTLINE**

## ORDERING INFORMATION

| Model | DLA SMD # | Screening | Package |
|---|---|---|---|
| RHD5958-7 | - | Commercial Flow, +25°C testing only | 40-lead CQFP |
| RHD5958-S | - | Military Temperature, -55°C to +125°C<br>Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications | |
| RHD5958-201-1S | 5962-1221101KXC | In accordance with DLA SMD | |
| RHD5958-901-1S | 5962H1221101KXC | DLA SMD and Radiation Certification Pending | |

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