RHFL6000L

Datasheet

2 A Rad-hard adjustable positive linear voltage regulator

FLAT-16 P

The upper metallic lid is connected to ground

Maturity status link
RHFL6000L

Features

- Input voltage range from 2.5 V to 12 V
- Adjustable output voltage from 0.6 V to 9 V
- 2 A guaranteed output current
- Low dropout voltage: 0.3 V typ. @ 0.4 A
- Embedded overtemperature and overcurrent protection
- Adjustable overcurrent limitation
- Output overload monitoring/signalling
- Internal control loop accessible via an external pin, optional, providing flexibility for stability margin tuning
- Inhibit (ON/OFF) TTL compatible control
- Programmable output short-circuit current
- Remote sensing operation
- Rad-hard: guaranteed up to 300 krad MIL-STD-883J method 1019.9 high dose rate and 0.01 rad/s in ELDRS conditions
- Radiation environment: SET/SEL/SEB:
  - SEL free @ LET=120 MeV/cm²/mg
  - SET: less than 3.3% of V_{OUT}@ 120 MeV
- Heavy-ions SET dedicated internal circuitry implemented for absorbing output transient
- Operating junction temperature range: -55 °C to 125 °C

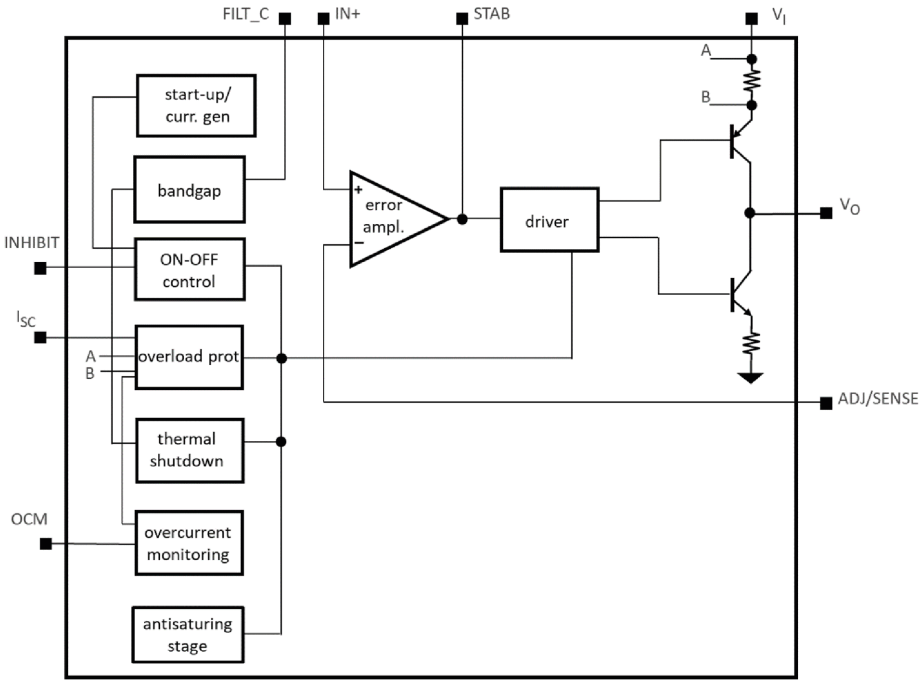
Description

The RHFL6000L high-performance adjustable positive voltage regulator provides exceptional radiation performance. It is tested in accordance with MIL-STD-883J method 1019.9, in ELDRS conditions. The device is available in the Flat-16P, a hermetic ceramic package. A dedicated internal circuitry is implemented to absorb output transients during SET events. The operating input voltage goes from 2.5 V to 12 V.

The RHFL6000L is an upgraded version of the RHFL6000A and is intended to extend the range of the regulated output voltages down to 0.6 V.

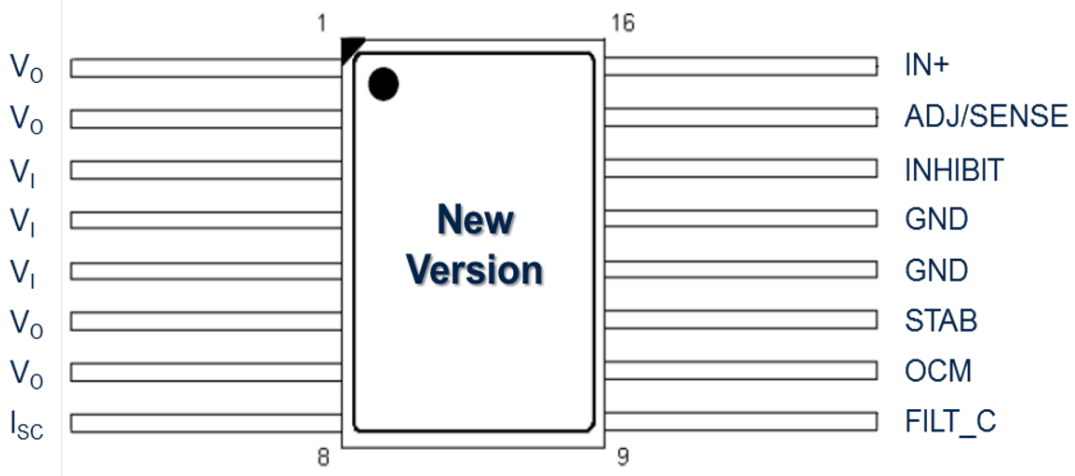
1 Diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. Pin configuration (top view)



Note: The upper metallic package lid is connected to ground. The bottom metallization is electrically floating.

Table 1. Pin description

Pin name	Flat-16P	Pin description
V_O (1)	1, 2, 6, 7	Output port of the regulator
V_I (2)	3, 4, 5	Input port of the regulator
GND	12, 13	Ground
I_{SC}	8	Current limit setting pin. Connect a resistor (Rsc) between this pin and V_I to set the current limit threshold.
OCM	10	Overcurrent monitor flag. Open collector, internally pulled up. The signal on this pin goes to low logic level when the current limit activates.
INHIBIT	14	Device inhibit pin. Internally pulled down. The regulator is off when this pin is set at high logic level.
ADJ/SENSE	15	Feedback pin
FILT C	9	Filter capacitor pin. An optional capacitor (Cfilt) can be connected between this pin and GND for SET mitigation and noise purposes.
STAB	11	An optional R-C network can be connected between this pin and GND to tune the internal control loop.
IN+	16	Non-Inverting input of the error amplifier

1. *All the output pins must be connected together on the PCB.*
2. *All input pins must be connected together on the PCB.*

Table 2. Recommended minimum and maximum operative conditions

Symbol	Parameter	Value	Unit
V_I	DC input voltage, V_I-V_{GROUND}	2.5 to 12	V
V_O	DC output voltage range	0.6 to 9	V
I_O	Continuous output current	0 to 2	A
T_A	Ambient operating temperature range	- 55 to +125	°C

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage, V_I-V_{GROUND}	- 0.3 to 14	V
V_O (1)	DC output voltage range	- 0.3 to (V_I + 0.3)	V
V_{ADJ} (2)	Adjustable pin voltage	- 0.3 to (V_O + 3.45)	V
I_O	Continuous output current	2	A
V_{OCM} (1)	Overcurrent monitor pin voltage vs. GND	- 0.3 to (Vi + 0.3)	V
V_{ISC} (1)	Current limit pin voltage vs. GND	- 0.3 to (Vi + 0.3)	V
INHIBIT (1)	Inhibit pin voltage	- 0.3 to (Vi + 0.3)	V
STAB	Stability capacitor pin voltage	- 0.3 to 1.5	V
FILT C	Filter capacitor pin voltage	- 0.3 to 1.3	V
IN+	Not inverting terminal of the error amplifier	- 0.3 to 1.3	V
T_{STG}	Storage temperature range	- 65 to +150	°C
T_{OP}	Operating junction temperature range	- 55 to +125	°C
ESD	Human body model (HBM)	2	kV
	Machine model (MM)	200	V
	Charged device model (CDM)	500	V

1. *Maximum voltage guaranteed to have zero current across the terminal.*
2. *To avoid risks of performance degradation.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case, Flat-16P	8.3	°C/W
T_{SOLD}	Maximum soldering temperature, 10 s	300	°C

4 Electrical characteristics

T_J = 25 °C, V_I - V_O = 2.5 V, C_I = C_O = 10 µF (tantalum), unless otherwise specified.

Table 5. Electrical characteristics

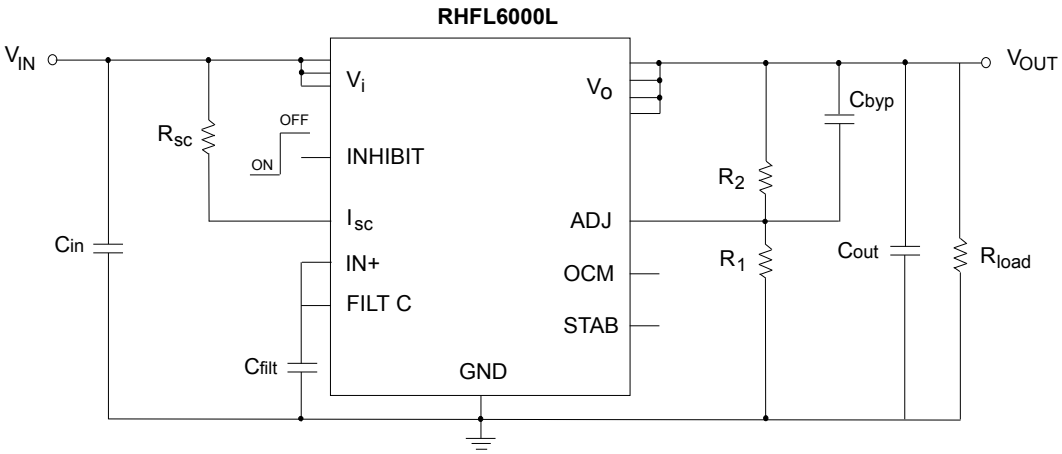
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage	I_O = 1 A, T_J = -55 to 125 °C	2.5		12	V
V_{ADJ}	Reference voltage	I_O = 5 mA to 1 A, V_O = V_{adj}, T_J = -55 to 125 °C, V_{OUT} ≥ 1.25 V	1.205	1.245	1.285	
V_{FILT_C}	Reference voltage	I_O = 5 mA to 1 A, V_O = V_{ADJ}, T_J = -55 to 125 °C, I_{REF} = 10 µA	1.205	1.245	1.285	
I_{SHORT} (1)	Output current limit	Adjustable by external resistor	1	3		A
$\Delta V_O/\Delta V_I$	Line regulation	V_I = 2.5 V to 12 V, I_O = 5 mA, T_J = -55 °C to +125 °C		0.2	0.6	%
$\Delta V_{FILT\_C}/\Delta V_I$	Line regulation on FILT_C	V_I = 2.5 V to 12 V, I_O = 5 mA, T_J = -55 °C to +125 °C, V_O = 0.6 V		0.2	0.6	
ΔV_O / ΔI_O	Load regulation	V_I = 2.5 V, I_O = 5 mA to 400 mA, T_J = -55 °C to +125 °C, 0.6 V < Vo < 1.25 V		0.01	0.5	
		V_I = 2.5 V, I_O = 5mA to 1 A, T_J = -55 °C to +125 °C, 0.6 V < Vo < 1.25 V		0.3	0.6	
		V_I = 2.5 V, I_O = 5 mA to 2 A, T_J = -40 to 125 °C, 0.6 V < Vo < 1.25 V		0.6		
		V_I = 3.0 V, I_O = 5 mA to 2 A, T_J = -55 to -40 °C, 0.6 V < Vo < 1.25 V				
Z_{OUT} (1)	Output impedance	I_O = 100 mA DC and 20 mA rms		100		mΩ
I_q	Quiescent current ON mode	V_I = 2.5 V to 12 V, I_O = 5 mA, T_J = +25 °C			15	mA
		V_I = 2.5 V to 12 V, I_O = 30 mA, T_J = +25 °C			15	
		V_I = 2.5 V to 12 V, I_O = 300 mA, T_J = +25 °C			30	
		V_I = 2.5 V to 12 V, I_O = 1 A, T_J = +25 °C			60	
		V_I = 2.5 V to 12 V, I_O = 30 mA, T_J = -55 °C			15	
		V_I = 2.5 V to 12 V, I_O = 300 mA, T_J = -55 °C			35	
		V_I = 2.5 V to 12 V, I_O = 1 A, T_J = -55 °C			80	
		V_I = 2.5 V to 12 V, I_O = 30 mA, T_J = +125 °C			15	
		V_I = 2.5 V to 12 V, I_O = 300 mA, T_J = +125 °C			30	
		V_I = 2.5 V to 12 V, I_O = 1 A, T_J = +125 °C			50	
I_{qOFF}	Quiescent current OFF mode	V_I = 2.5 V, V_{INH} = 2.4 V, OFF mode, T_J = -55 to +125 °C		0.2	1	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_d	Dropout voltage	I_O = 400 mA, V_O = 2.5 to 9 V, (+25 °C)		300	450	mV
		I_O = 400 mA, V_O = 2.5 to 9 V, (-55 °C)		250	400	
		I_O = 400 mA, V_O = 2.5 to 9 V, (+125 °C)		350	550	
		I_O = 1 A, V_O = 2.5 to 9 V, (+25 °C)		570	800	
		I_O = 1 A, V_O = 2.5 to 9 V, (-55 °C)		470	700	
		I_O = 1 A, V_O = 2.5 to 9 V, (+125 °C)		700	900	
		I_O = 2 A, V_O = 2.5 to 9 V, (+25 °C)		550		
		I_O = 2 A, V_O = 2.5 to 9 V, (-55 °C)		500		
		I_O = 2 A, V_O = 2.5 to 9 V, (125 °C)		700		
$V_{INH(ON)}$	Inhibit voltage	I_O = 5 mA, T_J = -55 to +125 °C			0.8	V
$V_{INH(OFF)}$	Inhibit voltage	I_O = 5 mA, T_J = -55 to +125 °C	2.4			
SVR (1)	Supply voltage rejection	V_I = V_O +2.5 V ± 0.5 V, V_O = 3 V I_O = 5 mA, f = 120 Hz TA = 25 °C	60	70		dB
		V_I = V_O +2.5 V ± 0.5 V, V_O = 3 V I_O = 5 mA, f = 33 kHz TA = 25 °C	30	40		
I_{SH}	Shutdown input current	V_{INH} = 5 V		220		µA
V_{OCM}	OCM pin voltage	Sinked I_{OCM} = 24 mA active low		0.4		V
t_{PLH} (1)	Inhibit propagation delay, turn-off	V_I = V_O +2.5 V, V_{INH} = from 0 V to 2.4 V, I_O = 400 mA, V_O = 3 V			30	µs
t_{PHL} (1)	Inhibit propagation delay, turn-on	V_I = V_O +2.5 V, V_{INH} = from 2.4 V to 0 V, I_O = 400 mA, V_O = 3 V			100	µs
eN (1)	Output noise voltage	B = 10 Hz to 100 kHz, V_{out} = 5 V I_O = 5 mA to 2 A, Cfilt = 22 µF		40		µVrms
		B = 10 Hz to 100 kHz; 1.0 ≤ V_O ≤ 1.25 V, Cfilt = 22 µF I_O = 5 mA to 2 A Iref = 10 µA		10		

1. *These values are guaranteed by design.*

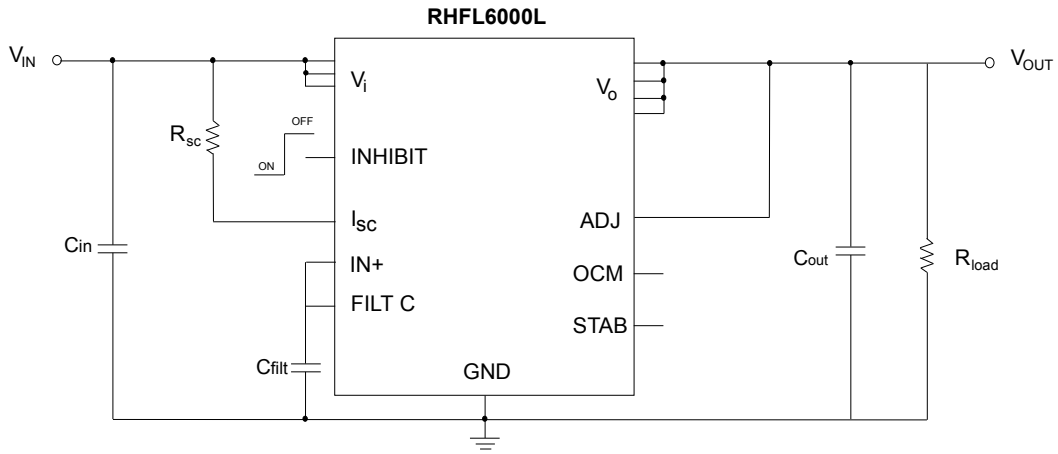
5 Typical application diagram

Figure 3. Typical application diagram for V_{out} > 1.25 V



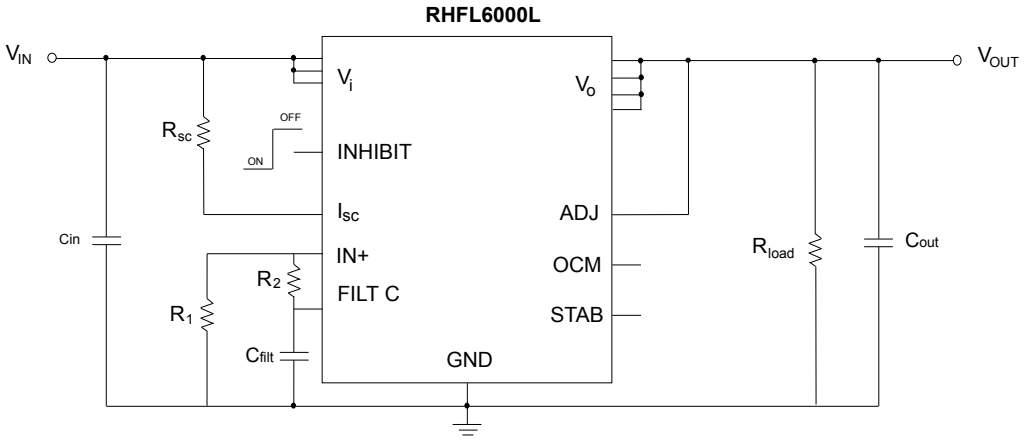
For V_O > 1.25 V, the divider resistor pair R_2 and R_1 are tied between V_O, ADJ/SENSE (middle point), and GND pins respectively; FILT_C and IN+ pins are externally shorted (see Figure 3. Typical application diagram for V_{out} > 1.25 V). In this case, the arrangement of the feedback control loop is identical to the one used for generating V_O > 1.25 V in the RHFL6000A device.

Figure 4. Typical application diagram for V_{out} = 1.25 V



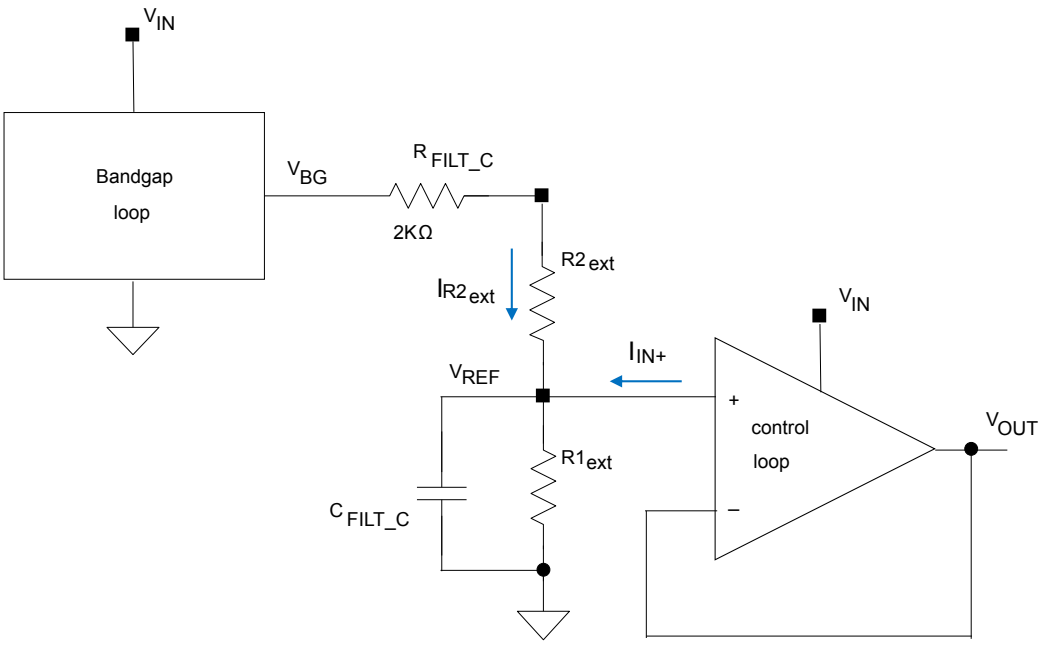
For V_O = 1.25 V, FILT_C must be shorted to IN+ and V_O to ADJ/SENSE terminals (see Figure 4. Typical application diagram for V_{out} = 1.25 V). Also in this case, the arrangement of the feedback control loop is identical to the one used for generating V_O = 1.25 V in the RHFL6000A device.

Figure 5. Typical application diagram for V_{out} < 1.25 V



When V_O < 1.25 V is required in the application, the divider resistor pair R2 and R1 are connected between FILT_C, IN+ (middle point), and GND pins respectively, as shown in Figure 5. Typical application diagram for V_{out} < 1.25 V and Figure 6. Detailed regulation loop diagram. V_O is externally shorted to the ADJ/SENSE pin (as in the typical control loop arranged in unity-gain feedback). Therefore, in this case, the output value (V_O < 1.25 V) is generated upstream to the error amplifier by fractioning the V_{BG} value (available on FILT_C pin) according to the ratio of the resistor divider composed by R1 and R2.

Figure 6. Detailed regulation loop diagram



With reference to Figure 6. Detailed regulation loop diagram, the ideal scenario for the voltage at IN+, let us call it V_{REF}, is to get as close as possible to:

$$V_{REF} \cong \frac{R1_{ext}}{R_{FILT\_C} + R2_{ext} + R1_{ext}} \times VBG$$

over the whole operating temperature range.

In this respect, it is necessary that $I_{IN}+ << I_{R2ext}$, where I_{IN+} is the current flowing through IN+ terminal and I_{R2ext} is the current across R2.

A too low I_{R2ext} value makes V_{REF} (and the output voltage V_{OUT}) sensitive to the β degradation of the bipolars at the input stage. This could lead to noticeable drifts under process and TID.

Conversely, a too high IR2ext value increases the minimum V_{IN} threshold needed for the regulation (since this current is provided by the bandgap buffer) and the V_{OUT} temperature drift.

Having an R1 high value (> 10 kΩ) is beneficial for the SEE immunity of the device as it enhances, in combination with CFILT_C, the mitigating effect of the low-pass filter versus the SEE arising on VBG and joining the node IN+.

Regarding IR2ext, the suggested value of this current in application ranges in the interval [10 µA ÷ 20 µA].

6 Radiations

6.1 Total ionizing dose (MIL-STD-883 test method 1019)

The products that are guaranteed in radiation within RHA QML-V system, fully comply with the MIL- STD-883test method 1019 specification. The RHFL6000L is being RHA QML-V qualified. It is covered by similarity with RHFL6000A tested and characterized in full compliance with the MIL-STD-883 specification, both below 10 mrad/s (low dose rate) and between 50 and 300 rad/s (high dose rate).

- Testing is performed in accordance with MIL-prf-38535 and the test method 1019 of the MIL- STD-883 for total ionizing dose (TID).
- ELDRS characterization is performed on RHFL6000A in qualification only on both biased and unbiased parts, on a sample of ten units from two different wafer lots.The RHFL6000L is covered by similarity.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Table 6. TID tests results

Type	Conditions	Value	Unit
TID	50 rad(Si)/s high dose rate up to	300	krad
	10 mrad(Si)/s low dose rate up to	300	
	ELDRS free up to	300	
Output voltage radiation drift	From 0 krad to 300 krad at 50 rad/s, MIL-STD-883J method 1019.9	< 1.1	ppm/krad
Quiescent current (ON-state)	From 0 krad to 300 krad at 50 rad/s, MIL-STD-883J method 1019.9 V_I = 2.5 V to 12 V, I_O = 5 to 30 mA, T_J = - 55 to +125 °C	< 30	mA

6.2 Heavy-ions

The heavy-ion trials are performed on qualification lots only. No additional test is performed.

Focus was on the configuration for V_O = 0.6 V but the results can be extrapolated to any V_O < 1.25 V for the expected accuracy, provided that the scheme shown in Figure 7. Heavy-ion test configuration for V_{OUT} < 1.25 V and the BOM list in Table 9 be adopted.

For V_O ≥ 1.25 V, the conclusions obtained on the former RHFL6000A device apply if compliant with the guidelines indicated in the AN5175 document.

Table 7. Heavy-ion results summarizes the results of heavy-ion tests.

Table 7. Heavy-ion results

Feature	Conditions	Value	Unit
SEL/B performance	LET = 120 MeV*cm2/mg V_I = 12 V	No latch-up/burn-out	-
SET performance during events	LET = 120 MeV*cm2/mg; V_I – V_O = 2.5 V (1); I_{OUT} ≤ 1 A:	No SET above ± 3.3 %	% of V_O

1. *For V_O < 1.25 V, the SET accuracy within X % is guaranteed only for V_I - V_O ≤ 2.5 V. For this, V_I = 1.25 + 2.5 V = 3.75 V is expected to be the max. limit of interest in the V_O output range of concern.*

SEL and SET performances described here below are related to the circuit configuration and bias conditions shown in Figure 7. Heavy-ion test configuration for V_{OUT} < 1.25 V and Table 8. Bias configurations and Table 9. Test configurations.

Figure 7. Heavy-ion test configuration for V_{OUT} < 1.25 V

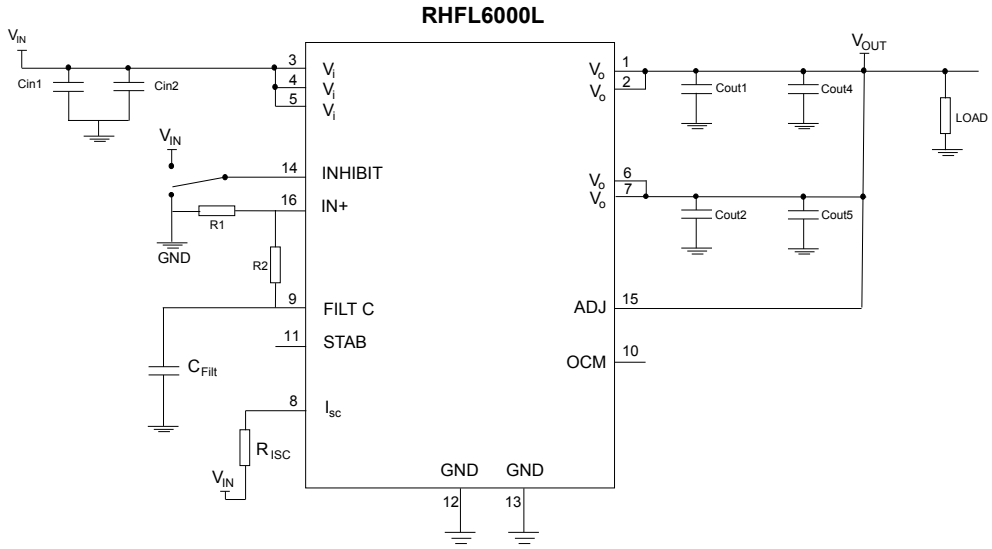


Table 8. Bias configurations

Test mode	Bias conditions
SEL	V_{IN} = 12 V, V_{OUT} = 0.6 V, $V_{INHIBIT}$ = 0 V, I_{OUT} = 5 mA
SET	V_{IN} = 3.1 V, V_{OUT} = 0.6 V, $V_{INHIBIT}$ = 0 V, I_{OUT} = 100 mA
	V_{IN} = 3.1 V, V_{OUT} = 0.6 V, $V_{INHIBIT}$ = 0 V, I_{OUT} = 1 A
	V_{IN} = 3.75 V, V_{OUT} = 0 V, VI_{NHIBIT} = 3.75 V

Table 9. Test configurations

Test mode	Test configurations	
SEL	Sel configuration	C_{IN1} = 150 µF
		C_{OUT4} = C_{OUT5} = 150 µF
		C_{IN2} = C_{OUT1} = C_{OUT2} = 100 µF
		R_1 = 62 KΩ
		R_2 = 68 KΩ
		C_{filt} = 22 µF
		R_{ISC} = 8.2 kΩ
		R_{load} = 1.8 kΩ
SET	SET configuration	C_{IN1} = 150 µF
		C_{OUT4} = C_{OUT5} = 150 µF
		C_{IN2} = C_{OUT1} = C_{OUT2} = 100 µF
		C_{filt} = 22 µF
		R_{ISC} = 8.2 kΩ
		R_{load} = depending on bias conditions
		R_1 = 62 KΩ

Test mode	Test configurations	
SET	SET configuration	R_2 = 68 KΩ

Table 10. BOM LIST

Component	Part number	Manufacturer
C_{IN1}, $C_{OUT4,5}$	T530D157M010ATE006	KEMET
C_{IN2}, $C_{OUT1,2}$	CDR04BX104AKWS	AVX

7 Additional guidelines for SET mitigation

This section provides detailed design guidelines necessary to obtain the required performance against SET. In this respect, we can identify two main areas for intervention: ground connection and external components selection.

7.1 Ground connections

To achieve the best performance in terms of output voltage accuracy, noise immunity and robustness against single event effects, it is recommended to implement a proper PCB layout by following the suggestions described below.

According to qualitative simulations of single events, some very short SET (that is, a duration in the 100 ns range) are strongly dependent on the stray inductances versus GND. The best solution to reduce the parasitic inductance is the adoption of a GND plane (with separate power and sense paths where possible). By minimizing the stray GND impedance, this approach is of great assistance in controlling the amplitude of the SET events near the load.

If this solution is not applicable, we suggest using a star-bus topology, where the PCB reference GND connection is close to the GND pin of the regulator.

To achieve a good GND sense, it is necessary to comply with the following rules:

- connect the chip GND and the load one to a common point (used as star GND);
- connect the power GND on the PCB to the star GND through an array of multiple vias;
- for GND connectors/plugs: use separate plugs for power supply and testing probes;
- connect I/O capacitors GND to the GND star by dedicated trace.

7.2 Capacitor selection

With reference to Figure 7. Heavy-ion test configuration for V_{OUT} < 1.25 V, a combination of capacitors must be present close to the I/O ports.

For the INPUT terminals, this may consist of a 150 µF bulk capacitor (C_{IN1}), esr ~ 6 mΩ in parallel with a 100 nF polyester one (C_{IN2}). The latter is used for decoupling purposes.

For each of the two OUTPUT connections (pins 1, 2 and 6, 7) we suggest using a combination of a 150 µF bulk capacitor with esr ~ 6 mΩ (C_{OUT4}, C_{OUT5}) in parallel with a polyester 100 nF one (C_{OUT1}, C_{OUT2}); the latter for decoupling purposes.

These capacitors must be placed as close to the I/O terminals as possible with the bypass ones (C_{In1}, $C_{OUT1,2}$) closer to the device to tackle stray PCB inductances related to the VIN/GND busses near to the device.

Regarding parts selection, we suggest the adoption of low-ESL, low ESR capacitors having characteristics similar to those listed in Table 9. Still, for the bulk capacitors, using an array of paralleled capacitors works better than a single component in limiting the intrinsic ESL (and thus against the short SETs).

8 Device description

The RHFL6000L adjustable voltage regulator contains a PNP type power element controlled by a signal resulting from an amplified comparison between the temperature-compensated internal bandgap and the fraction of the desired output voltage value obtained from an external resistor divider bridge, for $V_O \geq 1.25$ V.

For $V_O < 1.25$ V, the external resistor divider is moved upstream to the error amplifier and therefore the comparison occurs between a fraction of the temperature-compensated internal bandgap (according to the desired output voltage value) and the output voltage itself. The device is protected by several functional blocks.

8.1 ADJ pin

The feedback voltage necessary for the loop regulation comes from the load through an external resistor divider (R1, R2 as in Figure 5. Typical application diagram for $V_{out} < 1.25$ V) whose midpoint is connected to the ADJ/SENSE pin, allowing all possible output voltage settings for $V_{OUT} > 1.25$ V as per user requirements.

8.2 Inhibit ON-OFF control

By setting the INHIBIT pin to TTL high level, the device switches off. The device is in ON-state when the INHIBIT pin is set low. Since the INHIBIT pin is pulled down internally, it can be left floating whenever the inhibit function is not used. Alternatively, it can also be shorted to the GND.

8.3 Overtemperature protection

A temperature detector internally monitors the power element junction temperature. The device turns off when a temperature of approximately 175 °C is reached, returning to ON mode when the temperature decreases down to approximately 135 °C.

It should be noted that when the internal temperature detector reaches 175 °C, the active power element can be as high as 225 °C. Prolonged operation under these conditions may exceed the maximum operating ratings and device reliability cannot be guaranteed.

8.4 Overcurrent protection

A default internal constant current limit is set at I_{SHORT} = 3 A (when V_O is at 0 V).

This value can be decreased via an external resistor (R_{SHORT}) connected between the I_{SC} and V_I pins, with a typical value range of 10 kΩ to 200 kΩ.

To maintain optimal regulation, it is necessary to set I_{SHORT} 1.6 times greater than the desired maximum operating current (I_O). When I_O reaches I_{SHORT}–300 mA, the current limiter intervenes, V_O starts to drop and the OCM flag is raised. When no current limitation adjustment is required, the I_{SC} pin must be left unbiased.

The combination of overcurrent and overtemperature circuits provides the RHFL6000L with a high level of protection against destructive junction temperature excursions in all load conditions.

8.5 OCM pin

The OCM pin is an open collector flag normally pulled up at V_I by a 5 kΩ resistor.

It goes to low state when the current limit becomes active. It is buffered and can sink 10 mA.

8.6 STAB pin

The STAB pin gives the user direct access to regulator internal control loop stability adjustment. Its usage is optional and it should be left unconnected when not used.

8.7 FILT C pin

The FILT_C pin helps limiting SET amplitudes and output noise when bypassed vs. GND through a 22 µF polyester capacitor, Cfilt. Its usage is therefore mandatory in both SET and low-noise applications. Out of the mentioned cases, Cfilt is not needed.

8.8 IN+

By shorting this pin to the FILT_C pin, it is possible to set the values of output voltage $V_{OUT} \geq 1.25$ V (see Figure 3. Typical application diagram for $V_{out} > 1.25$ V and Figure 4. Typical application diagram for $V_{out} = 1.25$ V). For $V_{OUT} < 1.25$ V output voltage settings, the external resistor divider is moved upstream to the error amplifier and is connected between FILT_C, IN+ (as middle point), and GND pins, as shown in Figure 5. Typical application diagram for $V_{out} < 1.25$ V. Regarding the selection of the current value flowing across the mentioned resistor divider, $I_{REF} = 10$ µA is the value suggested as a good tradeoff between temperature V_{OUT} drift and absolute $V_{OUT} = (1 + R_2 / R_1) * V_{REF}$ limit.

Higher I_{REF} increases V_{OUT} temperature drift; conversely, the same V_O becomes immune to the current into the IN+ terminal. Lower I_{REF} gets V_{OUT} close to V_{REF} and limits the temperature drift but makes this parameter sensitive to the current into the IN+ terminals and could lead to an excessive TID drift of V_{OUT}.

9 Application information

With reference to Figure 3a, to adjust the output voltage values V_O > 1.25 V, the R2 resistor must be connected between the V_O and ADJ/SENSE pins. The R1 resistor must be connected between ADJ/SENSE and ground. FILT_C and IN+ pins must be externally shorted together.

9.1 Reliability considerations

A reverse operation (supply voltage applied on V_o instead of V_i) could expose the device to degradation in its regulation performances (line, load) when V_O - V_I ≥ 2 V.

The STAB pin is for tuning the control loop stability by a proper RC impedance put between this node and GND. Powering this node with a low impedance source, for V_I > 3.75 V the device could undergo regulation performance degradation.

9.2 Notes on the 16-pin hermetic flat package

The RHFL6000L adjustable voltage regulator is available in a high thermal dissipation 16-pin hermetic FLAT package, whose bottom flange is metallized to allow direct soldering or gluing to a heatsink (efficient thermal conductivity). The upper metallic package lid is connected to ground. The bottom metallization is electrically floating.

9.3 FPGA supply

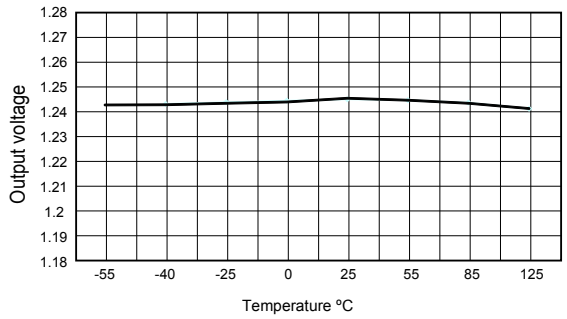
FPGA devices are very sensitive to VDD transients beyond a few % of their nominal supply voltage (usually 1.5 V).

The RHFL6000L includes specific integrated circuitry designed to absorb the output transients under heavy-ion beams, rendering it suitable for safe FPGA supply operation.

10 Typical performance characteristics

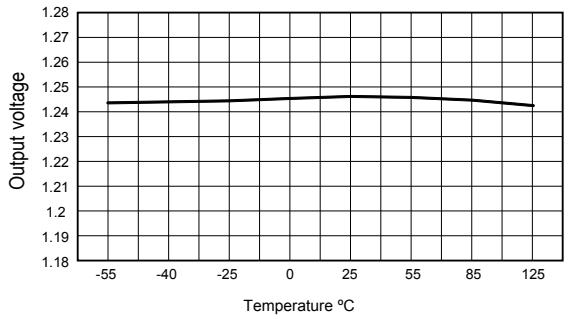
(C_{IN} = C_{OUT} = 10 µF tantalum, unless otherwise specified)

Figure 8. Output voltage vs. temperature (V_{IN} = 2.5 V, I_{OUT} = 5 mA)



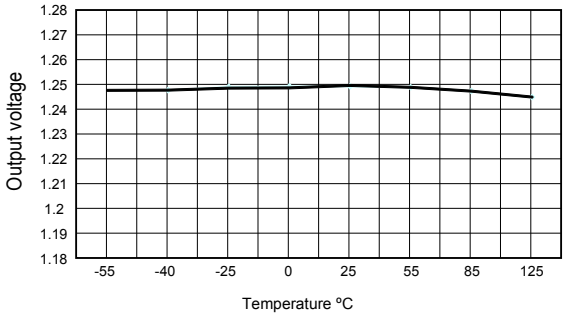
GIPD240620151357MT

Figure 9. Output voltage vs. temperature (V_{IN} = 2.5 V, I_{OUT} = 400 mA)



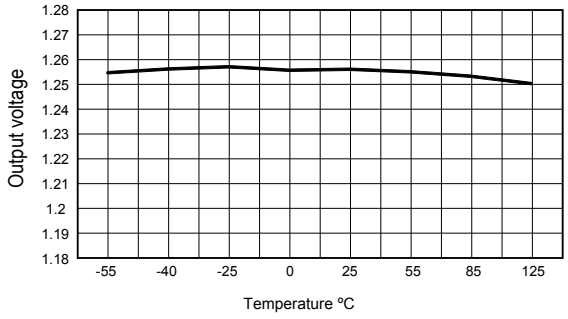
GIPD240620151216MT

Figure 10. Output voltage vs. temperature (V_{IN} = 2.5 V I_{OUT} = 1 A)



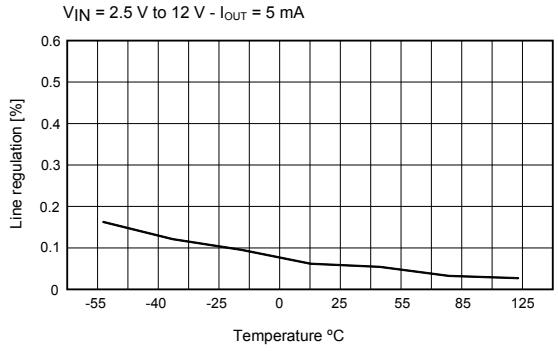
GIPD240620151155MT

Figure 11. Output voltage vs. temperature (V_{IN} = 2.5 V I_{OUT} = 2 A)



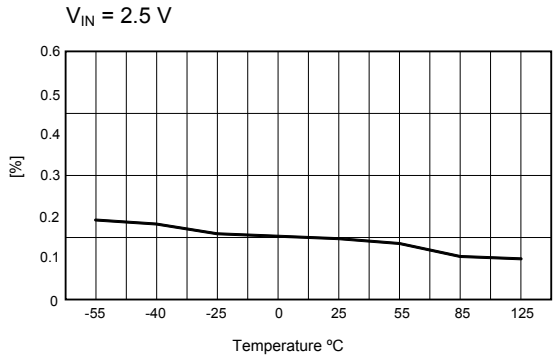
GIPD240620151148MT

Figure 12. Line regulation vs. temperature



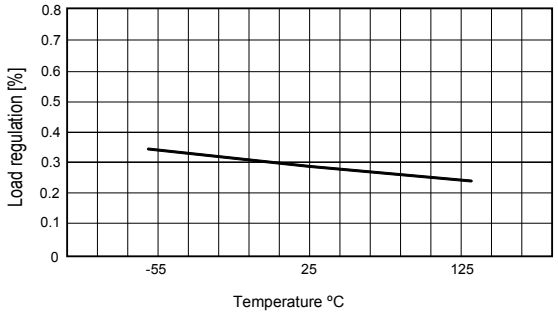
GIPD240620151142MT

Figure 13. Load regulation vs. temperature (I_{OUT} = 5 mA to 400 mA)



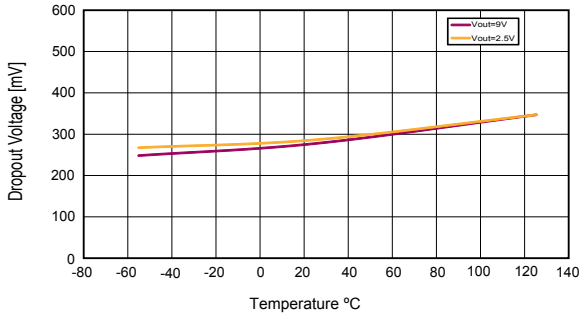
GIPD240620151136MT

Figure 14. Load regulation vs. temperature (I_{OUT} = 5 mA to 1 A, V_{IN} = 2.5 V)



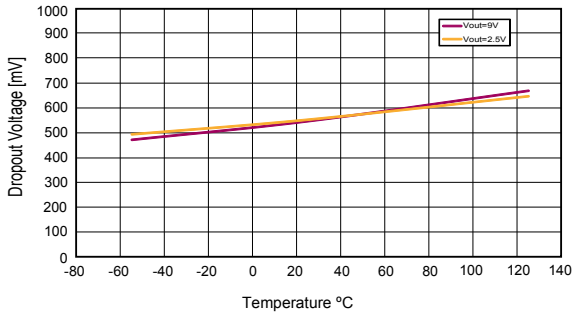
GIPD240620151125MT

Figure 15. Dropout voltage vs. temperature (I_{OUT} = 0.4 A)



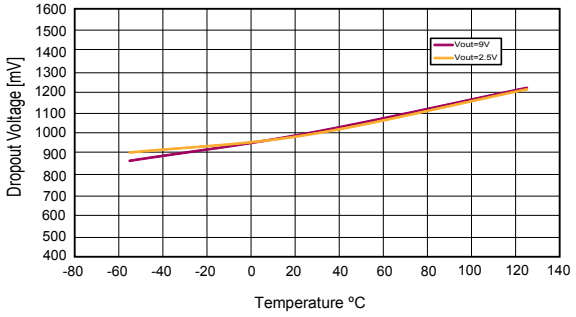
GIPD290620151104MT

Figure 16. Dropout voltage vs. temperature (I_{OUT} = 1 A)



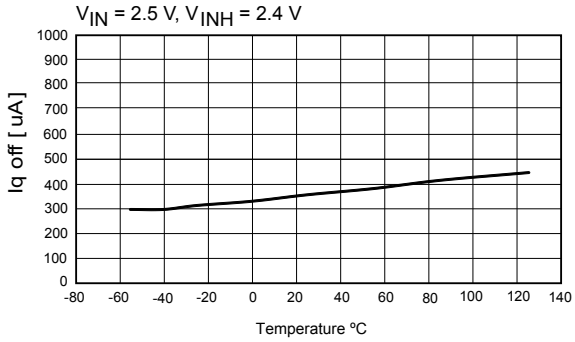
GIPD240620151103MT

Figure 17. Dropout voltage vs. temperature (I_{OUT} = 2 A)



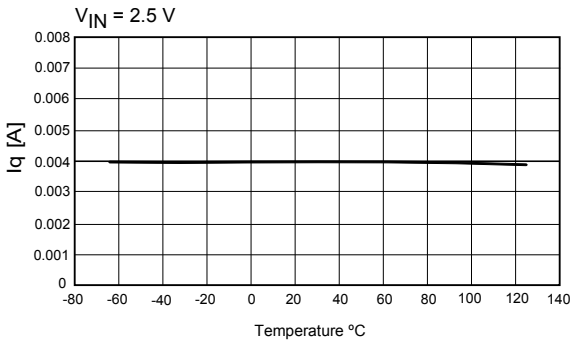
GIPD230620151454MT

Figure 18. Quiescent current (OFF mode)



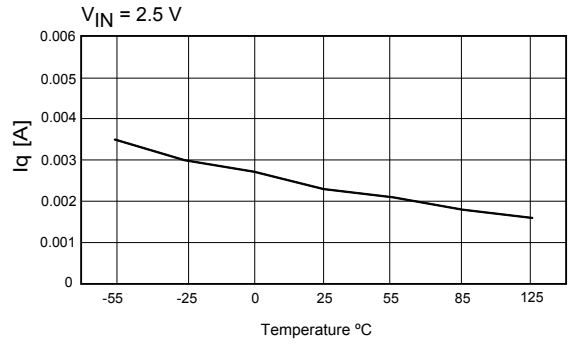
GIPD230620151442MT

Figure 19. Quiescent current (ON mode, I_{OUT} = 5 mA)



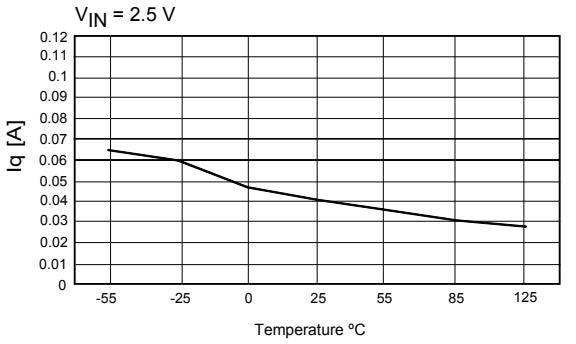
GIPD230620151432MT

Figure 20. Quiescent current (ON mode, I_{OUT} = 1 A)



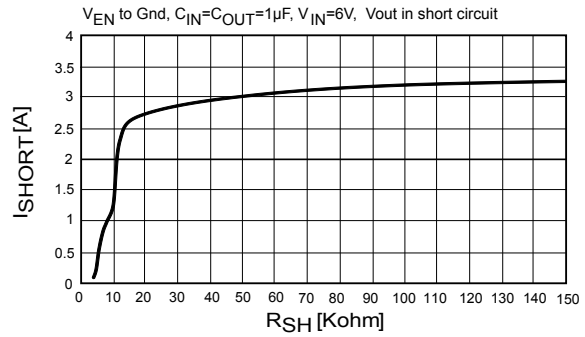
GIPD230620151152MT

Figure 21. Quiescent current (ON mode, I_{OUT} = 2 A)



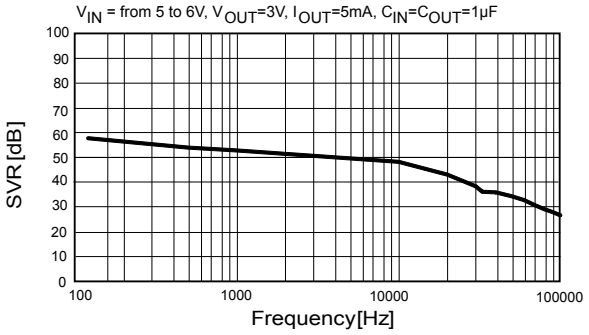
GIPD260620151051MT

Figure 22. Short-circuit current vs. R_{SHORT}



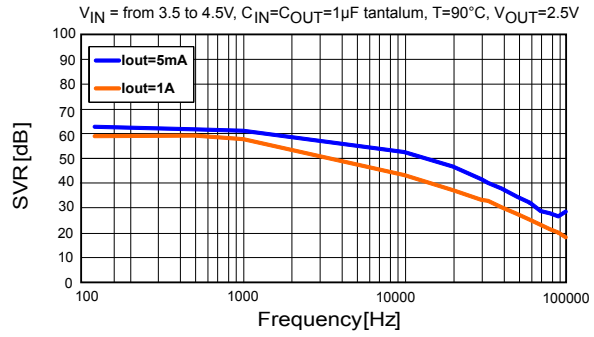
GIPD230620151141MT

Figure 23. SVR vs. frequency



GIPD230620151129MT

Figure 24. SVR vs. frequency (T = 90 °C)



GIPD230620151047MT

Figure 25. Turn-on transient

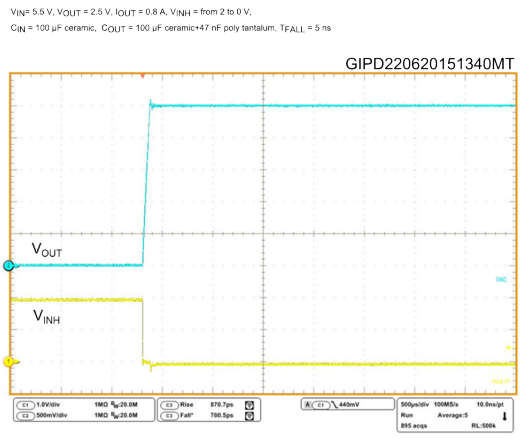


Figure 26. Turn-off transient

V_{IN} = 5.5 V, V_{OUT} = 2.5 V, I= 0.8 A, V_{INH} = from 0 to 2 V,
C_{IN} = 100 µF ceramic, C_{OUT} = 100 µF ceramic+47 nF poly tantalum, T_{RISE} = 5 ns

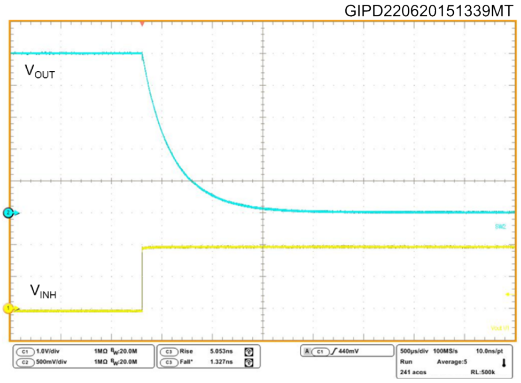


Figure 27. Line transient (I_{OUT} = 0.8 A, V_{OUT} = 3 V)

V_{INH} to Gnd, V_{IN}= from 5 V to 12 V and vice versa No C_{IN}, C_{OUT} = 10 µF tantalum

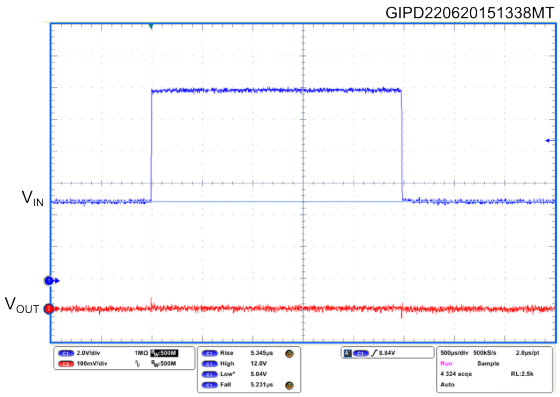


Figure 28. Line transient (I_{OUT} = 2 A, V_{OUT} = 2.5 V)

V_{INH} to Gnd, V_{IN}= from 5 V to 2 V and vice versa I_{OUT} = 2 A, No C_{IN}, C_{OUT} = 10 µF tantalum V_{OUT}= 2.5 V

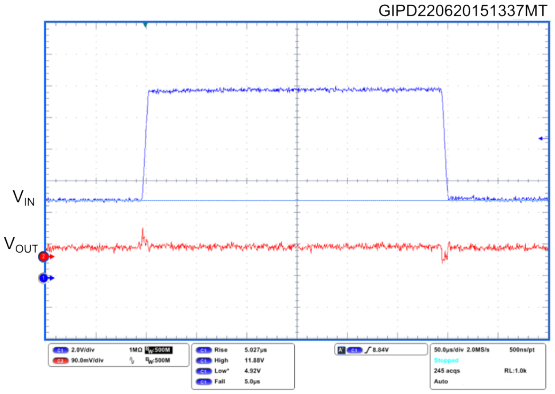


Figure 29. Load transient

V_{IN}= 5 V, I_{OUT}= from 5 mA to 2 A and vice versa, C_{IN} = C_{OUT} = 10 µF tantalum V_{OUT}= 1.24 V

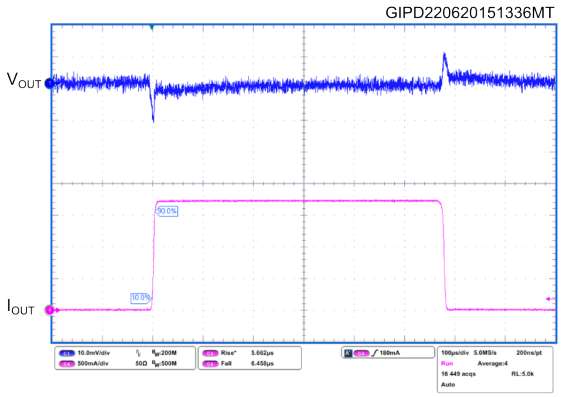


Figure 30. Stability area for ceramic capacitor

C_{IN} = 22 µF, V_{IN} = from 2.5 V to 12 V, I_{OUT} = from 10 mA to 2 A, V_{OUT} = 1.24 V, no C_{byp}, no C_{filter}

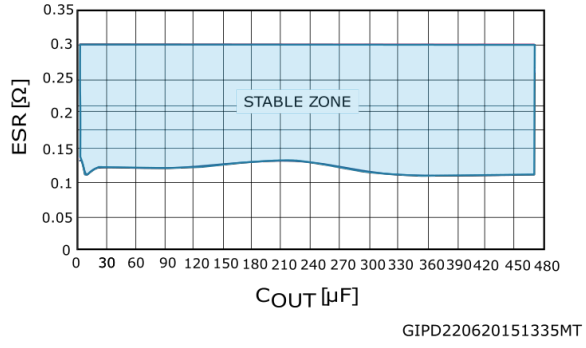
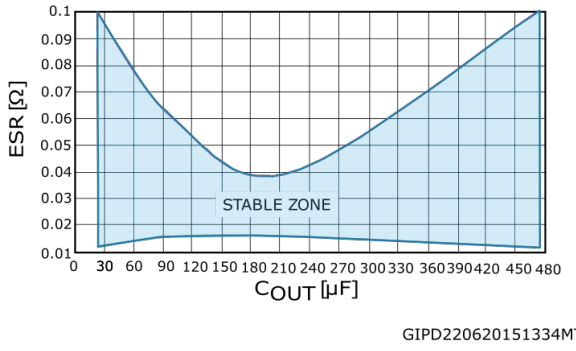


Figure 31. Stability area for tantalum capacitor

C_{IN} = 1 µF, V_{IN} = from 2.5 V to 12 V, I_{OUT} = from 10 mA to 2 A, V_{OUT} = 1.24 V, no C_{byp}, no C_{filter}

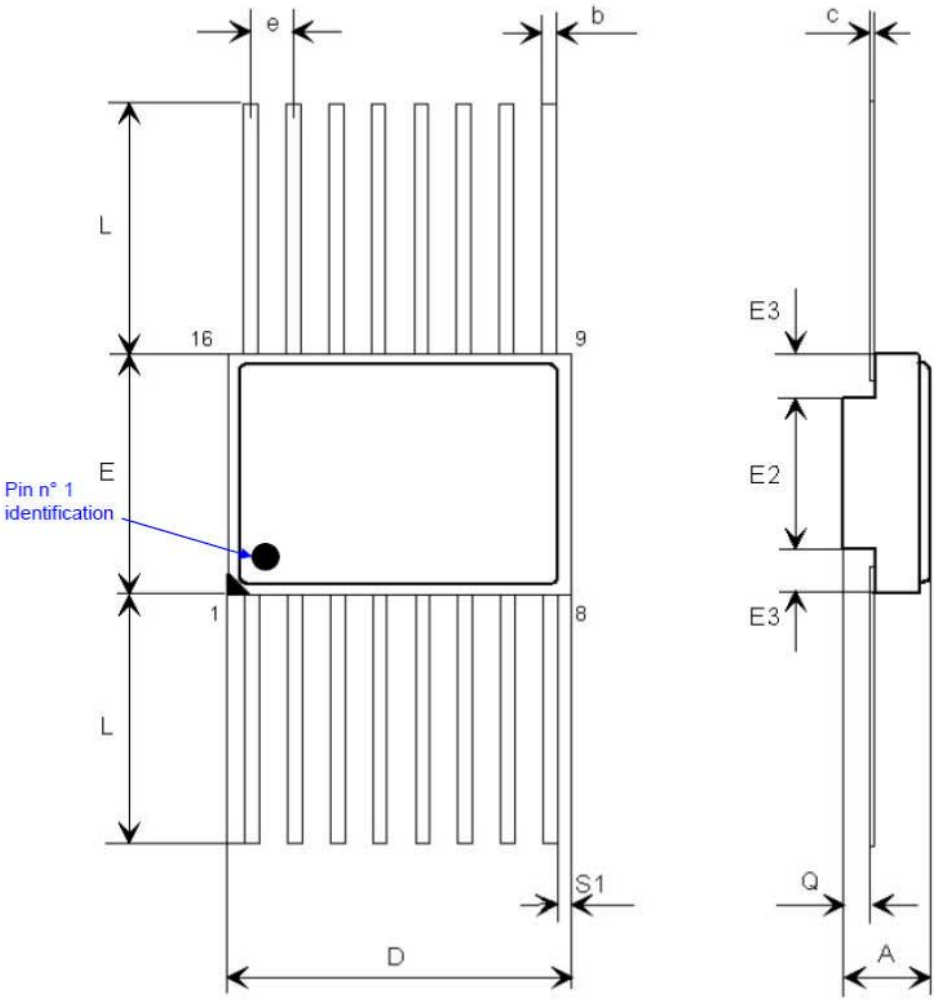


11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 FLAT-16P package information

Figure 32. **FLAT-16P package outline**



8241681_4

Table 11. **FLAT-16P package mechanical data**

Dim.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.42		2.88	0.095		0.113
b	0.38		0.48	0.015		0.019
c	0.10		0.18	0.004		0.007
D	9.71		10.11	0.382		0.398
E	6.71		7.11	0.264		0.280
E2	3.30	3.45	3.60	0.130	0.136	0.142
E3	0.76			0.030		
e		1.27			0.050	
L	6.35		7.36	0.250		0.290
Q	0.66		1.14	0.026		0.045
S1	0.13			0.005		

12 Ordering information

Table 12. Order codes

Part number	SMD pin	Quality level	Package	Lead finish	Marking (1)	Packing
RHFL6000LAKP1	-	Engineering model	Flat-16P	Gold	RHFL6000LKPA1	Strip pack
RHFL6000LAKP01V		QML-V flight	Flat-16P	Gold		Strip pack
RHFL6000LAKP02V		QML-V flight	Flat-16P	Tin		Strip pack

1. *Specific marking only. The full marking includes in addition: - for the engineering models: ST logo, date code, country of origin (FR) - for QML flight parts: ST logo, date code, country of origin (FR), manufacturer code (CSTM), serial number of the part within the assembly lot.*

Contact ST sales office for information about the specific conditions for:

1) Products in die form

2) Other quality levels

3) Tape and reel packing

12.1 Traceability information

Date code in formation is structured as described below:

Table 13. Date code

Model	Date code
EM	3yywwN
QML flight	yywwN

where:

- yy = year
- ww = week number
- N = lot index in the week

12.2 Documentation

The table below gives a summary of the documentation provided with each type of product:

Table 14. Table of documentation by product

Quality level	Documentation
Engineering model	Certificate of conformance
QML-V flight	Certificate of conformance (including group C and D reference) Precap report (100% high and low magnification) SEM report Screening summary Group A summary (quality conformance inspection of electrical tests) Group B summary (quality conformance inspection of mechanical tests) Group E (quality conformance inspection of wafer lot radiation verification test)

Revision history

Table 15. **Document revision history**

Date	Revision	Changes
04-Nov-2022	1	First release.

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List of figures

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