

RJF0604JPD

Silicon N Channel MOS FET Series Power Switching

R07DS0583EJ0200
Rev.2.00
Apr 13, 2012

Description

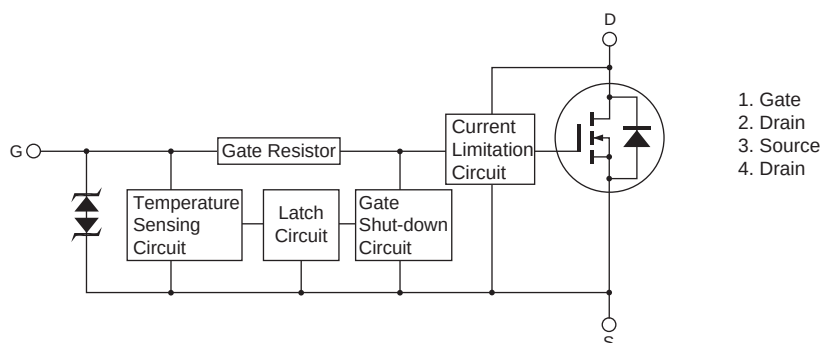
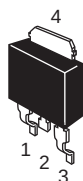
This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation (4 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V and 24 V.
- AEC-Q101 Compliant

Outline

RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	16	V
Gate to source voltage	V_{GSS}	-2.5	V
Drain current	I_D ^{Note 3}	5	A
Body-drain diode reverse drain current	I_{DR}	5	A
Avalanche current	I_{AP} ^{Note 2}	4.7	A
Avalanche energy	E_{AR} ^{Note 2}	94.7	mJ
Channel dissipation	P_{ch} ^{Note 1}	30	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. Value at $T_c = 25^\circ\text{C}$
2. $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
3. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	3.5	—	—	V	
	V_{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I_{IH1}	—	—	100	μA	$V_i = 8 V, V_{DS} = 0$
	I_{IH2}	—	—	50	μA	$V_i = 3.5 V, V_{DS} = 0$
	I_{IL}	—	—	1	μA	$V_i = 1.2 V, V_{DS} = 0$
Input current (Gate shut down)	$I_{IH(sd)1}$	—	0.8	—	mA	$V_i = 8 V, V_{DS} = 0$
	$I_{IH(sd)2}$	—	0.35	—	mA	$V_i = 3.5 V, V_{DS} = 0$
Shut down temperature	Tsd	—	175	—	°C	Channel temperature
Gate operation voltage	Vop	3.5	—	12	V	
Drain current (Current limitation value)	$I_{D \text{ limit}}$	5	—	—	A	$V_{GS} = 5 V, V_{DS} = 10 V$ ^{Note 4}

Note; 4. Pulse test

Electrical Characteristics

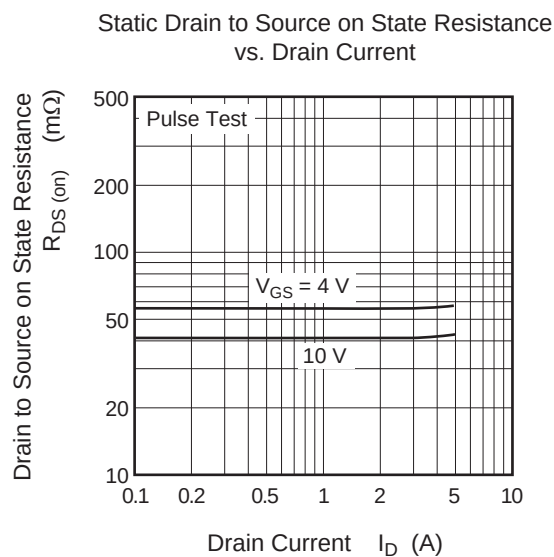
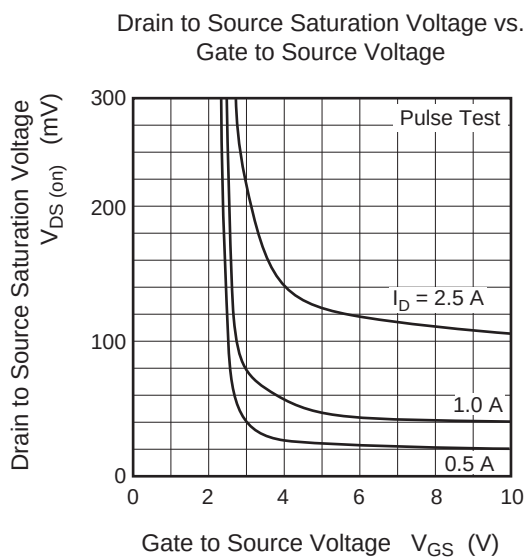
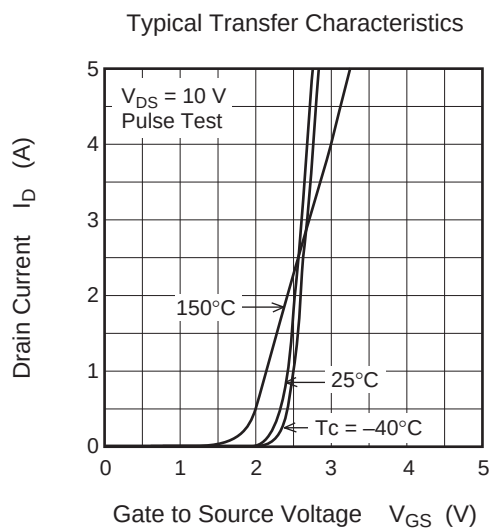
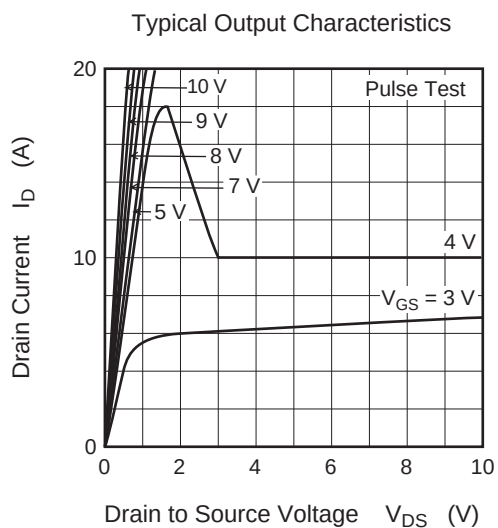
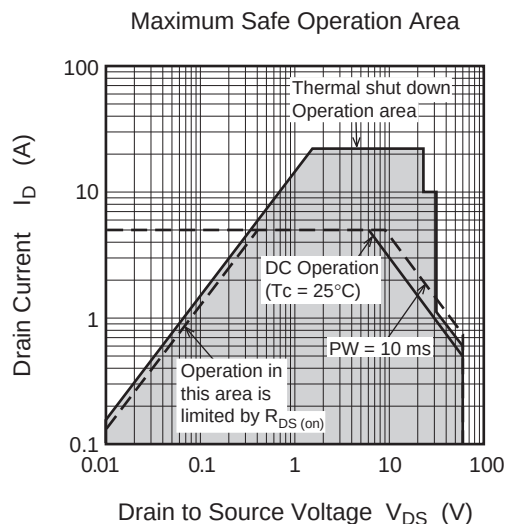
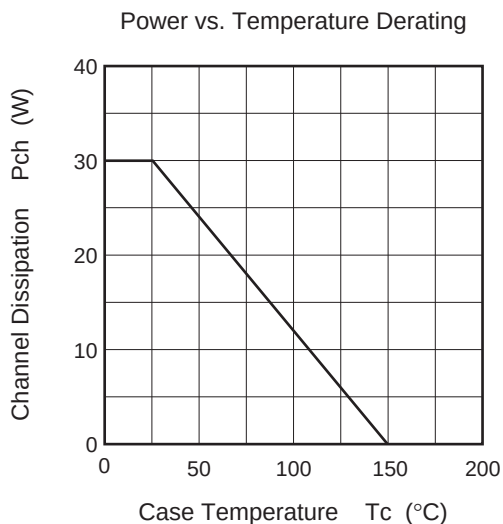
(Ta = 25°C)

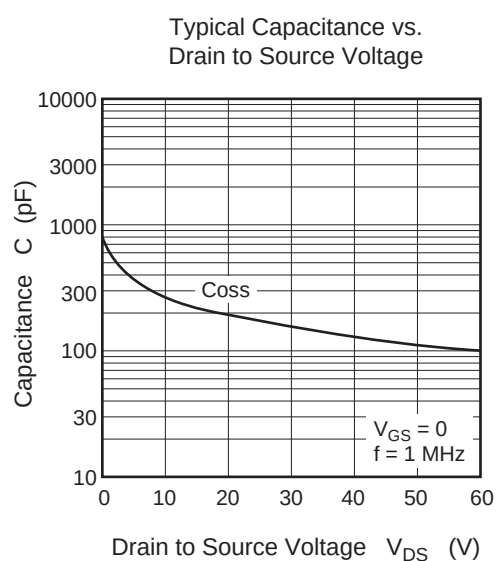
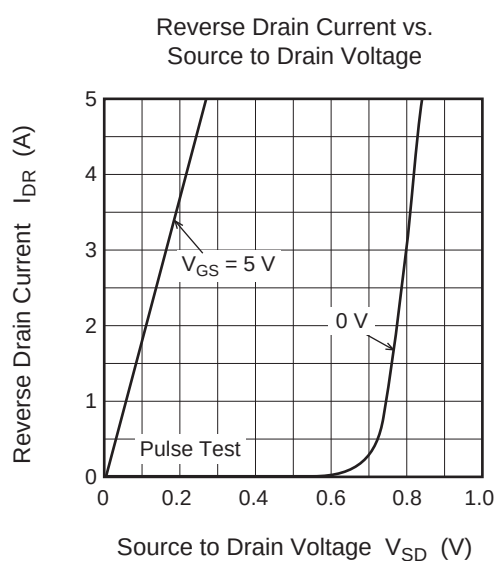
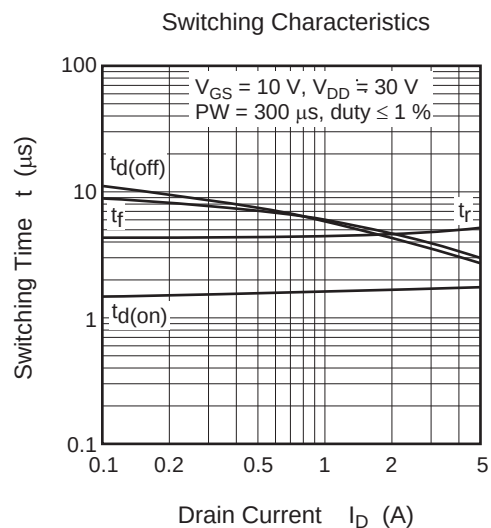
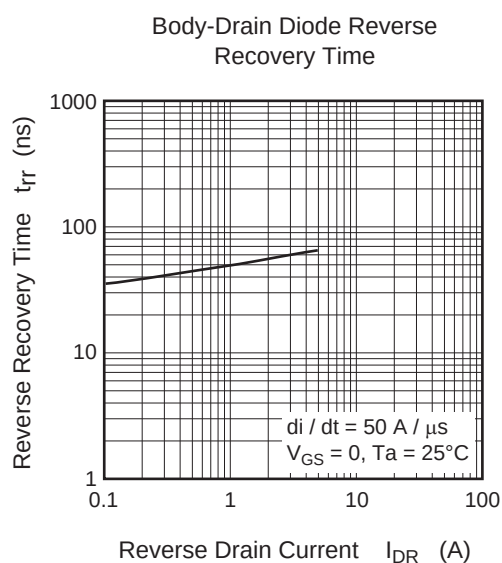
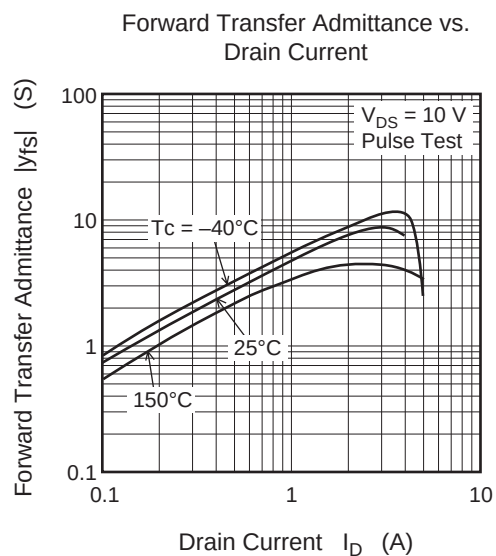
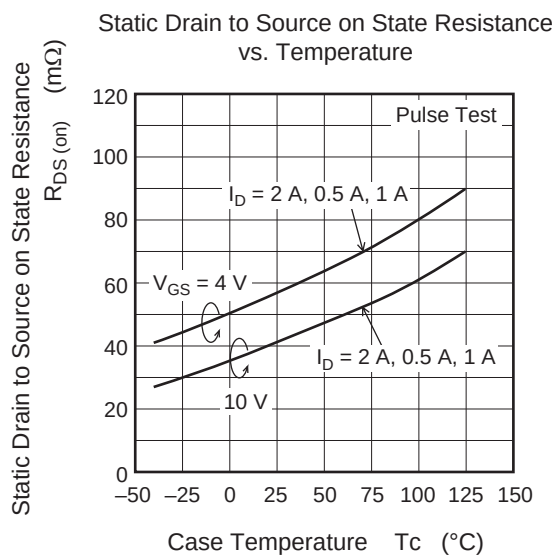
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	—	—	17	A	$V_{GS} = 3.5 V, V_{DS} = 10 V$ ^{Note 5}
	I_{D2}	—	—	10	mA	$V_{GS} = 1.2 V, V_{DS} = 10 V$
	I_{D3}	5	—	—	A	$V_{GS} = 5 V, V_{DS} = 10 V$ ^{Note 5}
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	16	—	—	V	$I_G = 800 \mu A, V_{DS} = 0$
	$V_{(BR)GSS}$	-2.5	—	—	V	$I_G = -100 \mu A, V_{DS} = 0$
Gate to source leak current	I_{GSS1}	—	—	100	μA	$V_{GS} = 8 V, V_{DS} = 0$
	I_{GSS2}	—	—	50	μA	$V_{GS} = 3.5 V, V_{DS} = 0$
	I_{GSS3}	—	—	1	μA	$V_{GS} = 1.2 V, V_{DS} = 0$
	I_{GSS4}	—	—	-100	μA	$V_{GS} = -2.4 V, V_{DS} = 0$
Input current (shut down)	$I_{GS(OP)1}$	—	0.8	—	mA	$V_{GS} = 8 V, V_{DS} = 0$
	$I_{GS(OP)2}$	—	0.35	—	mA	$V_{GS} = 3.5 V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 32 V, V_{GS} = 0, T_c = 110^\circ C$
Gate to source cutoff voltage	$V_{GS(off)}$	1.1	—	2.1	V	$V_{DS} = 10 V, I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	4	9	—	S	$I_D = 2.5 \text{ A}, V_{DS} = 10 V$ ^{Note 5}
Static drain to source on state resistance	$R_{DS(on)}$	—	58	100	m Ω	$I_D = 2.5 \text{ A}, V_{GS} = 4 V$ ^{Note 5}
	$R_{DS(on)}$	—	42	75	m Ω	$I_D = 2.5 \text{ A}, V_{GS} = 10 V$ ^{Note 5}
Output capacitance	Coss	—	276	—	pF	$V_{DS} = 10 V, V_{GS} = 0, f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	1.6	—	μs	$V_{GS} = 10 V, I_D = 2.5 \text{ A}, R_L = 12 \Omega$
Rise time	t_r	—	4.7	—	μs	
Turn-off delay time	$t_{d(off)}$	—	3.7	—	μs	
Fall time	t_f	—	4.4	—	μs	
Body-drain diode forward voltage	V_{DF}	—	0.81	—	V	$I_F = 5 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	67	—	ns	$I_F = 5 \text{ A}, V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$
Over load shut down operation time ^{Note 6}	t_{os1}	—	3.4	—	ms	$V_{GS} = 5 V, V_{DD} = 16 V$
	t_{os2}	—	1.2	—	ms	$V_{GS} = 5 V, V_{DD} = 24 V$

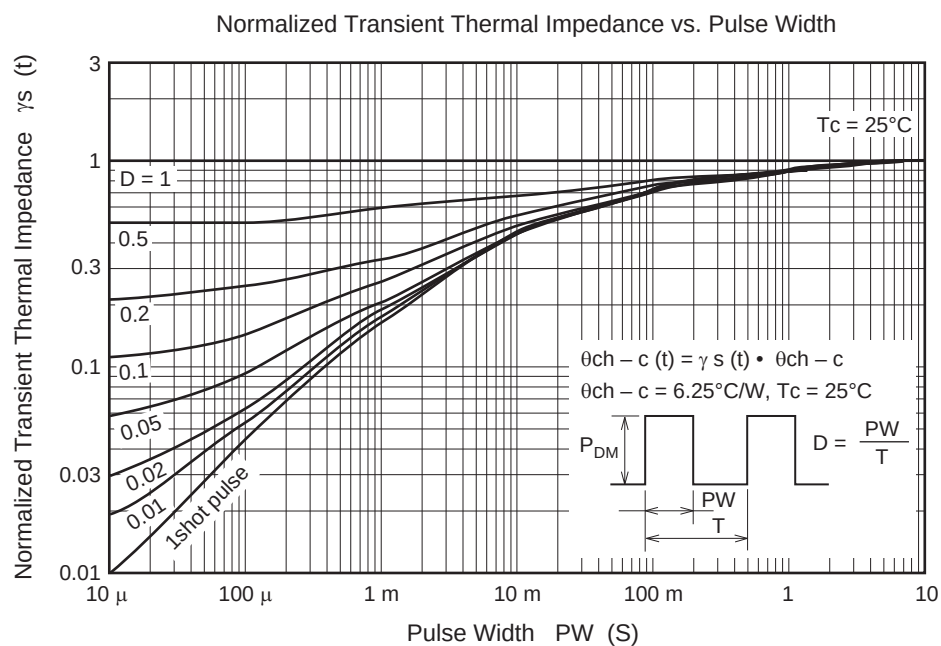
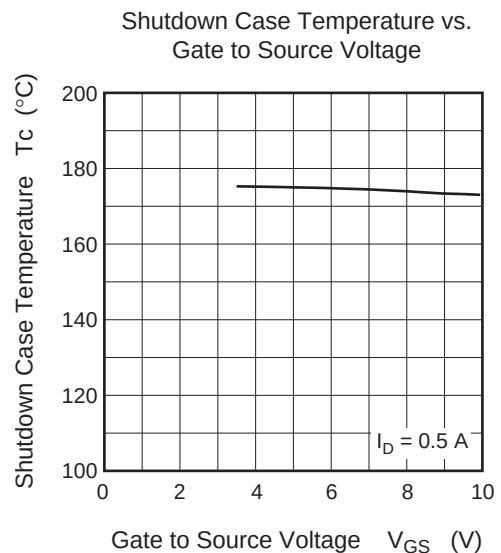
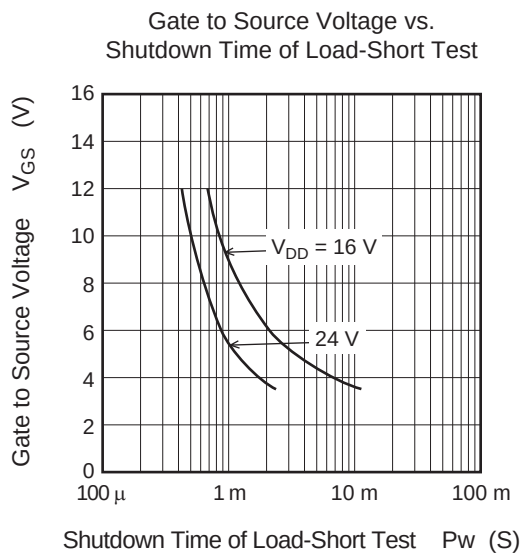
Notes: 5. Pulse test

6. Including the junction temperature rise of the over loaded condition.

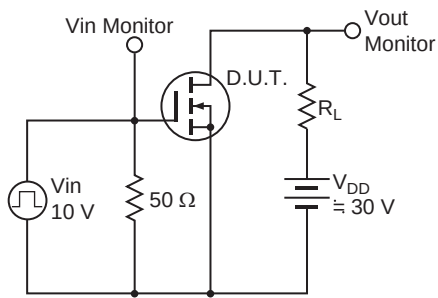
Main Characteristics



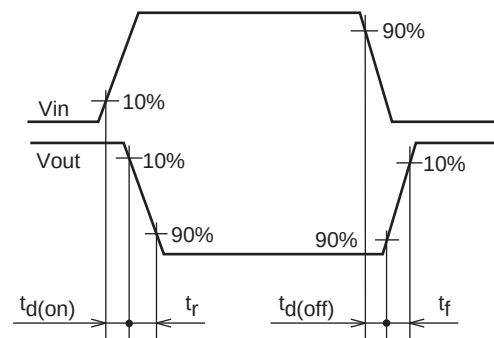




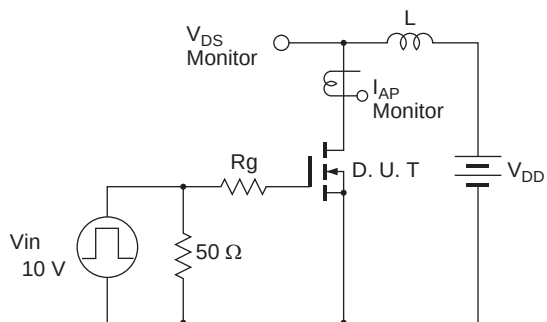
Switching Time Test Circuit



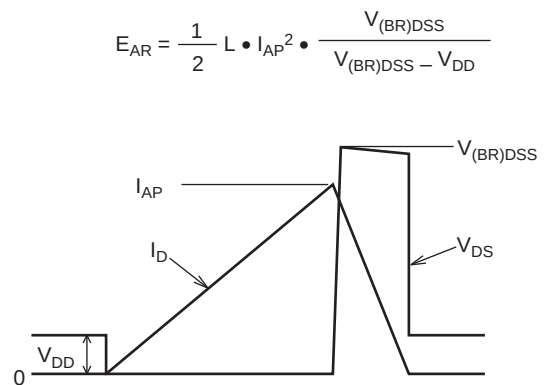
Waveform



Avalanche Test Circuit



Avalanche Waveform



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