RJK0212DPA

Silicon N Channel Power MOS FET
Power Switching

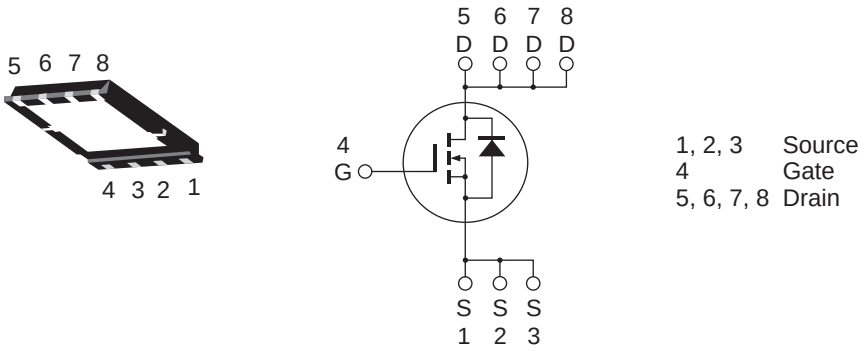
REJ03G1950-0011
Rev.0.11
Jul 02, 2010

Features

- Very high speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 9 mΩ typ. (at V_{GS} = 10 V)
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PWSN0008DC-A
(Package name: WPAK(2))



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	25	V
Gate to source voltage	V_{GSS}	+16, –12	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$ Note1	100	A
Body-drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP} Note 2	16	A
Avalanche energy	E_{AR} Note 2	32	mJ
Channel dissipation	Pch Note3	30	W
Channel to case thermal resistance	θch-c Note3	4.17	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C

Electrical Characteristics

(Ta = 25°C)

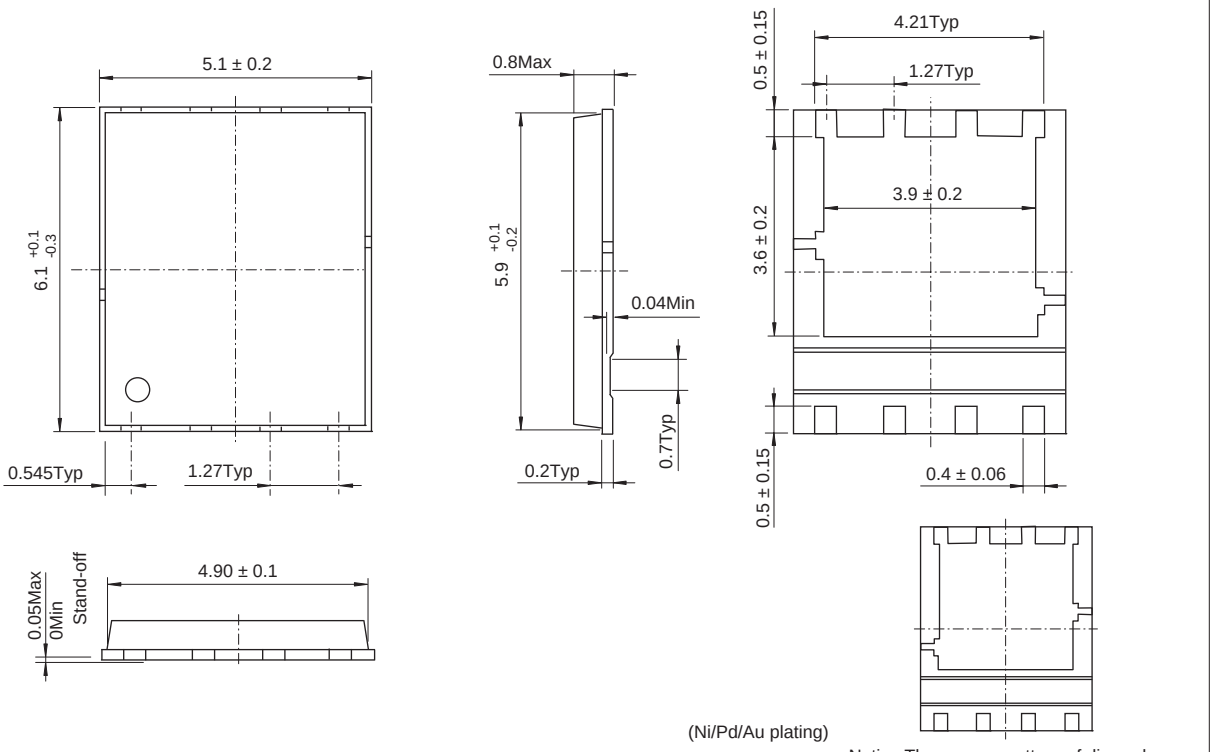
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	25	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = +16, –12 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	9	10.8	mΩ	I_D = 12.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	12	15.6	mΩ	I_D = 12.5 A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	—	40	—	S	I_D = 12.5 A, V_{DS} = 5 V Note4
Input capacitance	Ciss	—	1030	1440	pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	340	—	pF	
Reverse transfer capacitance	Crss	—	14	—	pF	
Gate Resistance	Rg	—	1.5	2.5	Ω	
Total gate charge	Qg	—	5.4	—	nC	V_{DD} = 10 V V_{GS} = 4.5 V I_D = 25 A
Gate to source charge	Qgs	—	2.8	—	nC	
Gate to drain charge	Qgd	—	0.6	—	nC	
Turn-on delay time	$t_{d(on)}$	—	TBD	—	ns	V_{GS} = 10 V, I_D = 12.5 A V_{DD} ≅ 10 V R_L = 0.8 Ω Rg = 4.7 Ω
Rise time	t_r	—	TBD	—	ns	
Turn-off delay time	$t_{d(off)}$	—	TBD	—	ns	
Fall time	t_f	—	TBD	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.83	1.08	V	IF = 25 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	TBD	—	ns	IF =25 A, V_{GS} = 0 di_F/dt = 100 A/μs

Notes: 4. Pulse test

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
WPAK(2)	—	PWSN0008DC-A	WPAK(2)V	0.07g

Unit: mm



Notice: The reverse pattern of die-pad support lead described above exists.

Ordering Information

Part No.	Quantity	Shipping Container
RJK0212DPA-00-J53	3000 pcs	Taping

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