

RJK0352DSP

Silicon N Channel Power MOS FET Power Switching

REJ03G1660-0501 Rev.5.01 Apr 24, 2008

Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance $R_{DS(on)}\!=4.3~\text{m}\Omega~\text{typ.}~(\text{at }V_{GS}=10~\text{V})$
- Pb-free

Outline

RENESAS Package code: PRSP0008DD-D (Package name: SOP-8<FP-8DAV>)

8765

BDDDDD

1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$

			(1a 25 c)
Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	30	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	18	Α
Drain peak current	I _{D(pulse)} Note1	144	Α
Body-drain diode reverse drain current	I _{DR}	18	Α
Avalanche current	I _{AP} Note 2	17	Α
Avalanche energy	E _{AR} Note 2	28.9	mJ
Channel dissipation	Pch Note3	2.0	W
Channel to ambient thermal impedance	θch-a Note3	62.5	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

- Notes: 1. PW \leq 10 μ s, duty cycle \leq 1%
 - 2. Value at Tch = 25°C, Rg \geq 50 Ω
 - 3. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW \leq 10s

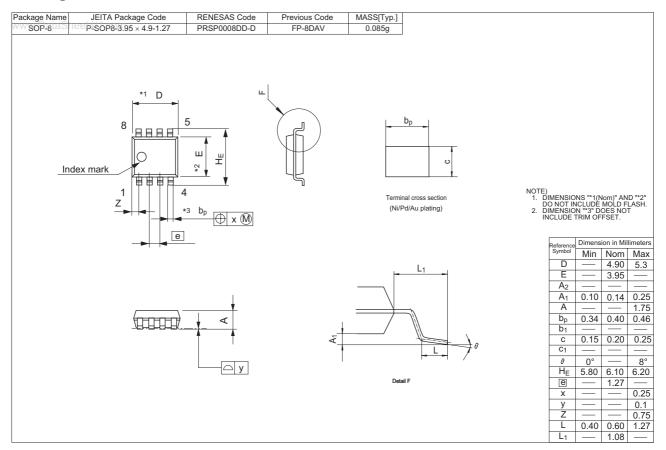
Electrical Characteristics

 $(Ta = 25^{\circ}C)$

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	30	_	_	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I _{GSS}	_	_	± 0.1	μΑ	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}	_	_	1	μΑ	$V_{DS} = 30 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	V _{GS(off)}	1.2	_	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state	R _{DS(on)}	_	4.3	5.6	mΩ	I _D = 9 A, V _{GS} = 10 V Note4
resistance	R _{DS(on)}	_	5.5	7.0	mΩ	$I_D = 9 \text{ A}, V_{GS} = 4.5 \text{ V}^{\text{Note4}}$
Forward transfer admittance	y _{fs}	_	41	_	S	I _D = 9 A, V _{DS} = 10 V Note4
Input capacitance	Ciss	_	2440	_	pF	V _{DS} = 10 V
Output capacitance	Coss	_	470	_	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	_	150	_	pF	f = 1 MHz
Gate Resistance	Rg	_	2.1	_	Ω	
Total gate charge	Qg	_	16	_	nC	V _{DD} = 10 V
Gate to source charge	Qgs	_	6.0	_	nC	V _{GS} = 4.5 V
Gate to drain charge	Qgd	_	3.4	_	nC	I _D = 9 A
Turn-on delay time	t _{d(on)}	_	8.6	_	ns	V _{GS} = 10 V, I _D = 9 A
Rise time	t _r	_	4.5	_	ns	V _{DD} ≅ 10 V
Turn-off delay time	t _{d(off)}	_	51.6	_	ns	$R_L = 1.11 \Omega$
Fall time	t _f	_	6.5	_	ns	$Rg = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	_	0.8	1.04	V	$I_F = 18 \text{ A}, V_{GS} = 0^{\text{Note4}}$
Body-drain diode reverse recovery	t _{rr}	_	25	_	ns	I _F = 18 A, V _{GS} = 0
time						$di_F/dt = 100 A/ \mu s$

Notes: 4. Pulse test

Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RJK0352DSP-00-J0	2500 pcs	Taping

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