

RJK0358DSP

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Silicon N Channel Power MOS FET Power Switching

REJ03G1652-0501

Rev.5.01

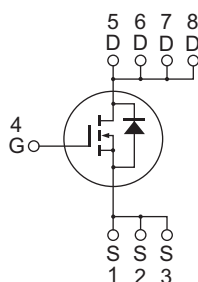
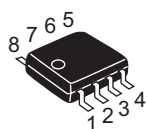
Apr 24, 2008

Features

- Capable of 5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 3.2 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)
- Pb-free

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8<FP-8DAV>)



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	160	A
Body-drain diode reverse drain current	I_{DR}	20	A
Avalanche current	I_{AP} ^{Note 2}	19	A
Avalanche energy	E_{AR} ^{Note 2}	36.1	mJ
Channel dissipation	P_{ch} ^{Note 3}	2.5	W
Channel to ambient thermal impedance	θ_{ch-a} ^{Note 3}	50	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

3. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10\text{s}$

Electrical Characteristics

(Ta = 25°C)

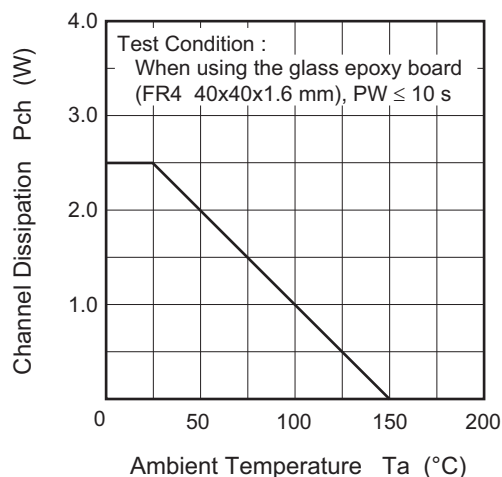
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.2	4.2	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	4.4	6.2	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	35	—	S	$I_D = 10 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	4300	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	500	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	280	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	33	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	13	—	nC	$V_{GS} = 5 \text{ V}$
Gate to drain charge	Q_{gd}	—	8	—	nC	$I_D = 20 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$
Rise time	t_r	—	5.6	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	76	—	ns	$R_L = 1.0 \Omega$
Fall time	t_f	—	10	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.80	1.04	V	$I_F = 20 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	25	—	ns	$I_F = 20 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

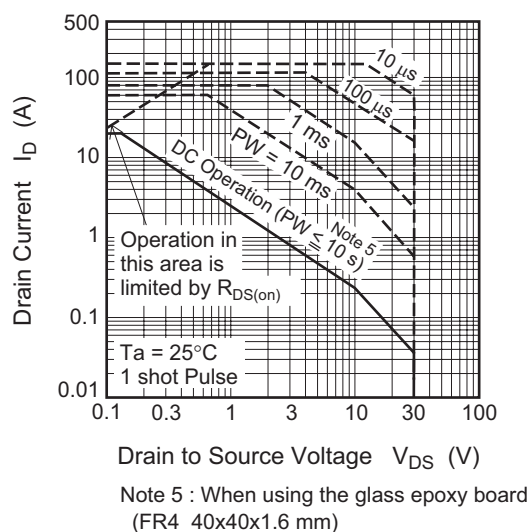
Main Characteristics

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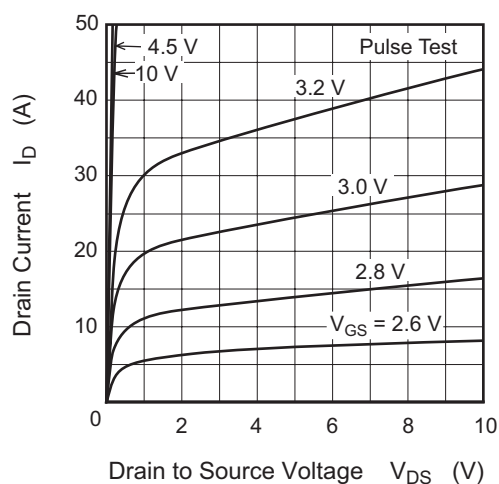
Power vs. Temperature Derating



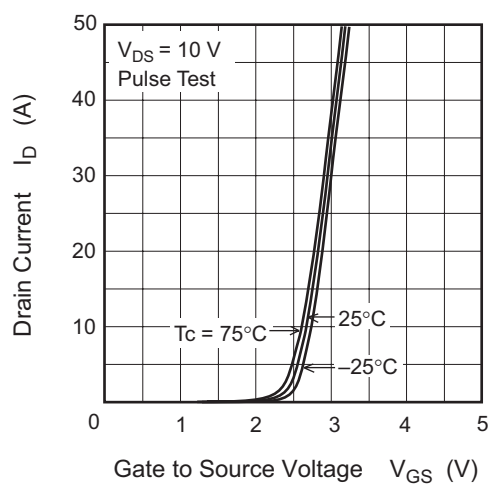
Maximum Safe Operation Area



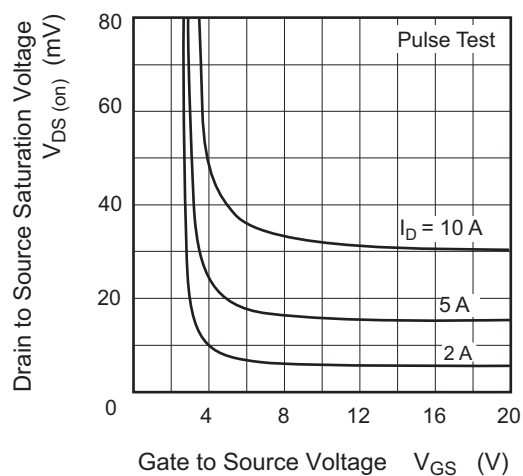
Typical Output Characteristics



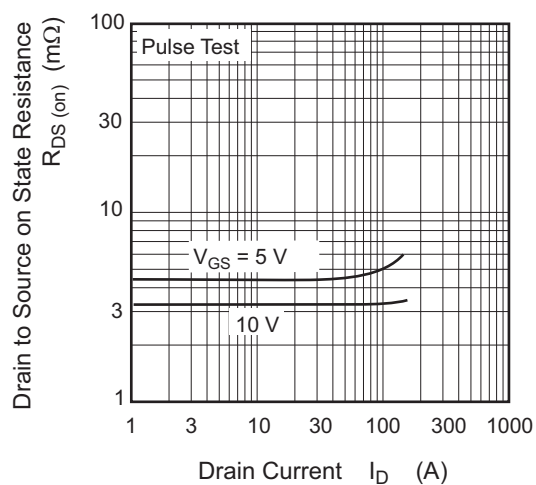
Typical Transfer Characteristics



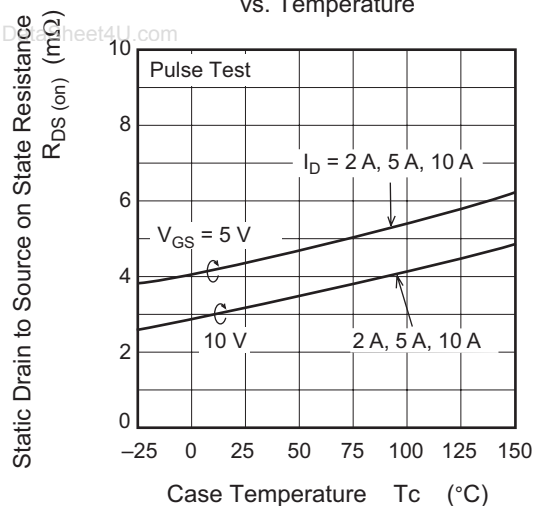
Drain to Source Saturation Voltage vs. Gate to Source Voltage



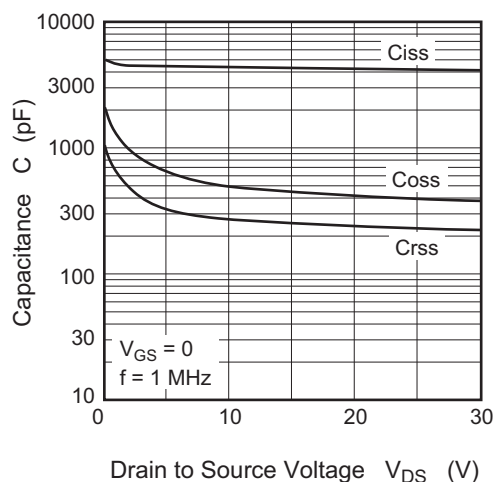
Static Drain to Source on State Resistance vs. Drain Current



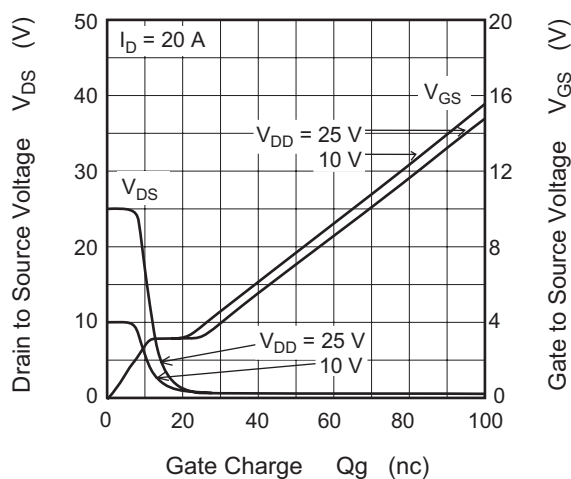
Static Drain to Source on State Resistance vs. Temperature



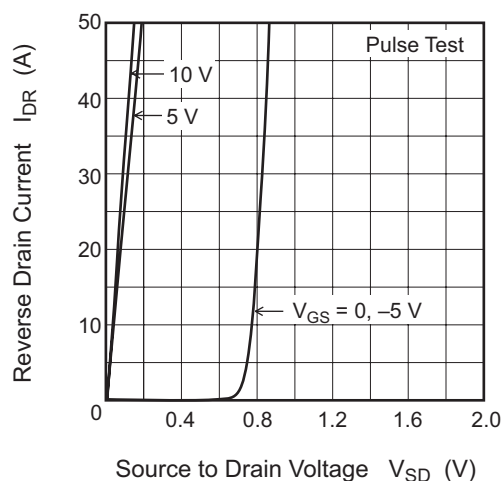
Typical Capacitance vs. Drain to Source Voltage



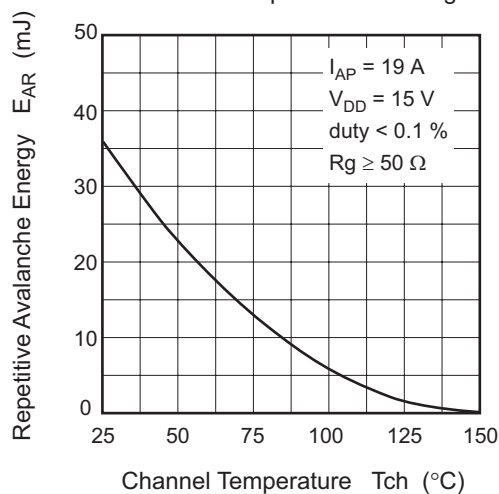
Dynamic Input Characteristics

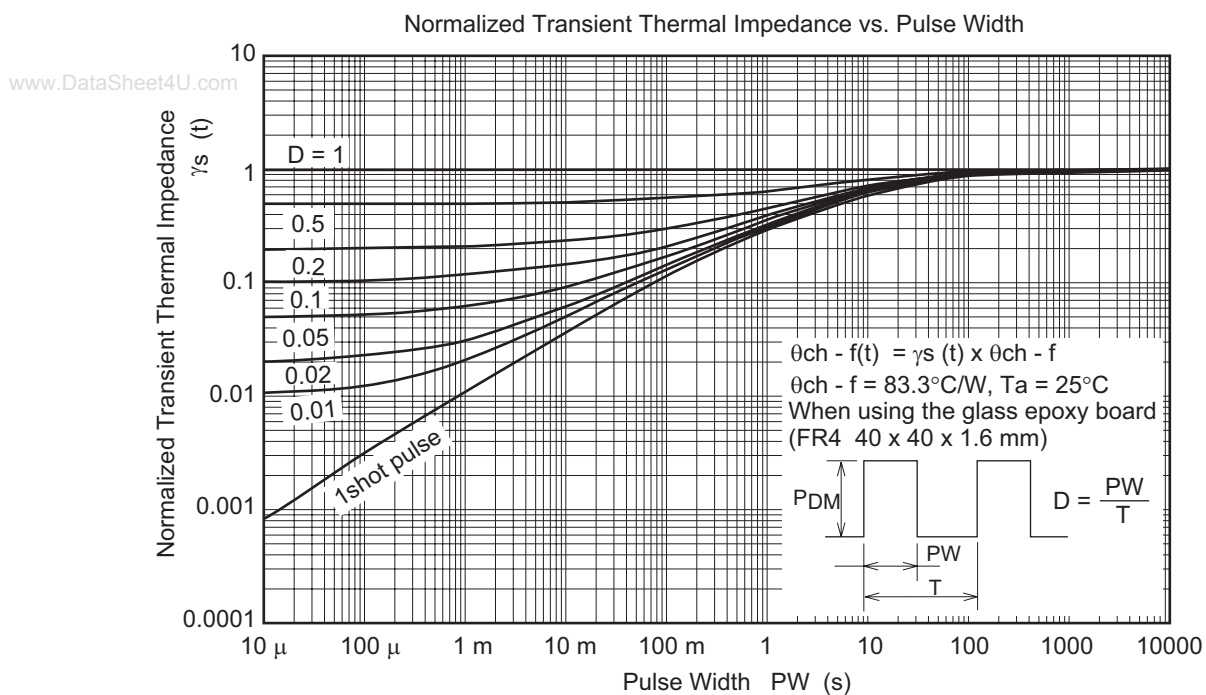


Reverse Drain Current vs. Source to Drain Voltage

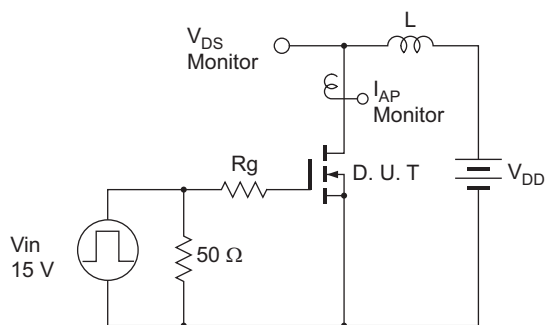


Maximum Avalanche Energy vs. Channel Temperature Derating

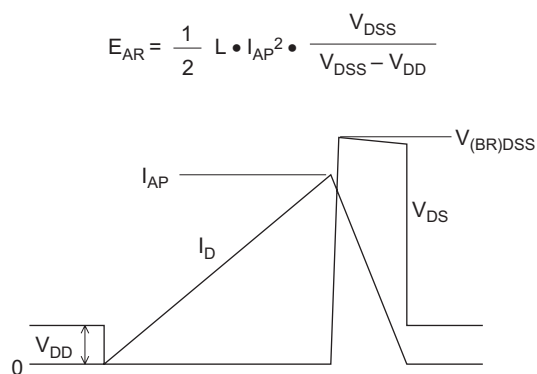




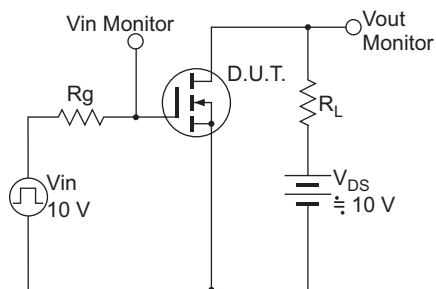
Avalanche Test Circuit



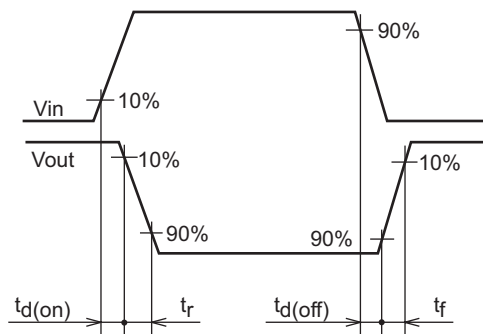
Avalanche Waveform



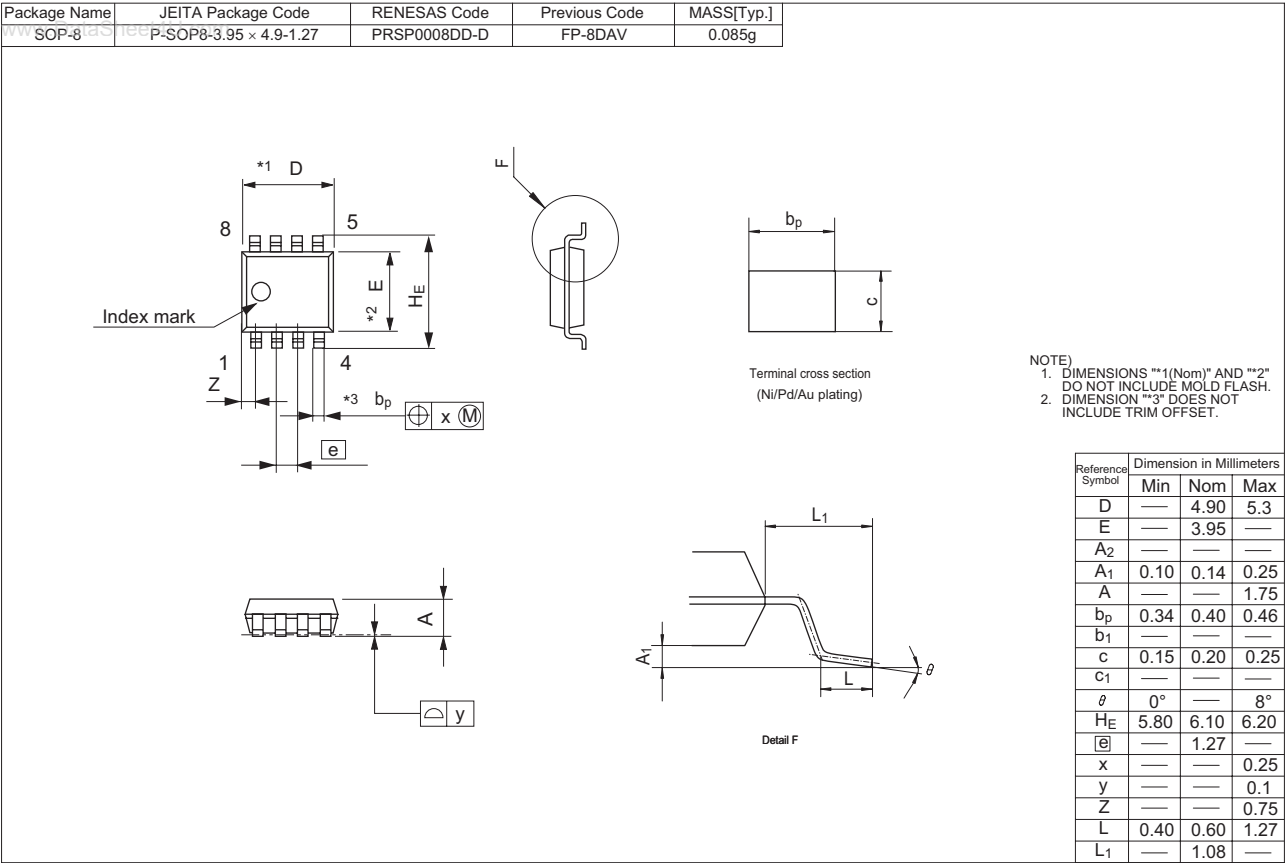
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RJK0358DSP-00-J0	2500 pcs	Taping

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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