

RJK03F8DNS

Silicon N Channel Power MOS FET Power Switching

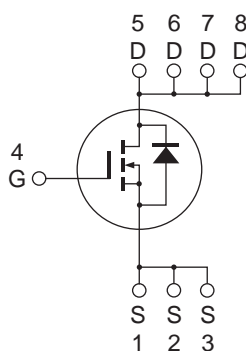
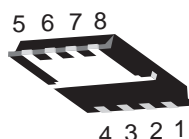
REJ03G1918-0100
Rev.1.00
Apr 21, 2010

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 7 \text{ m}\Omega$ typ. (at $V_{GS} = 8 \text{ V}$)
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PWSN0008JB-A
(Package name: HWSN-8)



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 12	V
Drain current	I_D	16	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	64	A
Body-drain diode reverse drain current	I_{DR}	16	A
Avalanche current	I_{AP} ^{Note 2}	10	A
Avalanche energy	E_{AR} ^{Note 2}	10	mJ
Channel dissipation	P_{ch} ^{Note 3}	12.5	W
Channel to case thermal impedance	θ_{ch-c} ^{Note 3}	10.0	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
3. $T_c = 25^\circ\text{C}$

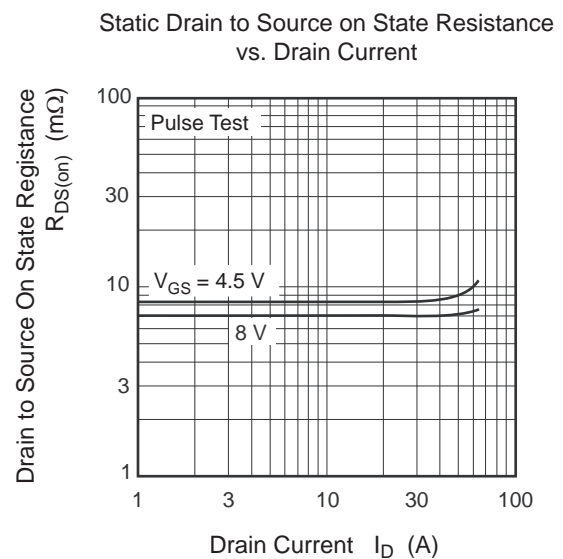
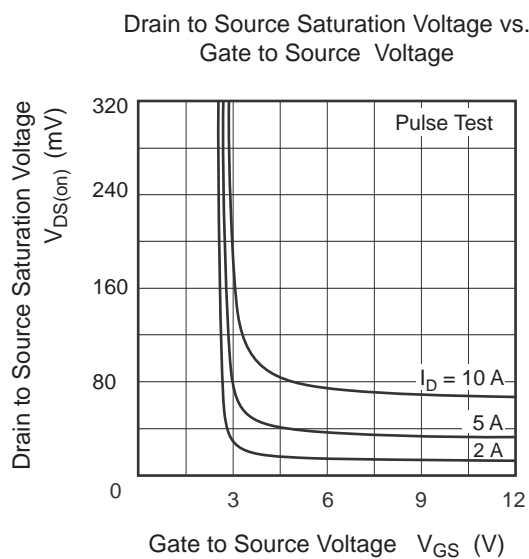
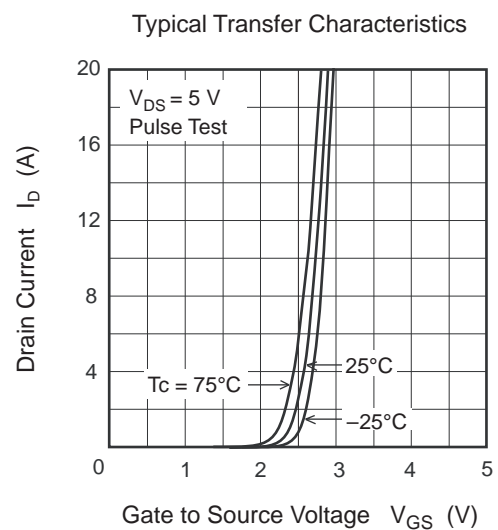
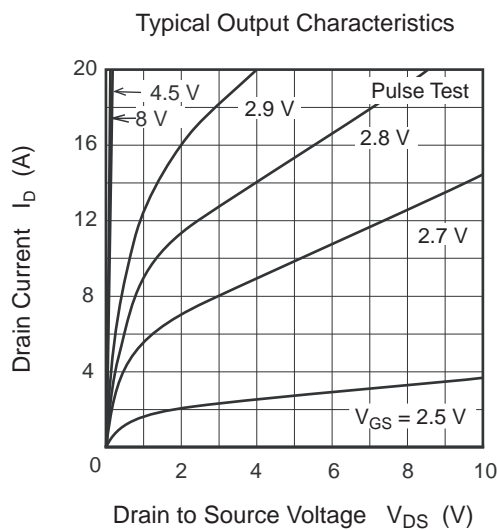
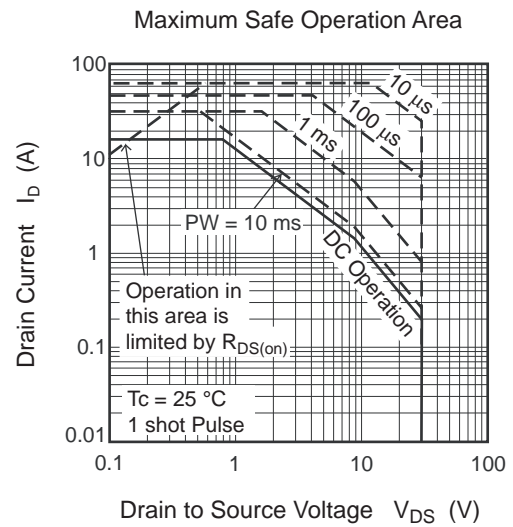
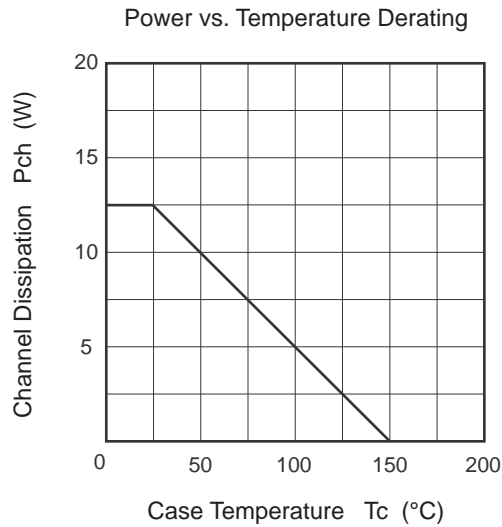
Electrical Characteristics

(Ta = 25°C)

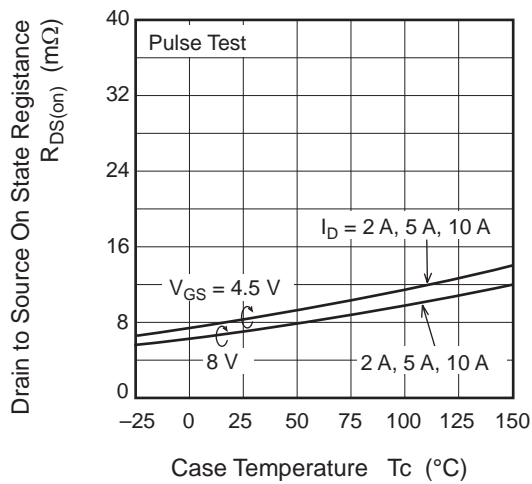
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 12 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	7	8.4	$\text{m}\Omega$	$I_D = 8 \text{ A}$, $V_{GS} = 8 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	8.3	10.4	$\text{m}\Omega$	$I_D = 8 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	40	—	S	$I_D = 8 \text{ A}$, $V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1500	2100	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	162	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	104	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	0.7	1.9	Ω	
Total gate charge	Q_g	—	11.3	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	3.5	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	4.6	—	nC	$I_D = 16 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	12.8	—	ns	$V_{GS} = 8 \text{ V}$, $I_D = 8 \text{ A}$
Rise time	t_r	—	8.0	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	38.1	—	ns	$R_L = 1.25 \Omega$
Fall time	t_f	—	6.8	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.85	1.11	V	$I_F = 16 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	21	—	ns	$I_F = 16 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

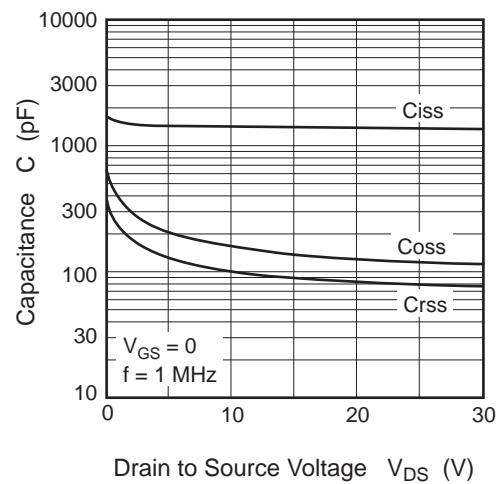
Main Characteristics



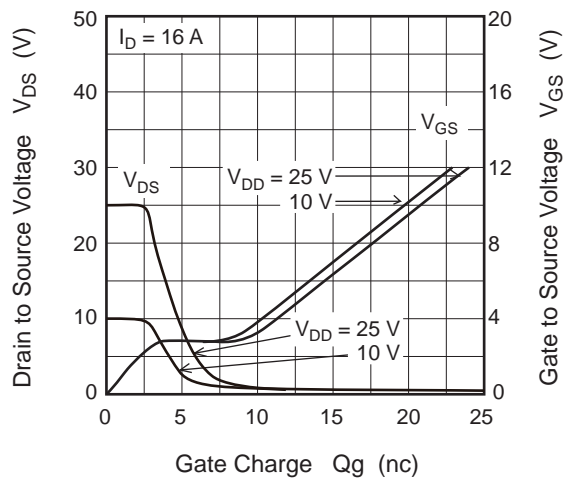
Static Drain to Source on State Resistance vs. Temperature



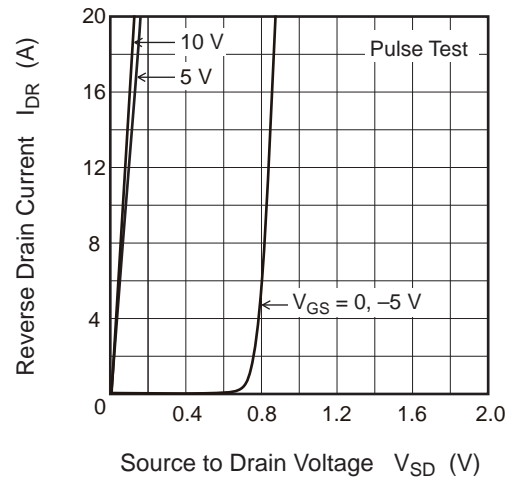
Typical Capacitance vs. Drain to Source Voltage



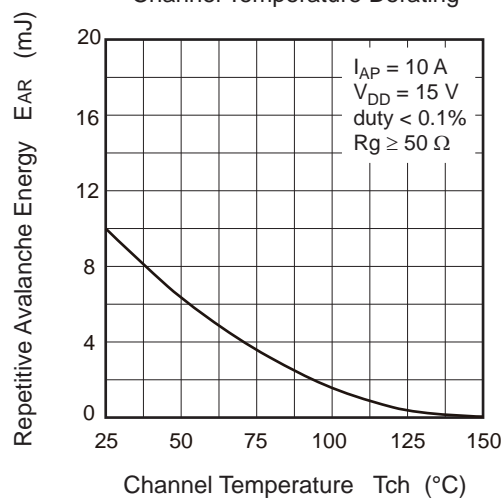
Dynamic Input Characteristics



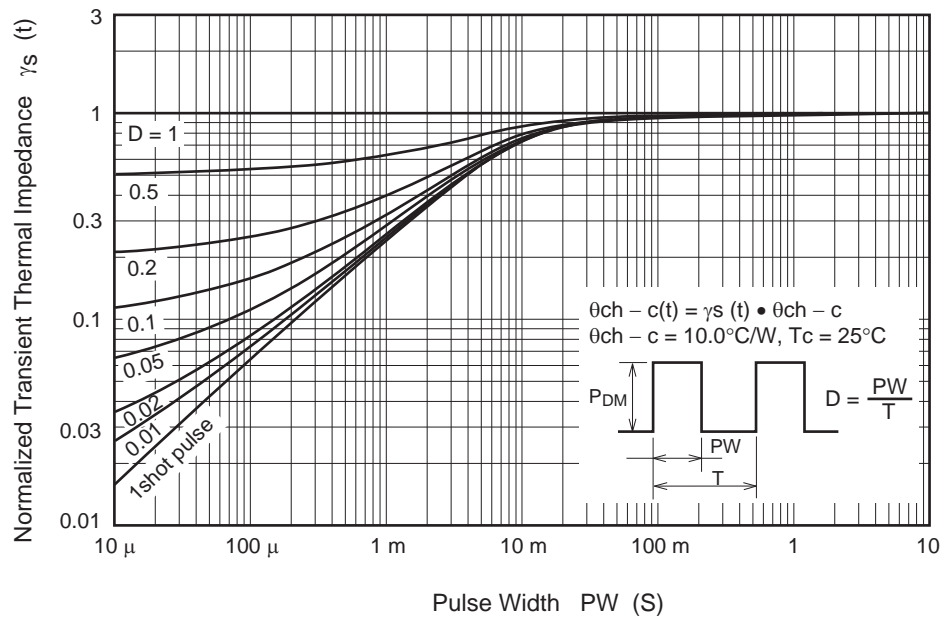
Reverse Drain Current vs. Source to Drain Voltage



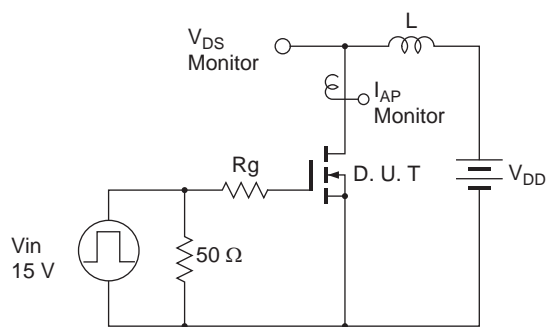
Maximum Avalanche Energy vs. Channel Temperature Derating



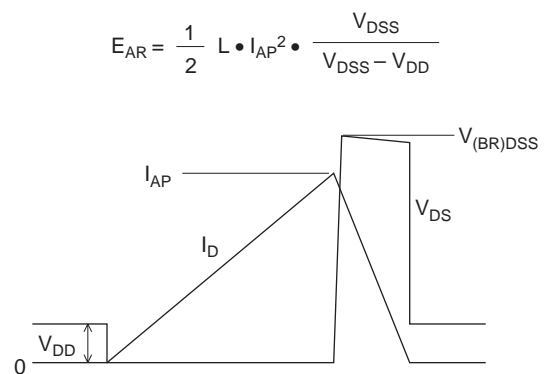
Normalized Transient Thermal Impedance vs. Pulse Width



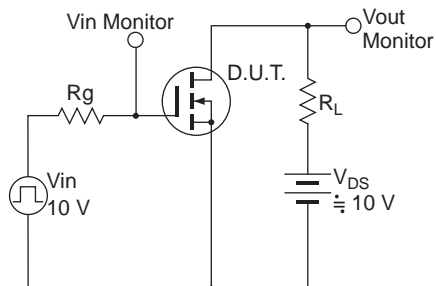
Avalanche Test Circuit



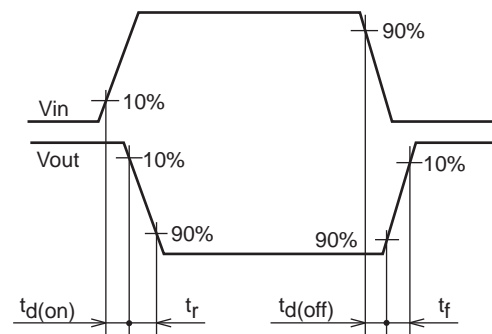
Avalanche Waveform



Switching Time Test Circuit

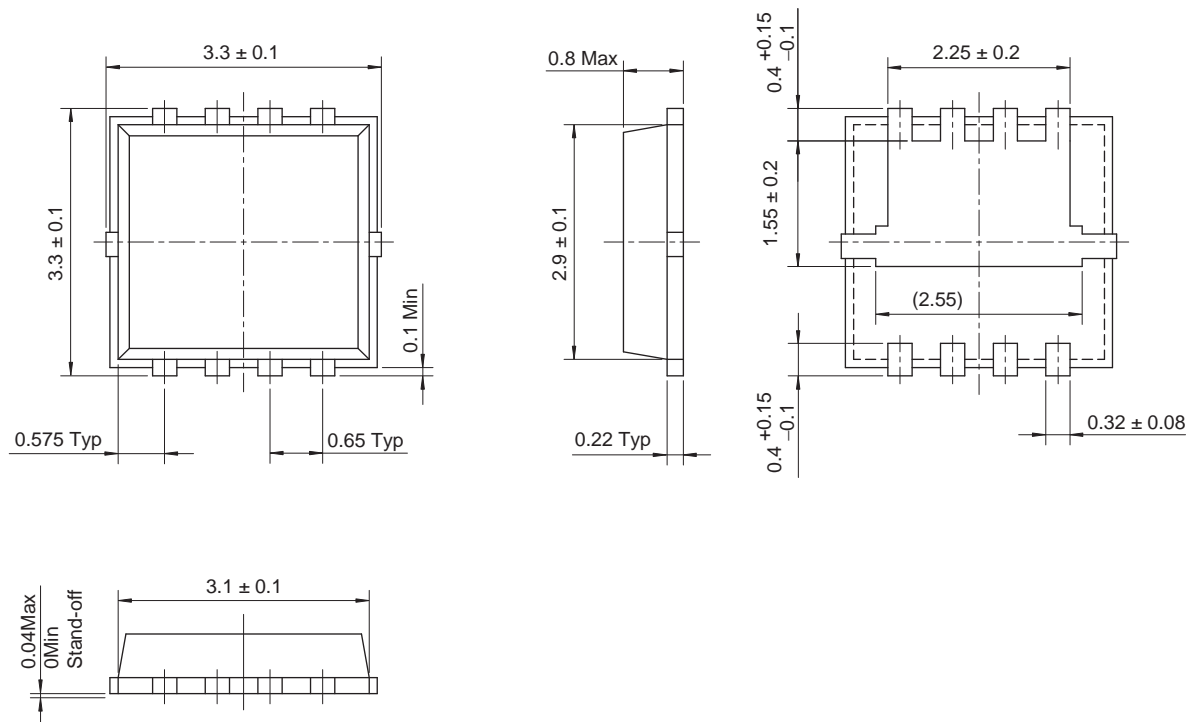


Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
HWS0N-8	P-HWS0N8-2.9x3.1-0.65	PWSN0008JB-A	—	0.022g



Ordering Information

Part No.	Quantity	Shipping Container
RJK03F8DNS-00-J5	5000 pcs	Taping

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Renesas Electronics America Inc.

2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
 Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
 Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
 Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
 Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

7th Floor, Quantum Plaza, No.27 Zhichunlu Haidian District, Beijing 100083, P.R.China
 Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
 Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
 Tel: +852-2886-9318, Fax: +852-2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

7F, No. 363 Fu Shing North Road Taipei, Taiwan
 Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
 Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
 Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

11F., Samik Laviel' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
 Tel: +82-2-558-3737, Fax: +82-2-558-5141