

# RJK4002DJE

400V - 3A - MOS FET  
High Speed Power Switching

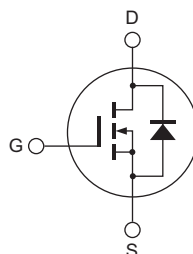
R07DS0842EJ0200  
Rev.2.00  
Aug 03, 2012

## Features

- Low on-state resistance  
 $R_{DS(on)} = 2.4 \Omega$  typ. (at  $I_D = 1.5 A$ ,  $V_{GS} = 10 V$ ,  $T_a = 25^\circ C$ )
- High speed switching

## Outline

RENESAS Package code: PRSS0003DC-A  
(Package name: TO-92 Mod)



1. Source
2. Drain
3. Gate

## Absolute Maximum Ratings

( $T_a = 25^\circ C$ )

Item	Symbol	Value	Unit
Drain to source voltage	$V_{DSS}$	400	V
Gate to source voltage	$V_{GSS}$	$\pm 30$	V
Drain current	$I_D$ <sup>Note1</sup>	3	A
Drain peak current	$I_{D(pulse)}$ <sup>Note4</sup>	6	A
Body-drain diode reverse drain current	$I_{DR}$ <sup>Note1</sup>	3	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ <sup>Note4</sup>	6	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	2.5	A
Avalanche energy	$E_{AR}$ <sup>Note3</sup>	0.357	mJ
Channel dissipation	$P_{ch}$ <sup>Note 2</sup>	2.54	W
Channel to ambient thermal Impedance	$\theta_{ch-a}$	49.2	$^\circ C/W$
Channel temperature	$T_{ch}$	150	$^\circ C$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ C$

- Notes: 1. Limited by  $T_{ch}$  max.  
 2. Value at  $T_c = 25^\circ C$   
 3.  $ST_{ch} = 25^\circ C$ ,  $T_{ch} \leq 150^\circ C$   
 4. Pulse width limited by safe operating area.

## Electrical Characteristics

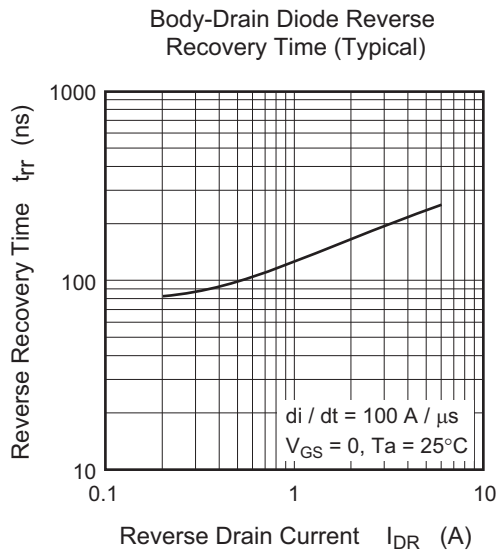
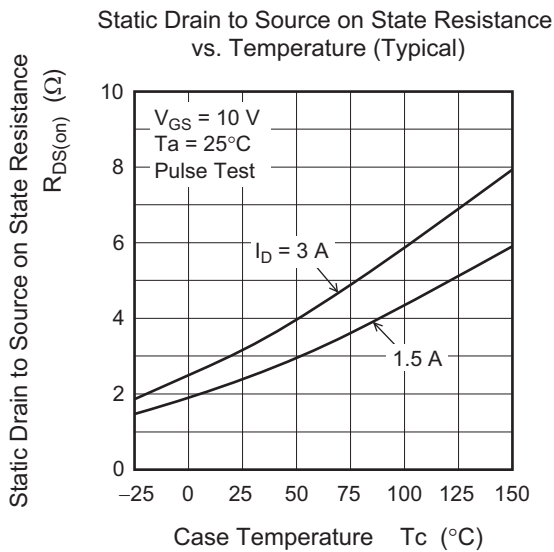
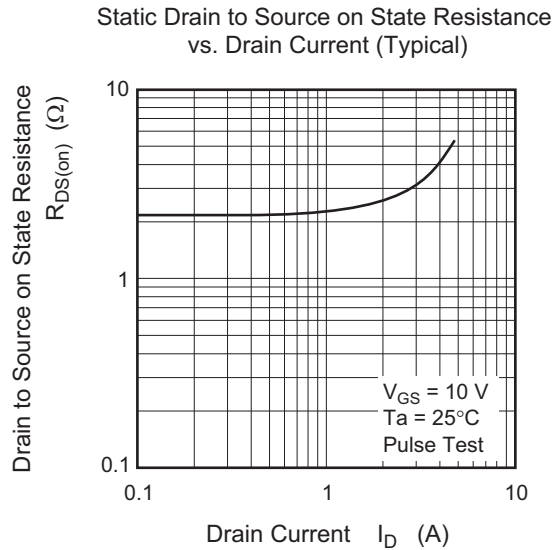
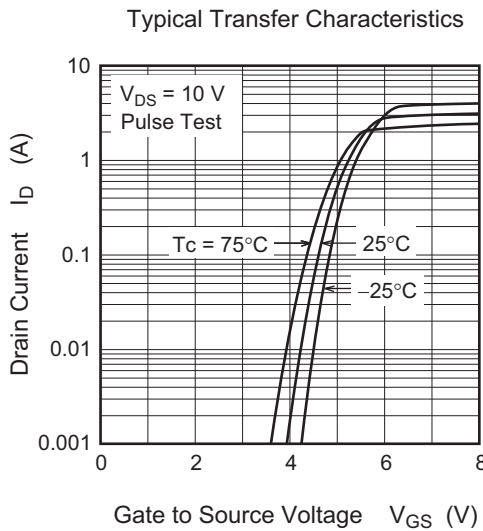
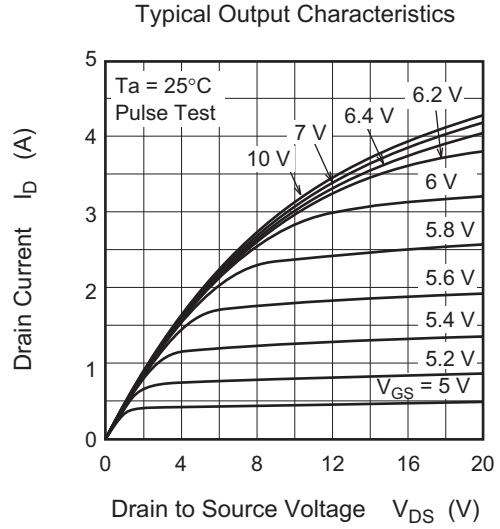
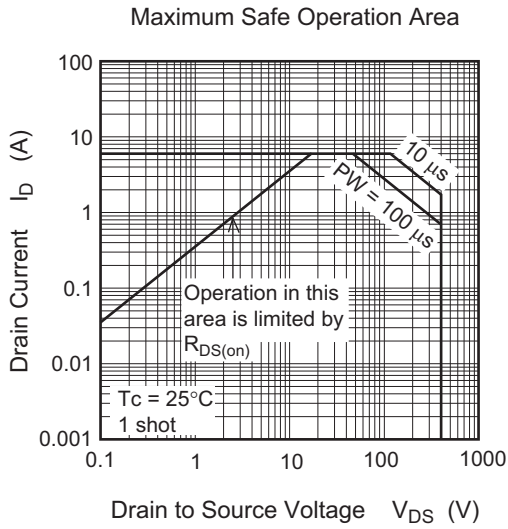
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	400	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 400 \text{ V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 30 \text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.5	—	4.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	2.4	2.9	$\Omega$	$I_D = 1.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note 5</sup>
Input capacitance	$C_{iss}$	—	165	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	$C_{oss}$	—	25	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	2.6	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$I_D = 1.5 \text{ A}$
Rise time	$t_r$	—	12	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	23	—	ns	$R_L = 133 \Omega$
Fall time	$t_f$	—	20	—	ns	$R_g = 10 \Omega$
Total gate charge	$Q_g$	—	6.0	—	nC	$V_{DD} = 320 \text{ V}$
Gate to source charge	$Q_{gs}$	—	1.2	—	nC	$V_{DS} = 100 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	3.4	—	nC	$I_D = 3 \text{ A}$
Body-drain diode forward voltage	$V_{DF}$	—	0.9	1.5	V	$I_F = 3 \text{ A}$ , $V_{GS} = 0$ <sup>Note 5</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	200	—	ns	$I_F = 3 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

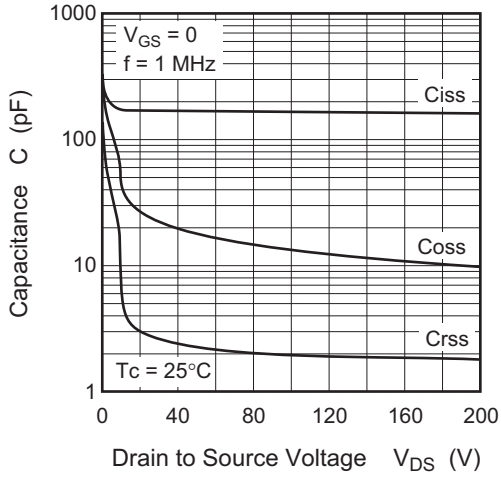
Note: 5. Pulse test

6. Since this device is equipped with high voltage FET chip ( $V_{DSS} \geq 400 \text{ V}$ ), high voltage may be supplied. Therefore, please be sure to confirm about electric discharge between drain terminal and other terminal.
7. This device is sensitive to electrostatic discharge. It is recommended to adopt appropriate cautions when handling this product.

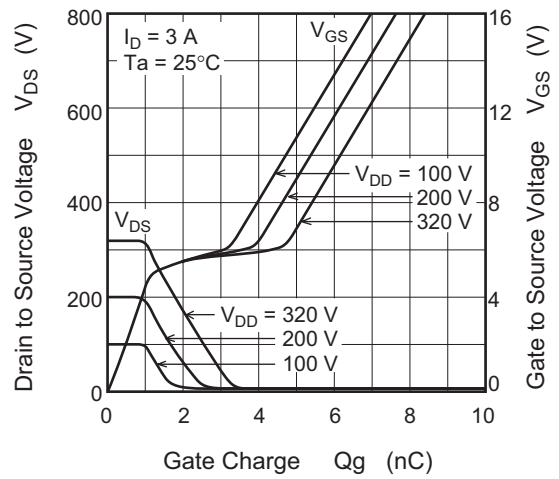
Main Characteristics



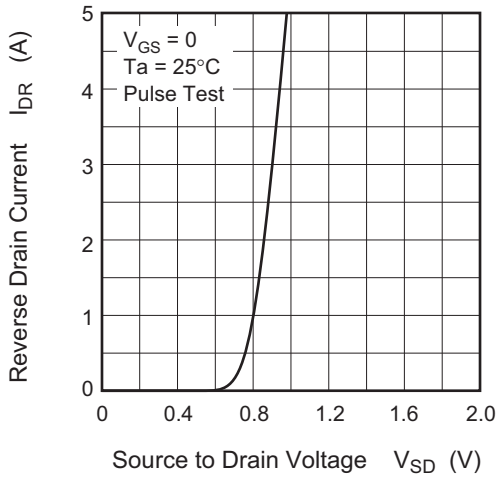
Typical Capacitance vs. Drain to Source Voltage



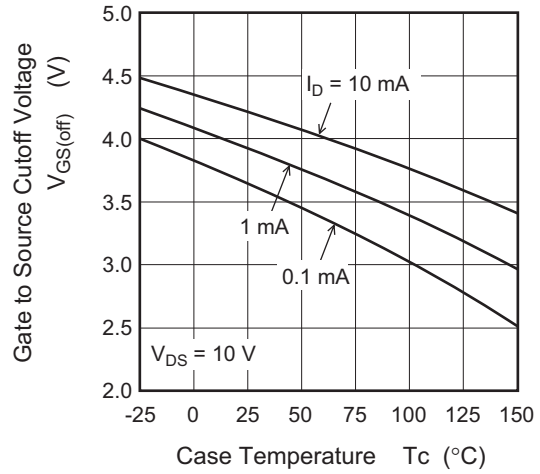
Dynamic Input Characteristics (Typical)



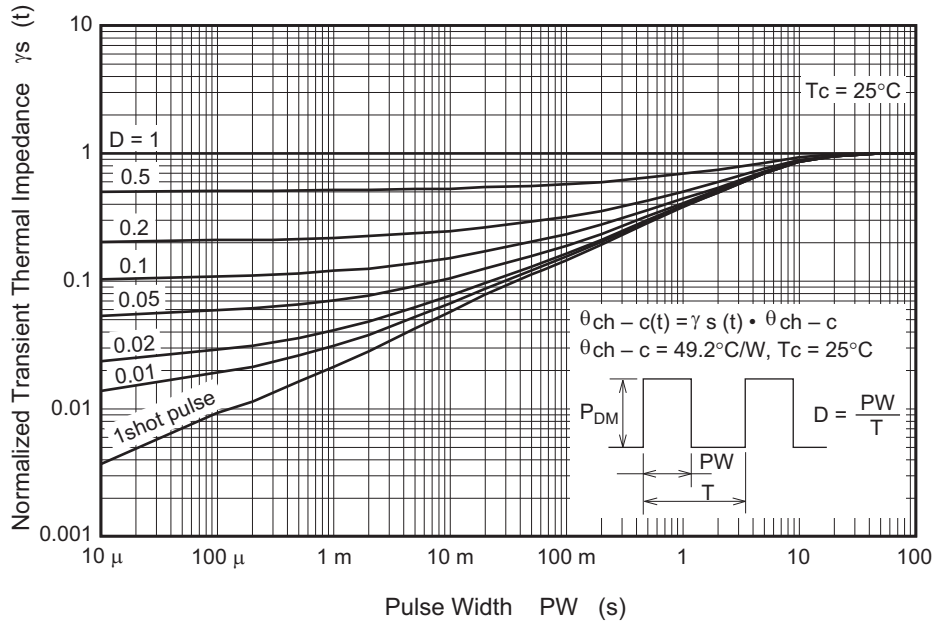
Reverse Drain Current vs. Source to Drain Voltage (Typical)



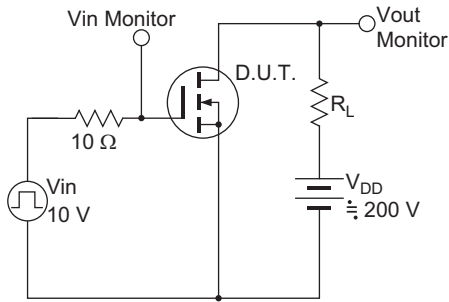
Gate to Source Cutoff Voltage vs. Case Temperature (Typical)



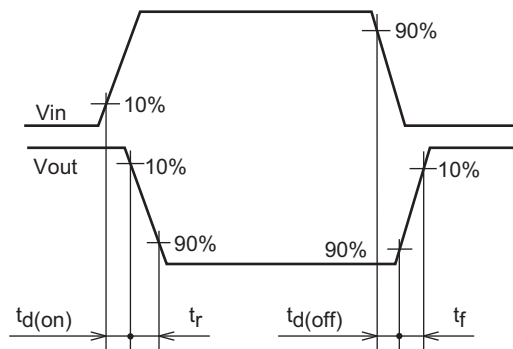
Normalized Transient Thermal Impedance vs. Pulse Width



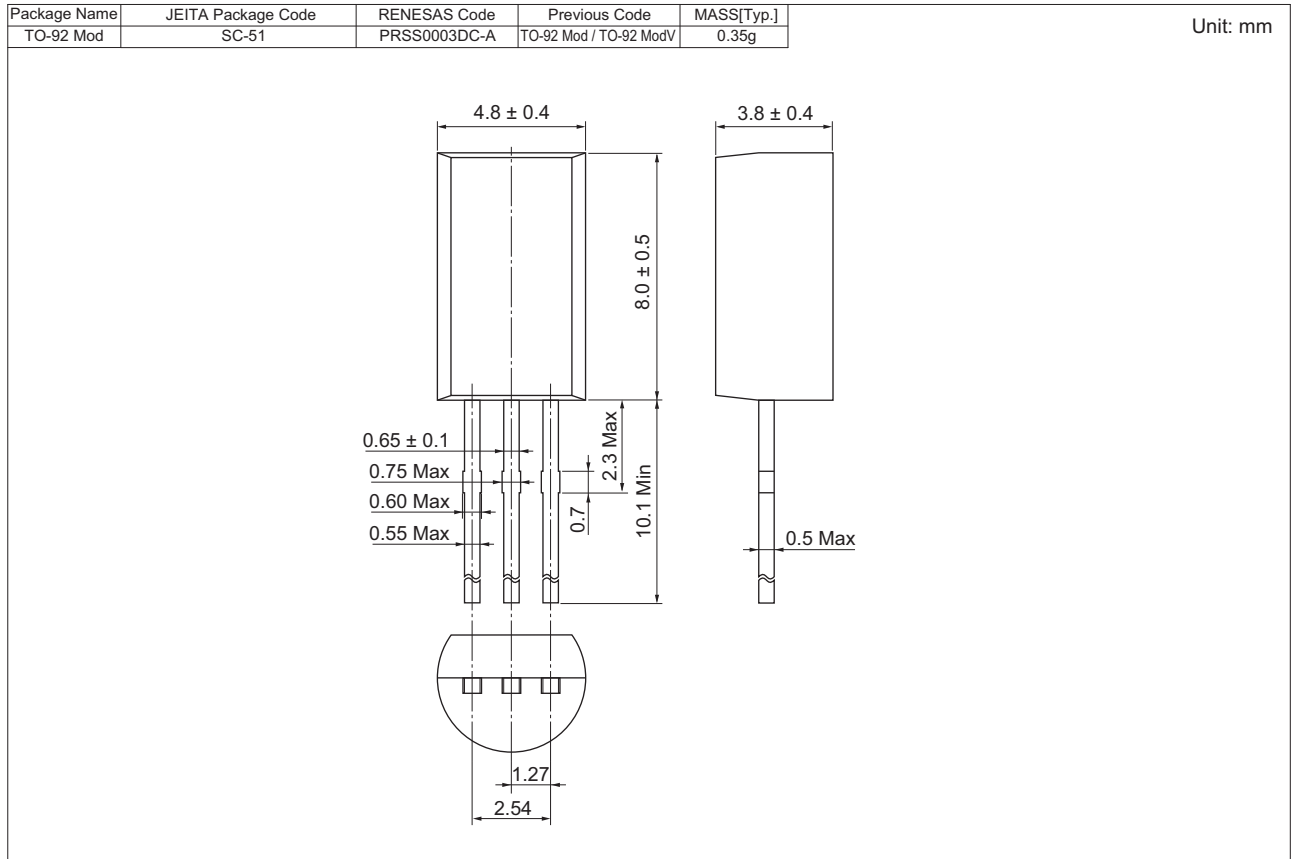
Switching Time Test Circuit



Waveform



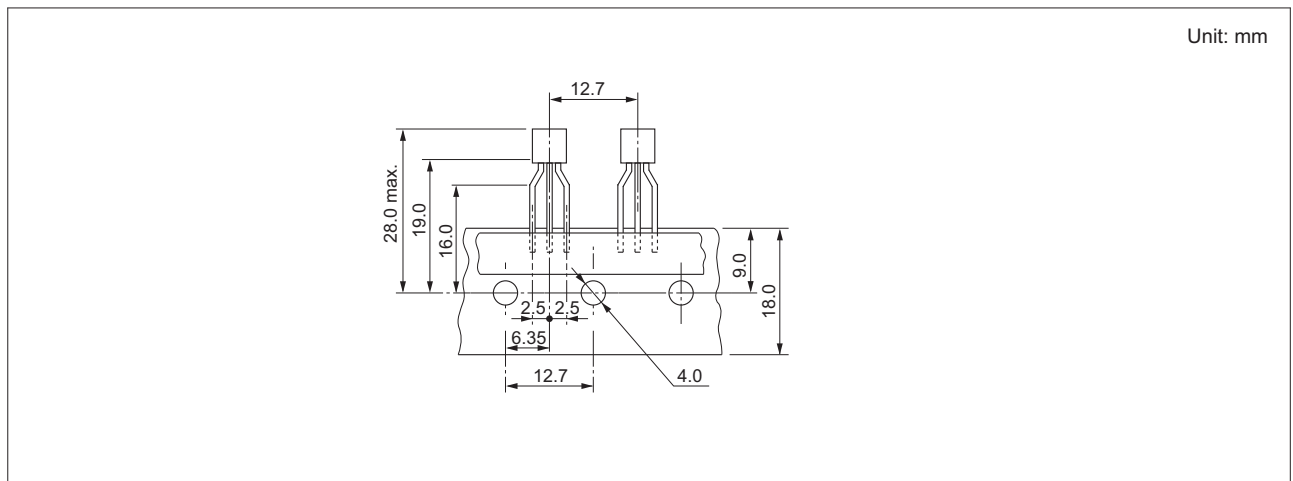
### Package Dimensions



### Ordering Information

Orderable Part No.	Quantity	Shipping Container
RJK4002DJE-00#Z0	2500 pcs	Hold Box, Radial Taping

Note: Leads is forming applied as following figure.



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