

# RJK4006DPD

Silicon N Channel MOS FET  
High Speed Power Switching

REJ03G1547-0100

Rev.1.00

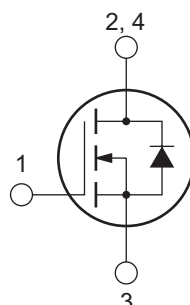
Dec 19, 2008

## Features

- Low on-resistance
- Low leakage current
- High speed switching

## Outline

RENESAS Package code: PRSS0004ZG-A  
(Package name : MP-3A)



1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	400	V
Gate to source voltage	$V_{GSS}$	$\pm 30$	V
Drain current	$I_D$ <sup>Note4</sup>	8	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	24	A
Body-drain diode reverse drain current	$I_{DR}$	8	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ <sup>Note1</sup>	24	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	8	A
Avalanche energy	$E_{AR}$ <sup>Note3</sup>	3.7	mJ
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	65	W
Channel to case thermal impedance	$\theta_{ch-c}$	1.92	$^\circ\text{C}/\text{W}$
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

- Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$   
 2. Value at  $T_c = 25^\circ\text{C}$   
 3.  $ST_{ch} = 25^\circ\text{C}$ ,  $T_{ch} \leq 150^\circ\text{C}$   
 4. Limited by maximum safe operation area

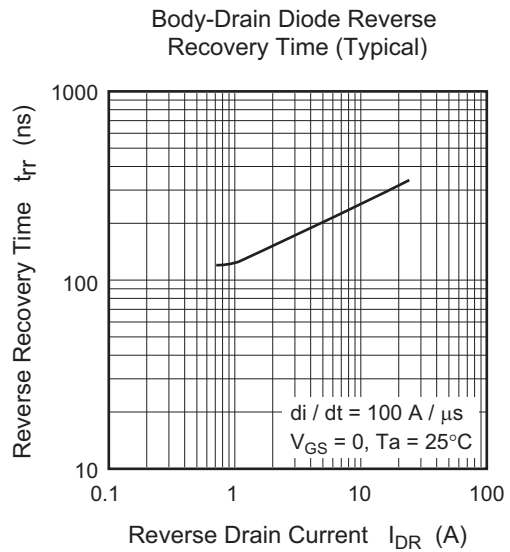
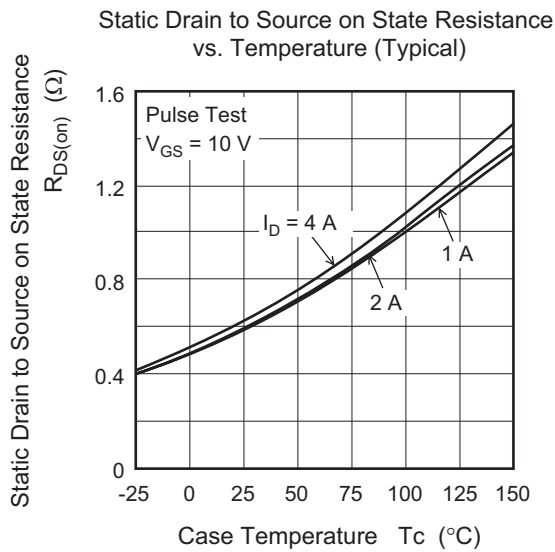
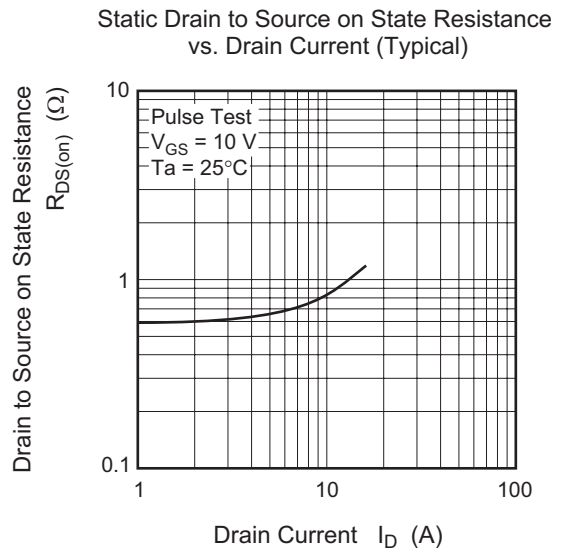
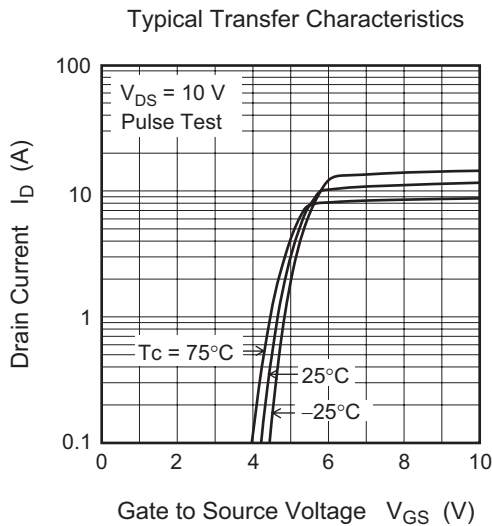
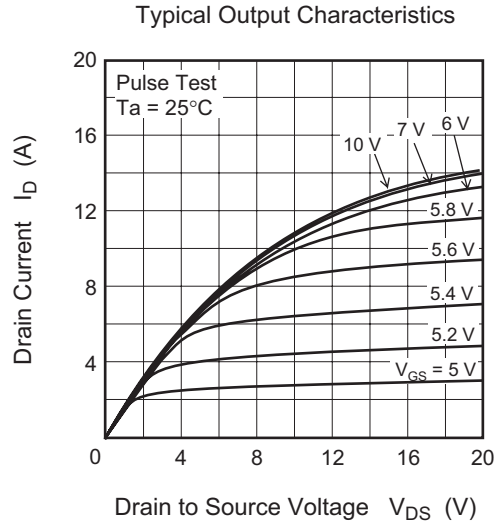
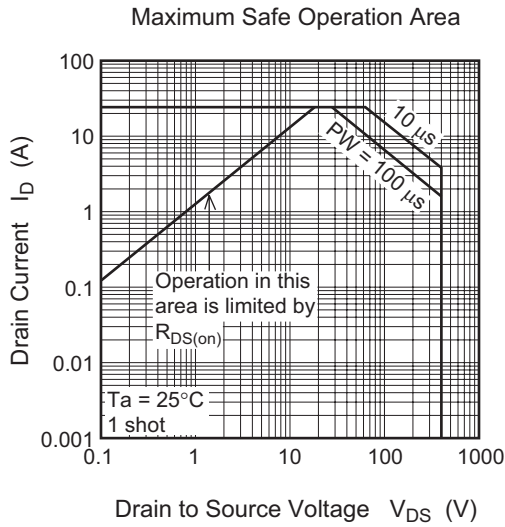
## Electrical Characteristics

(Ta = 25°C)

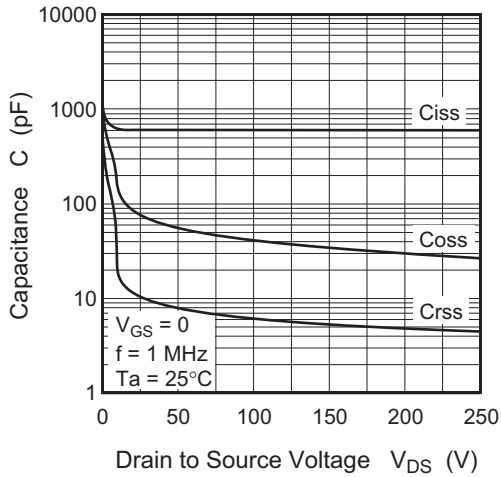
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	400	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 400 \text{ V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 30 \text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.69	0.80	$\Omega$	$I_D = 4 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note5</sup>
Input capacitance	$C_{iss}$	—	620	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	$C_{oss}$	—	80	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	11	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$I_D = 4 \text{ A}$
Rise time	$t_r$	—	30	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	60	—	ns	$R_L = 50 \Omega$
Fall time	$t_f$	—	20	—	ns	$R_g = 10 \Omega$
Total gate charge	$Q_g$	—	20	—	nC	$V_{DD} = 320 \text{ V}$
Gate to source charge	$Q_{gs}$	—	4	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	9	—	nC	$I_D = 8 \text{ A}$
Body-drain diode forward voltage	$V_{DF}$	—	0.9	1.5	V	$I_F = 8 \text{ A}$ , $V_{GS} = 0$ <sup>Note5</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	230	—	ns	$I_F = 8 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 5. Pulse test

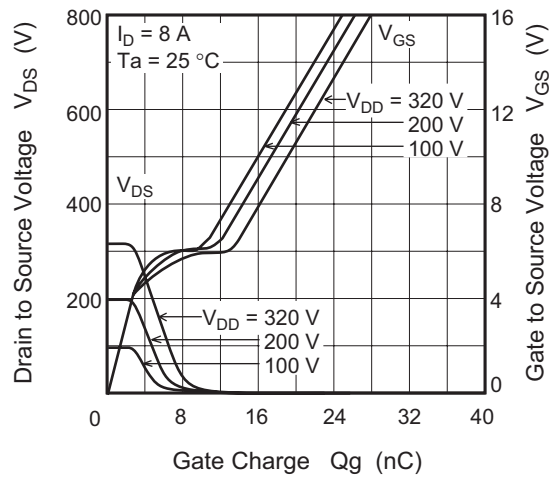
Main Characteristics



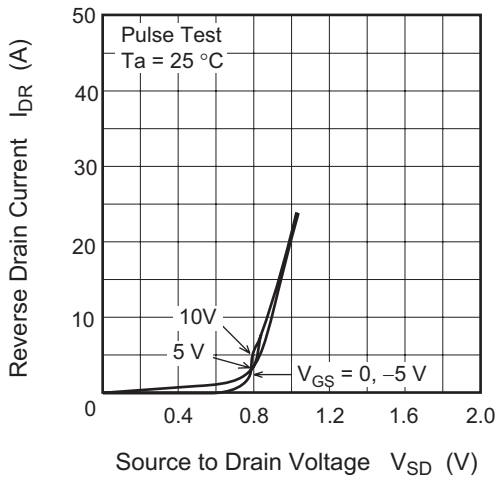
Typical Capacitance vs. Drain to Source Voltage (Typical)



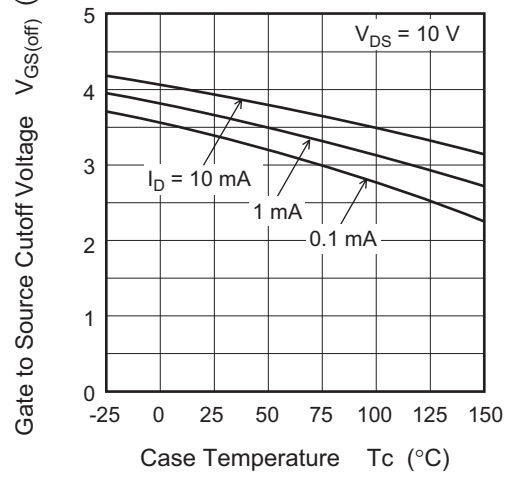
Dynamic Input Characteristics (Typical)



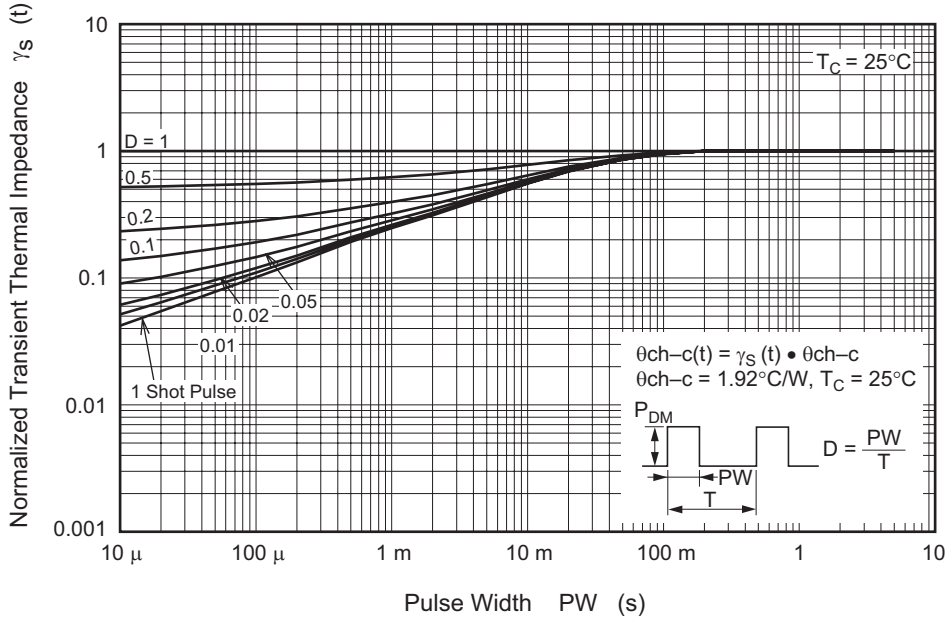
Reverse Drain Current vs. Source to Drain Voltage (Typical)



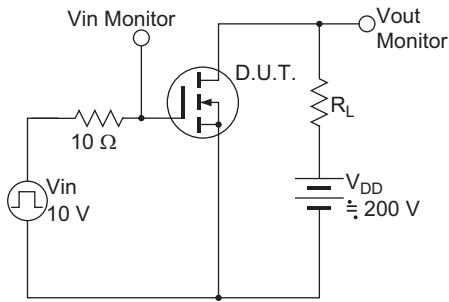
Gate to Source Cutoff Voltage vs. Case Temperature (Typical)



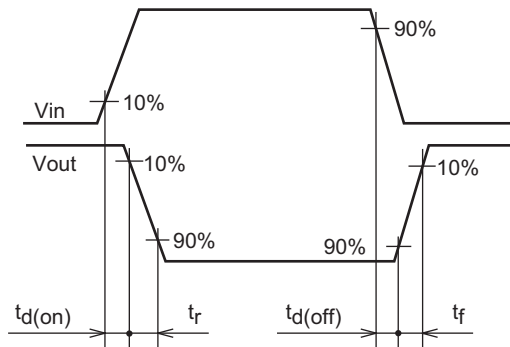
Normalized Transient Thermal Impedance vs. Pulse Width



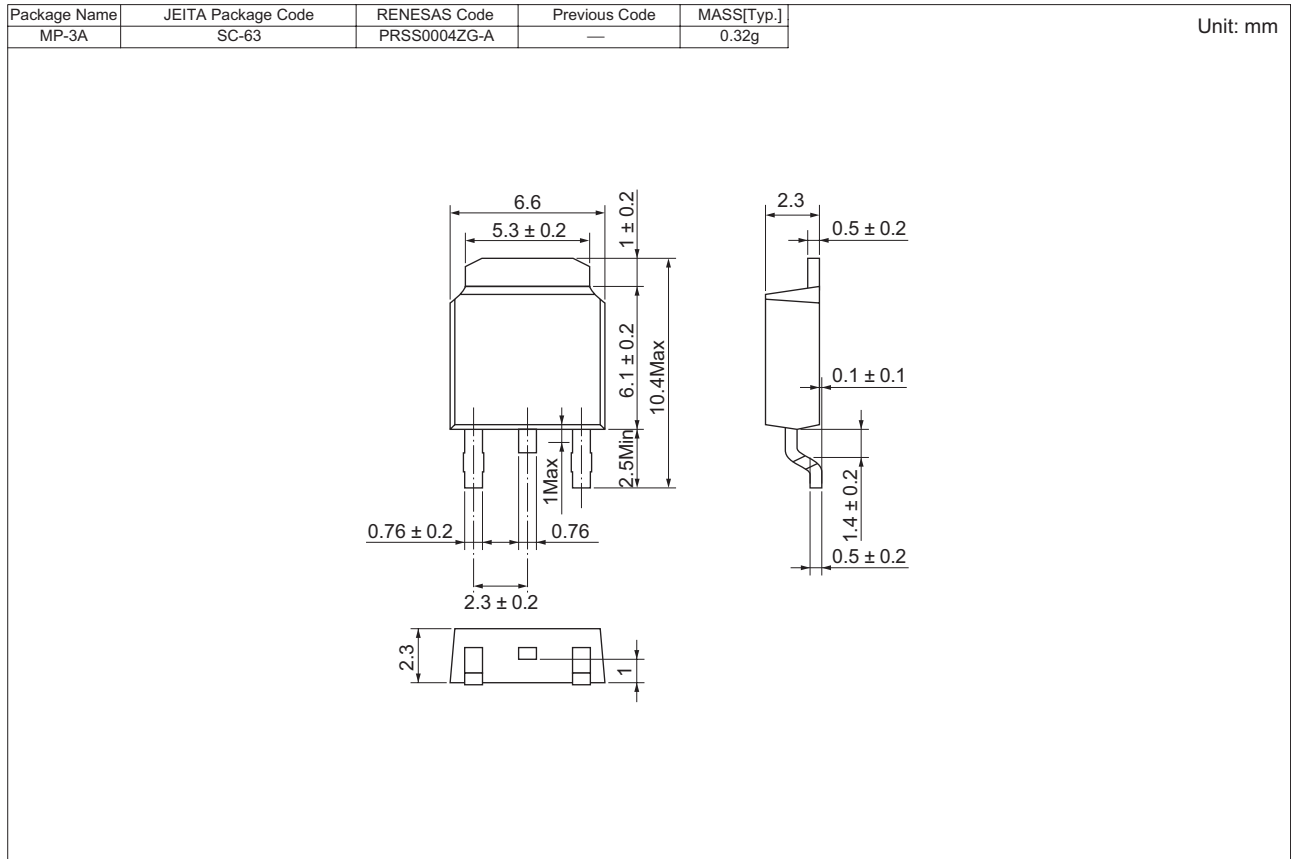
Switching Time Test Circuit



Waveform



### Package Dimensions



### Ordering Information

Part No.	Quantity	Shipping Container
RJK4006DPD-00-J2	3000 pcs	Taping

Notes:

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