

RJK5013DPE

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1488-0200

Rev.2.00

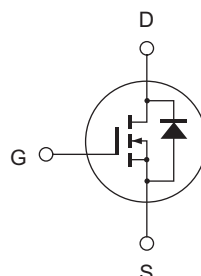
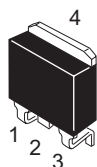
Nov 29, 2006

Features

- Low on-resistance
- Low leakage current
- High speed switching

Outline

RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK(S)-(1))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	14	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	42	A
Body-drain diode reverse drain current	I_{DR}	14	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note1}	42	A
Avalanche current	I_{AP} ^{Note3}	4	A
Avalanche energy	E_{AR} ^{Note3}	0.88	mJ
Channel dissipation	P_{ch} ^{Note2}	100	W
Channel to case thermal impedance	θ_{ch-c}	1.25	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. Value at $T_c = 25^\circ C$

3. $STch = 25^\circ C$, $T_{ch} \leq 150^\circ C$

Electrical Characteristics

(Ta = 25°C)

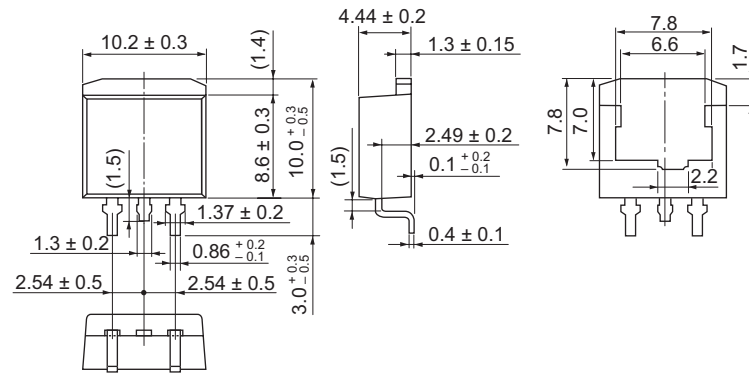
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.385	0.465	Ω	$I_D = 7 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1450	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	155	—	pF	
Reverse transfer capacitance	C_{rss}	—	19	—	pF	
Turn-on delay time	$t_{d(on)}$	—	34	—	ns	$I_D = 7 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 35.7 \Omega$ $R_g = 10 \Omega$
Rise time	t_r	—	24	—	ns	
Turn-off delay time	$t_{d(off)}$	—	86	—	ns	
Fall time	t_f	—	16	—	ns	
Total gate charge	Q_g	—	38	—	nC	$V_{DD} = 400 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 14 \text{ A}$
Gate to source charge	Q_{gs}	—	8	—	nC	
Gate to drain charge	Q_{gd}	—	17	—	nC	
Body-drain diode forward voltage	V_{DF}	—	0.9	1.5	V	$I_F = 14 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	310	—	ns	$I_F = 14 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBAK(S)-(1)	SC-83	PRSS0004AE-B	LDBAK(S)-(1) / LDBAK(S)-(1)V	1.30g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
RJK5013DPE-00-J3	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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