PRODUCT DATA SHEET

RK2710

PRELIMINARY

Revision A1.0
Sep, 2008

Release Note

Document Version Information

Product Version Information	
Product Name	RK2710
Version Number	A1.0
Previous Version	
Release Date	Sep,26,2007

Document History

Version Number	Release Date	Change Notes
A 1.0	Sept,26,2008	First release

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Product Overview

1.1 Overview

The RK2710 is an integrated system-on-chip with Dual Core architecture, which will focus on portable DAB, DVB-T solution with multimedia player. The Dual-Core architecture integrated ARM7EJC and DSP micro processor and by co-operating of those two CPUs, RK27xx can get high performance on Low-Power platform.

The RK2710 solution is base on RK27xx PMP solution, also add DAB demodulator architecture and DVB-T decoder.

Features

- **System Operation**
  - Dual Core Architecture (ARM7EJC+DSP)
  - Support system boot sequentially from ARM7EJC to DSP
  - Selectable JTAG debug method
  - Selectable booting method
    - Boot from NOR Flash
    - Boot from Embedded ROM
  - Internal memory space
    - DSP IMEM 32Kwords
    - DSP DMEM 32Kwords
    - ARM7EJC Embedded Sync SRAM 4Kbytes
    - ARM7EJC Embedded Boot ROM 8Kbytes

- **Clock & Power Management**
  - Use two crystal oscillator (24MHz/32.768KHz)
  - Use three PLL (For ARM/DSP/CODEC+HSADC)
  - Support different AHB Bus and ARM7EJC clock ratio
    - 1:1 and 1:2 mode
  - Max frequency of every domain

    RK2710-G
    - ARM7EJC 266MHz (default 12MHz)
    - AHB BUS 133MHz (default 12MHz)
    - APB BUS 133MHz (default 12MHz)
    - DSP 176MHz (default 24MHz)

    RK2710-M
    - ARM7EJC 300MHz (default 12MHz)
    - AHB BUS 166MHz (default 12MHz)
    - APB BUS 133MHz (default 12MHz)
    - DSP 176MHz (default 24MHz)

  - Power management mode
    - Normal, slow, idle, stop, and power-off mode

- **Processor**
  - ARM7EJC
    - Max frequency 200MHz / 300MHz
    - ARMv5TE architecture with Jazella technology
    - 8x Java performance improvement
    - Five-stage pipeline
    - DSP extensions with 32x16 MAC
    - Small, cost-effective, processor macro cell
    - Unified Cache architecture , Size is 16KB(8words/line)
    - Two way configurable write-through cache
  - DSP

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- RISC-based four-way superscalar architecture
- Eight-stage pipeline
- Support 4GB address space

- Dual-Core communication unit
  - Support dual cores system
  - Mailbox handshaking with interrupt mechanism
    - Support two AHB slave ports
    - Each mailbox element includes one data word register, one command word register, and one flag bit that can represent one interrupt
    - 4 interrupts to Host Interrupt Controller
    - 4 interrupts to Client Interrupt Controller

- **Memory controller**
  - Static/SDRAM Memory controller
    - Dynamic memory interface support
    - Asynchronous static memory device support including SRAM, ROM and Flash with or without asynchronous page mode
    - Support 1 independent AHB slave port for control register, and up to 2 individual AHB slave port for data access
    - Support 1 chip selects for SDRAM and 2 chip selects for static memory
    - support 16-bit wide SDRAM and 8-bit or 16-bit wide static memory
    - Support industrial standard SDRAM from 16MBytes to 128MBytes devices
    - 16Mbytes access space per static memory support
  - Embed 8x16 low power SDRAM (RK2710-M only)
  - NAND Flash controller
    - Support 4 chip selects for NAND flash
    - support 8-bit wide data
    - Flexible CPU interface support
    - Embedded buffer to improve performance
    - Support internal DMA transfer from/to flash
    - 512bytes、2Kbytes、4Kbytes page size support
    - Hardware ECC
  - SD controller
    - Compliant with SD spec. Version 2.00 except SPI mode
    - Compliant with Multimedia Card system specification V3.3 except SPI mode, Stream R/W mode and I/O (Interrupt) mode
    - Variable SD/MMC card clock rate 0 – 25 MHz which depends on APB clock frequency
    - Controllable SD/MMC card clock to save power consumption
    - Support MMU ping-pong structure to enhance the SD/MMC data transfer performance
    - Support DMA transfer

- **High speed ADC interface**
  - Support 8/10 bits HS ADC transfer

- **DVB-T / DVB-C TS interface**
  - Support MPEG-2 TS interface
  - Compliant with DVB-T standard ETS 300 744
  - Full frequency range from 174 to 858 MHz
  - Support EPG (Electronic Program Guide)
  - Support up to 720*576 with 25 frames
  - Support Auto-Scan and full channel Scan
  - Total system Power consumption: 1.4W (with 3.5 inch TFT LCD)

- **DAB Demodulator and Audio Decoder**
  - Support of DAB+ Audio Operation;
  - Support of Recording to files.
  - Support of 120km/h Mobile Receiving

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- Display for Ensemble label、Programme service label and Data service label
- Manual /Auto-Scan;150 Broadcasting Station Saved

- **LCD controller**
  - Support video data input format
    - 24bit RGB
    - 16bit RGB
    - YUV 4:2:2
    - YUV 4:2:0
  - Support serial 8bit RGB LCD panel with dummy data or not
  - Support Parallel 24bit (max) RGB LCD panel
  - Built-in 2 640x32bit buffer
  - Support DMA transfer
- **DMA Controller**
  - 3 DMA Controller on-chip
  - AHB DMA (HDMA)
    - Integrated in AHB BUS0
    - Two DMA channels support
    - 8 hardware request handshaking support
    - Built-in 32x16 data FIFO
    - Support hardware and software trigger DMA transfer mode
  - AHB-to-AHB Bridge (A2A)
    - Integrated between AHB BUS0 and AHB BUS1
    - Provide AHB-to-AHB bus protocol translation
    - Support AHB-to-AHB DMA or Single AHB DMA
    - Two DMA Channels support
    - On-the-fly mode between two level bus support
    - 4 hardware request handshaking support
    - Support hardware and software trigger DMA transfer mode
  - DW DMA
    - Integrated in AHB BUS1
    - Four DMA Channels support
    - 8 hardware request handshaking support
    - Support hardware and software trigger DMA transfer mode
    - Build-in 4 data FIFO : 64bytes/64bytes/64bytes/64bytes
    - Scatter/Gather transfer support
    - LLP transfer support
    - Two master for on-the-fly support
- **USB interface**
  - UHC(USB HOST Controller) and UDC(USB DEV Controller) share PHY
  - Only support UHC or UDC work at the same time
  - USB2.0 Host Controller
    - USB 2.0 high speed host controller and specification compliant
    - Intel™ EHCI host controller interface specification compliant
    - OHCI host controller interface specification compliant
    - Supports USB Transceiver Macro cell Interface+ (UTMI+ level 3)
  - USB2.0 Device Controller
    - Complies with the Universal Serial Bus specification Rev. 2.0, Supports USB Full Speed (12Mb/sec) and High Speed (480 Mb/sec), is Backward compatible with USB1.1
    - On-chip USB2.0 PHY and Parallel Bus Interface Engine (PIE)
    - Suspend / Resume operation - Supports USB remote wake-up

- **Low_speed Peripheral interface**
  - Serial Peripheral Interface (SPI) Master Controller
    - Four transfer protocols available with selectable clock polarity and clock phase
    - Different bit rates available for SCLK

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- Bi-direction mode
- UART (16550)
  - 2 UART support
  - UART0 support modem function
  - Supports up to 3Mbps baud-rate
  - Programmable baud rate generator. This enables division of the internal clock by (1 ~ 65535 x 16) and generates an internal x16 clock
  - Standard asynchronous communication bits (start, stop and parity).
- I2C controller
  - Multi masters operation
  - Software programmable clock frequency and transfer rate up to 400Kbit/sec
  - Supports 7 bits and 10 bits addressing modes
- I2S
  - Support mono/stereo audio file
  - Support audio resolution: 8, 16 bits
  - Support audio sample rate from 32 to 96 KHz
  - Support I2S, Left-Justified, Right-Justified digital serial audio data interface
- PWM
  - Built-in three 32 bit timer modulers
  - Programmable counter
  - Chained timer for long period purpose
  - 4-channel 32-bit timer with Pulse Width Modulation (PWM)
  - Programmable duty-cycle, and frequency output
- General Purpose IO (GPIO)
  - Support 48 individually programmable input/output pins
  - Support GPIO with interrupt capability
- Timers
  - Built-in three 32 bits timer modules
  - Programmable counter
- Watchdog Timer (WDT)
  - Watchdog function
  - Built-in 32 bits programmable reset counter

- Analog IP interface
  - ADC Converter
    - 4-channel single-ended 10-bit 1MSPS Successive Approximation Register (SAR) analog-to-digital converter
    - Supply 2.5V to 3.6V for analog and 0.9V to 1.3V for digital interface
    - Very Low Power : <0.4mW power consumption at 1MSPS
  - CODEC
    - Support built-in codec or external codec through I2S interface
    - Build in Stereo 24-bit Delta-Sigma DAC with on-chip headphone amplifier
    - Build in Stereo 16-bit Sigma-Delta ADC

- **Operation Frequency**
  - ARM7: up to 200MHz
  - DSP : up to 176MHz
  - AMBA AHB bus: up to 133 MHz
  - AMBA APB bus: up to 66 MHz

- **Package**
  - RK2710-G BGA169
  - RK2710-M BGA169

- **Operation Temperature Range**
  - 0°C to +125°C

- **Operation Voltage Range**
  - Core: 1.25 V

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- I/O : 3.0 - 3.3V

- **DAB Demodulator and Audio Decoder**
  - Support of DAB+ Audio Operation;
  - Support of Recording to files.
  - Support of 120km/h Mobile Receiving
  - Display for Ensemble label、Programme service label and Data service label
  - Manual /Auto-Scan;150 Broadcasting Station Saved
  - Support of all DAB transmission modes (I, II, III, and IV)
  - Automatic mode detection and frame synchronization
  - Support of dynamic multiplex re-configuration
  - Support of Signal intensity Indication

1.3 Pin Description

1.3.3 RK2710-G PIN Description

RK2710-G BGA169	Pad NAME	Direction	PIN Description
A1	NPOR	I Pull up	Power on Reset
B2	XIN27M	I PullDown	External wakeup ARM7 from stop mode
C3	SDT_A6	O	SDRAM/SRAM addr[6]
B1	SDT_A5	O	SDRAM/SRAM addr[5]
C2	SDT_A4	O	SDRAM/SRAM addr[4]
D3	SDT_A3	O	SDRAM/SRAM addr[3]
C1	SDT_A2	O	SDRAM/SRAM addr[2]
D2	SDT_A1	O	SDRAM/SRAM addr[1]
E4	SDT_A0	O	SDRAM/SRAM addr[0]
D1	LCD_D0	O	lcd data[0]
E3	LCD_D1	O	lcd data[1]
F5	LCD_D2	O	lcd data[2]
E1	LCD_D3	O	lcd data[3]
E2	VDDIO	P	IO POWER SUPPLY 3.3V
F3	VSSIO	P	IO GROUND
F2	VSSD	P	CORE GROUND
G2	VSSD		
F1	XIN24M	I OSC	Crystal 24M input
G1	XOUT24M	O OSC	Crystal 24M output
H2	VDDD	P	CORE POWER SUPPLY 1.2V
H3	VDDD		
F4	LCD_D4	O	lcd data[4]
G6	LCD_D5	O	lcd data[5]
G5	LCD_D6	O	lcd data[6]
G4	LCD_D7	O	lcd data[7]
G3	PE0/LCD_D8	IO Pull up/O	GPIO E0/LCD data[8]
H1	PE1/LCD_D9	IO Pull up/O	GPIO E1/LCD data[9]
H4	PE2/LCD_D10	IO Pull up/O	GPIO E2/LCD data[10]
H5	PE3/LCD_D11	IO Pull up/O	GPIO E3/LCD data[11]
J2	PE4/LCD_D12	IO Pull up/O	GPIO E4/LCD data[12]
J1	PA3/LCD_D20/NRTS0	IO Pull up/O	GPIO A3/LCD data[20]/UART0 NRTS0
J3	PA2/LCD_D18/NCTS0	IO Pull up/O	GPIO A2/LCD data[18]/UART0 NCTS0

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J4	PE5/LCD_D13	IO Pull up/O	GPIO E5/LCD data[13]
K1	PE6/LCD_D14	IO Pull up/O	GPIO E6/LCD data[14]
K2	PE7/LCD_D15	IO Pull up/O	GPIO E7/LCD data[15]
K3	PA0/LCD_D16/RXD0	IO Pull up/O/O	GPIO A1/LCD data[16]/UART0 rxd
K4	PA1/LCD_D17/TXD0	IO Pull up/O/O	GPIO A1/LCD data[17]/UART0 txd
L1	LCD_CLK	O	RGB dot clock / MUC pannel RS
L2	VIP_D0/HADC_D0	I pull up	HS adc data[0]
L3	VIP_D1/HADC_D1	I pull up	HS adc data[1]
M1	VIP_D2/HADC_D2	I pull up	HS adc data[2]
M2	VIP_D3/HADC_D3	I pull up	HS adc data[3]
N1	VIP_D4/HADC_D4	I pull up	VIP data[0]
N2	VIP_D5/HADC_D5	I pull up	VIP data[1]
M3	VIP_D6/HADC_D6	I pull up	VIP data[2]
L4	VIP_D7/HADC_D7	I pull up	VIP data[3]
K5	LCD_HSYNC	O	RGB HSYNC/MCU_WR
J5	PA7/LCD_VSYNC	IO Pull up/O	GPIO A7/RGB_VSYNC/MCU_CS
M4	FLASH_RDY	I pull up	NAND FLASH R/B
L5	FLASH_RDN	O	NAND FLASH RD
N3	FLASH_CS0	O	NAND FLASH CS0
N4	FLASH_D7	B	nand flash data[7]
M5	FLASH_D6	B	nand flash data[6]
H6	FLASH_D5	B	nand flash data[5]
J6	FLASH_D4	B	nand flash data[4]
N5	FLASH_D3	B	nand flash data[3]
K6	FLASH_D2	B	nand flash data[2]
H7	FLASH_D1	B	nand flash data[1]
J7	FLASH_D0	B	nand flash data[0]
N6	FLASH_CLE	O	nand flash cle
K7	FLASH_ALE	O	nand flash ale
N7	FLASH_WRN	O	NAND FLASH WR
M6	VDDD	P	CORE POWER SUPPLY 1.2V
L6	VDDD		
M7	VSSD	P	CORE GROUND
L7	VSSD		
M8	VSSIO	P	IO GROUND
L8	VDDIO	P	IO POWER SUPPLY 3.3V
N8	PB0/SDDATA1	IO Pull up/B/B	GPIO B0/SD DATA1
K8	PB1/SDDATA2	IO Pull up/B/B	GPIO B1/SD DATA2
J8	PB2/SDDATA0/SPI_MISO	IO Pull up/B/B	GPIO B2/SD DATA0/SPI_MISO
H8	PB3/SDCMD/SPI_MOSI	IO Pull up/B/B	GPIO B3/SD MD/SPI_MOSI
N9	PB4/SDDATA3/SPI_CSN	IO Pull up/B/B	GPIO B3/SD DATA3/SPI_CS
M9	PB5/SDCLK/SPI_CLK	IO Pull up/O/O	GPIO B3/SD CLK/SPI_CLK
L9	CODEC_AIL1	AI	L-channel analog input 1
K9	CODEC_AIR1	AI	R-channel analog input 1
J9	CODEC_MIC	AI	Mic input
N10	CODEC_VCOM	AO	Internal biasing voltage
M10	CODEC_VSSA	P	Ground for Codec
L10	CODEC_VDDA	P	Power supply for CODEC, 3.3V
K10	CODEC_AOHPL	AO	L-channel headphone output
N11	CODEC_VSSAO	P	Ground for amplifiers

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M11	CODEC_AOM	AO	common mode analog output
L11	CODEC_VDDAO	P	Power supply for amplifiers 3.3V
N12	CODEC_AOHPR	AO	R-channel headphone output
M12	CODEC_AOMS	AI	common mode sense input
N13	CODEC_HPSENSE	AI	Sense of jack insertion
M13	PA5/FLASH_CS1	IO Pull up/O	GPIO A5/FLASH CS1
L13	SDA/FLASH_CS3/PB7	IO Pull up/O/IO Pull up	SCL/NAND FLASH CS3/GPIO B7
L12	SCL/FLASH_CS2/PB6	IO Pull up/O/IO Pull up	SCL/NAND FLASH CS2/GPIO B6
K13	PC0	IO Pull down	GPIO C0
K12	PC1/LCD_DEN	IO Pull down/O	GPIO C1/RGB DEN
K11	PC2/I2S_SCLK	IO Pull down/B	GPIO C2/I2S SCLK
J13	PC3/I2S_LRCK	IO Pull down/B	GPIO C3/I2S LRCK
J12	PC4/I2S_SDI	IO Pull down/I	GPIO C4/I2S DATA IN
J11	PC5/I2S_SDO	IO Pull down/O	GPIO C5/I2S DATA OUT
J10	PC6/I2S_MCLK	IO Pull down/O	GPIO C6/I2S CLOCK OUT
H13	PC7/ST_CSN1	IO Pull up/O	GPIO C7/static memory CS1
H12	PF0/VIP_CLKO	IO pull up/O	GPIO F7/VIP clock out
H11	PD0/SDPCA/TXD1	IO Pull up/O/O	GPIO D0/SD Power control/Uart1 txd
H10	PD1/SDCDA/RXD1	IO Pull up/O/O	GPIO D1/SD detect/Uart1 rxd
H9	PD2/SDWPA	IO Pull up/I	GPIO D2/SD Card wirte protect
G13	PD3/SD_CKE	IO Pull up/O	GPIO D3/SDRAM CKE
G9	PD6/PWM2	IO Pull down/O	GPIO D6/PWM2
G10	PD5/PWM1	IO Pull down/O	GPIO D5/PWM1
G11	PD4/PWM0	IO /O	GPIO D4/PWM0
G12	VDDIO	P	IO POWER SUPPLY 3.3V
F11	VSSIO	P	IO GROUND
F12	VDDD	P	CORE POWER SUPPLY 1.2V
F9	SDT_D15	B	SDRAM/SRAM data[15]
F10	SDT_D14	B	SDRAM/SRAM data[14]
F13	SDT_D13	B	SDRAM/SRAM data[13]
E10	SDT_D12	B	SDRAM/SRAM data[12]
E11	SDT_D11	B	SDRAM/SRAM data[11]
E12	VBUS_DET	I Pull down	USB VBUS detect
E13	LADC_AIN0	A	10bit adc channel0 input
D11	LADC_AIN1	A	10bit adc channel1 input
D12	LADC_AIN2	A	10bit adc channel2 input
D13	LADC_VSSA	P	10bit adc analog ground
C13	PHY_VDDA	P	10bit adc analog power 2.7V -3.3V
B13	PHY_DN	A	USB DP
A13	PHY_DP	A	USB DN
A12	PHY_VSSA	P	USB PHY Analog Ground
B12	PHY_REF	A	Resistor for USB 6.04K 1%
C12	PHY_VDDP	P	USB PHY PLL POWER 1.2V
A11	PHY_VSSP	P	USB PHY PLL Ground
B11	TDO	O	JTAG TDO
C11	TMS	I PullUp	JTAG TMS
A10	TDI	I PullUp	JTAG TDI

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B10	TRST	I PullUp	JTAG TRST
C10	TCK	I PullUp	JTAG TCK
D10	RTCK	O	JTAG RTCK
A9	SDT_D10	B	SDRAM/SRAM data[10]
B9	SDT_D9	B	SDRAM/SRAM data[8]
C9	SDT_D8	B	SDRAM/SRAM data[8]
D9	SDT_D7	B	SDRAM/SRAM data[7]
E9	SDT_D6	B	SDRAM/SRAM data[6]
A8	SDT_D5	B	SDRAM/SRAM data[5]
D8	SDT_D4	B	SDRAM/SRAM data[4]
E8	SDT_D3	B	SDRAM/SRAM data[3]
F8	SDT_D2	B	SDRAM/SRAM data[2]
G8	SDT_D1	B	SDRAM/SRAM data[1]
D7	SDT_D0	B	SDRAM/SRAM data[0]
E7	SD_DQM1	O	SDRAM dqm[1]
F7	SD_DQM0	O	SDRAM dqm[0]
G7	SD_WEN	O	SDRAM wen
B8	VDDIO	P	IO POWER SUPPLY 3.3V
C8	VSSIO	P	IO GROUND
B7	VSSD	P	CORE GROUND
C7	VDDD	P	CORE POWER SUPPLY 1.2V
A7	SD_CASN	O	SDRAM casn
B6	SD_RASN	O	SDRAM rasn
A6	SD_CLK	O	SDRAM clkout
C6	SD_CSN	O	SDRAM csn
D6	SD_BA0	O	SDRAM ba[0]
E6	SD_BA1	O	SDRAM ba[1]
F6	SDT_A12/PF2	O/IO Pull up	SDRAM/SRAM addr[12]/GPIO F2
A5	SDT_A11/PF1	O/IO Pull up	SDRAM/SRAM addr[11]/GPIO F1
B5	SDT_A10	O	SDRAM/SRAM addr[10]
C5	SDT_A9	O	SDRAM/SRAM addr[9]
D5	SDT_A8	O	SDRAM/SRAM addr[8]
E5	SDT_A7	O	SDRAM/SRAM addr[7]
D4	TEST	I PullDown	Test mode
	VIP_PCLK	I pullup	VIP pclk
C4	VIP_VSYNC/HADC_D9	I pullup	VIP vsync
B4	VIP_HSYNC/HADC_D8	I pullup	VIP hsync
A4	HADC_CLK	O	hsadc clk output
A3	ZPLL_VDDA	P	DSP PLL power 1.2V
B3	PLL_VSSA	P	PLL Ground
A2	APLL_VDDA	P	ARM PLL power 1.2V

P	power supply pad
IO	IO pad
O	output pad
I	input pad
AI	analog input pad
AO	analgo output pad

PC5/PD0/PD1/PD2/PD3/PD5/PD6/PF0 can not using as input IO port, only can using as output port

B2 Pin is EWAKEUP PIN before June 2008.

UART1 only can using as TX mode, it can not receive data

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1.3.4 RK2710-M PIN Description

RK2710-M BGA169	Pad NAME	Direction	PIN Description
A1	NPOR	I Pull up	Power on Reset
B2	XIN27M	I PullDown	External wakeup ARM7 from stop mode
C3	NC	O	NC
B1	NC	O	NC
C2	NC	O	NC
D3	NC	O	NC
C1	NC	O	NC
D2	NC	O	NC
E4	NC	O	NC
D1	LCD_D0	O	lcd data[0]
E3	LCD_D1	O	lcd data[1]
F5	LCD_D2	O	lcd data[2]
E1	LCD_D3	O	lcd data[3]
E2	VDDIO	P	IO POWER SUPPLY 3.3V
F3	VSSIO	P	IO GROUND
F2	VSSD	P	CORE GROUND
G2	VSSD		
F1	XIN24M	I OSC	Crystal 24M input
G1	XOUT24M	O OSC	Crystal 24M output
H2	VDDD	P	CORE POWER SUPPLY 1.2V
H3	VDDD		
F4	LCD_D4	O	lcd data[4]
G6	LCD_D5	O	lcd data[5]
G5	LCD_D6	O	lcd data[6]
G4	LCD_D7	O	lcd data[7]
G3	PE0/LCD_D8	IO Pull up/O	GPIO E0/LCD data[8]
H1	PE1/LCD_D9	IO Pull up/O	GPIO E1/LCD data[9]
H4	PE2/LCD_D10	IO Pull up/O	GPIO E2/LCD data[10]
H5	PE3/LCD_D11	IO Pull up/O	GPIO E3/LCD data[11]
J2	PE4/LCD_D12	IO Pull up/O	GPIO E4/LCD data[12]
J1	PA3/LCD_D20/NRTS0	IO Pull up/O	GPIO A3/LCD data[20]/UART0 NRTS0
J3	PA2/LCD_D18/NCTS0	IO Pull up/O	GPIO A2/LCD data[18]/UART0 NCTS0
J4	PE5/LCD_D13	IO Pull up/O	GPIO E5/LCD data[13]
K1	PE6/LCD_D14	IO Pull up/O	GPIO E6/LCD data[14]
K2	PE7/LCD_D15	IO Pull up/O	GPIO E7/LCD data[15]
K3	PA0/LCD_D16/RXD0	IO Pull up/O/O	GPIO A1/LCD data[16]/UART0 rxd
K4	PA1/LCD_D17/TXD0	IO Pull up/O/O	GPIO A1/LCD data[17]/UART0 txd
L1	LCD_CLK	O	RGB dot clock / MUC pannel RS
L2	VIP_D0/HADC_D0	I pull up	HS adc data[0]
L3	VIP_D1/HADC_D1	I pull up	HS adc data[1]
M1	VIP_D2/HADC_D2	I pull up	HS adc data[2]
M2	VIP_D3/HADC_D3	I pull up	HS adc data[3]
N1	VIP_D4/HADC_D4	I pull up	VIP data[0]
N2	VIP_D5/HADC_D5	I pull up	VIP data[1]

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M3	VIP_D6/HADC_D6	I pull up	VIP data[2]
L4	VIP_D7/HADC_D7	I pull up	VIP data[3]
K5	LCD_HSYNC	O	RGB HSYNC/MCU_WR
J5	PA7/LCD_VSYNC	IO Pull up/O	GPIO A7/RGB_VSYNC/MCU_CS
M4	FLASH_RDY	I pull up	NAND FLASH R/B
L5	FLASH_RDN	O	NAND FLASH RD
N3	FLASH_CS0	O	NAND FLASH CS0
N4	FLASH_D7	B	nand flash data[7]
M5	FLASH_D6	B	nand flash data[6]
H6	FLASH_D5	B	nand flash data[5]
J6	FLASH_D4	B	nand flash data[4]
N5	FLASH_D3	B	nand flash data[3]
K6	FLASH_D2	B	nand flash data[2]
H7	FLASH_D1	B	nand flash data[1]
J7	FLASH_D0	B	nand flash data[0]
N6	FLASH_CLE	O	nand flash cle
K7	FLASH_ALE	O	nand flash ale
N7	FLASH_WRN	O	NAND FLASH WR
M6	VDDD	P	CORE POWER SUPPLY 1.2V
L6	VDDD		
M7	VSSD	P	CORE GROUND
L7	VSSD		
M8	VSSIO	P	IO GROUND
L8	VDDIO	P	IO POWER SUPPLY 3.3V
N8	PB0/SDDATA1	IO Pull up/B/B	GPIO B0/SD DATA1
K8	PB1/SDDATA2	IO Pull up/B/B	GPIO B1/SD DATA2
J8	PB2/SDDATA0/SPI_MISO	IO Pull up/B/B	GPIO B2/SD DATA0/SPI_MISO
H8	PB3/SDCMD/SPI_MOSI	IO Pull up/B/B	GPIO B3/SD MD/SPI_MOSI
N9	PB4/SDDATA3/SPI_CSN	IO Pull up/B/B	GPIO B3/SD DATA3/SPI_CS
M9	PB5/SDCLK/SPI_CLK	IO Pull up/O/O	GPIO B3/SD CLK/SPI_CLK
L9	CODEC_AIL1	AI	L-channel analog input 1
K9	CODEC_AIR1	AI	R-channel analog input 1
J9	CODEC_MIC	AI	Mic input
N10	CODEC_VCOM	AO	Internal biasing voltage
M10	CODEC_VSSA	P	Ground for Codec
L10	CODEC_VDDA	P	Power supply for CODEC, 3.3V
K10	CODEC_AOHPL	AO	L-channel headphone output
N11	CODEC_VSSAO	P	Ground for amplifiers
M11	CODEC_AOM	AO	common mode analog output
L11	CODEC_VDDAO	P	Power supply for amplifiers 3.3V
N12	CODEC_AOHPR	AO	R-channel headphone output
M12	CODEC_AOMS	AI	common mode sense input
N13	CODEC_HPSENSE	AI	Sense of jack insertion
M13	PA5/FLASH_CS1	IO Pull up/O	GPIO A5/FLASH CS1
L13	SDA/FLASH_CS3/PB7	IO Pull up/O/IO Pull up	SCL/NAND FLASH CS3/GPIO B7
L12	SCL/FLASH_CS2/PB6	IO Pull up/O/IO Pull up	SCL/NAND FLASH CS2/GPIO B6
K13	PC0	IO Pull down	GPIO C0
K12	PC1/LCD_DEN	IO Pull down/O	GPIO C1/RGB DEN
K11	PC2/I2S_SCLK	IO Pull down/B	GPIO C2/I2S SCLK
J13	PC3/I2S_LRCK	IO Pull down/B	GPIO C3/I2S LRCK

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J12	PC4/I2S_SDI	IO Pull down/I	GPIO C4/I2S DATA IN
J11	PC5/I2S_SDO	IO Pull down/O	GPIO C5/I2S DATA OUT
J10	PC6/I2S_MCLK	IO Pull down/O	GPIO C6/I2S CLOCK OUT
H13	PC7/ST_CSN1	IO Pull up/O	GPIO C7/static memory CS1
H12	PF0/VIP_CLKO	IO pull up/O	GPIO F7/VIP clock out
H11	PD0/SDPCA/TXD1	IO Pull up/O/O	GPIO D0/SD Power control/Uart1 txd
H10	PD1/SDCDA/RXD1	IO Pull up/O/O	GPIO D1/SD detect/Uart1 rxd
H9	PD2/SDWPA	IO Pull up/I	GPIO D2/SD Card wirte protect
G13	PD3/SD_CKE	IO Pull up/O	GPIO D3/SDRAM CKE
G9	PD6/PWM2	IO Pull down/O	GPIO D6/PWM2
G10	PD5/PWM1	IO Pull down/O	GPIO D5/PWM1
G11	PD4/PWM0	IO /O	GPIO D4/PWM0
G12	VDDIO	P	IO POWER SUPPLY 3.3V
F11	VSSIO	P	IO GROUND
F12	VDDD	P	CORE POWER SUPPLY 1.2V
F9	NC	B	NC
F10	NC	B	NC
F13	NC	B	NC
E10	NC	B	NC
E11	NC	B	NC
E12	VBUS_DET	I Pull down	USB VBUS detect
E13	LADC_AIN0	A	10bit adc channel0 input
D11	LADC_AIN1	A	10bit adc channel1 input
D12	LADC_AIN2	A	10bit adc channel2 input
D13	LADC_VSSA	P	10bit adc analog ground
C13	PHY_VDDA	P	10bit adc analog power 2.7V -3.3V
B13	PHY_DN	A	USB DP
A13	PHY_DP	A	USB DN
A12	PHY_VSSA	P	USB PHY Analog Ground
B12	PHY_REF	A	Resistor for USB 6.04K 1%
C12	PHY_VDDP	P	USB PHY PLL POWER 1.2V
A11	PHY_VSSP	P	USB PHY PLL Ground
B11	TDO	O	JTAG TDO
C11	TMS	I PullUp	JTAG TMS
A10	TDI	I PullUp	JTAG TDI
B10	TRST	I PullUp	JTAG TRST
C10	TCK	I PullUp	JTAG TCK
D10	RTCK	O	JTAG RTCK
A9	NC	B	NC
B9	NC	B	NC
C9	NC	B	NC
D9	NC	B	NC
E9	NC	B	NC
A8	NC	B	NC
D8	NC	B	NC
E8	NC	B	NC
F8	NC	B	NC
G8	NC	B	NC

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D7	NC	B	NC
E7	NC	O	NC
F7	NC	O	NC
G7	NC	O	NC
B8	VDDIO	P	IO POWER SUPPLY 3.3V
C8	VSSIO	P	IO GROUND
B7	VSSD	P	CORE GROUND
C7	VDDD	P	CORE POWER SUPPLY 1.2V
A7	NC	O	NC
B6	NC	O	NC
A6	NC	O	NC
C6	NC	O	NC
D6	NC	O	NC
E6	NC	O	NC
F6	SDT_A12/PF2	O/IO Pull up	SDRAM/SRAM addr[12]/GPIO F2
A5	NC	O/IO Pull up	NC
B5	NC	O	NC
C5	NC	O	NC
D5	NC	O	NC
E5	NC	O	NC
D4	TEST	I PullDown	Test mode
	VIP_PCLK	I pullup	VIP pclk
C4	VIP_VSYNC/HADC_D9	I pullup	VIP vsync
B4	VIP_HSYNC/HADC_D8	I pullup	VIP hsync
A4	HADC_CLK	O	hsadc clk output
A3	ZPLL_VDDA	P	DSP PLL power 1.2V
B3	PLL_VSSA	P	PLL Ground
A2	APLL_VDDA	P	ARM PLL power 1.2V

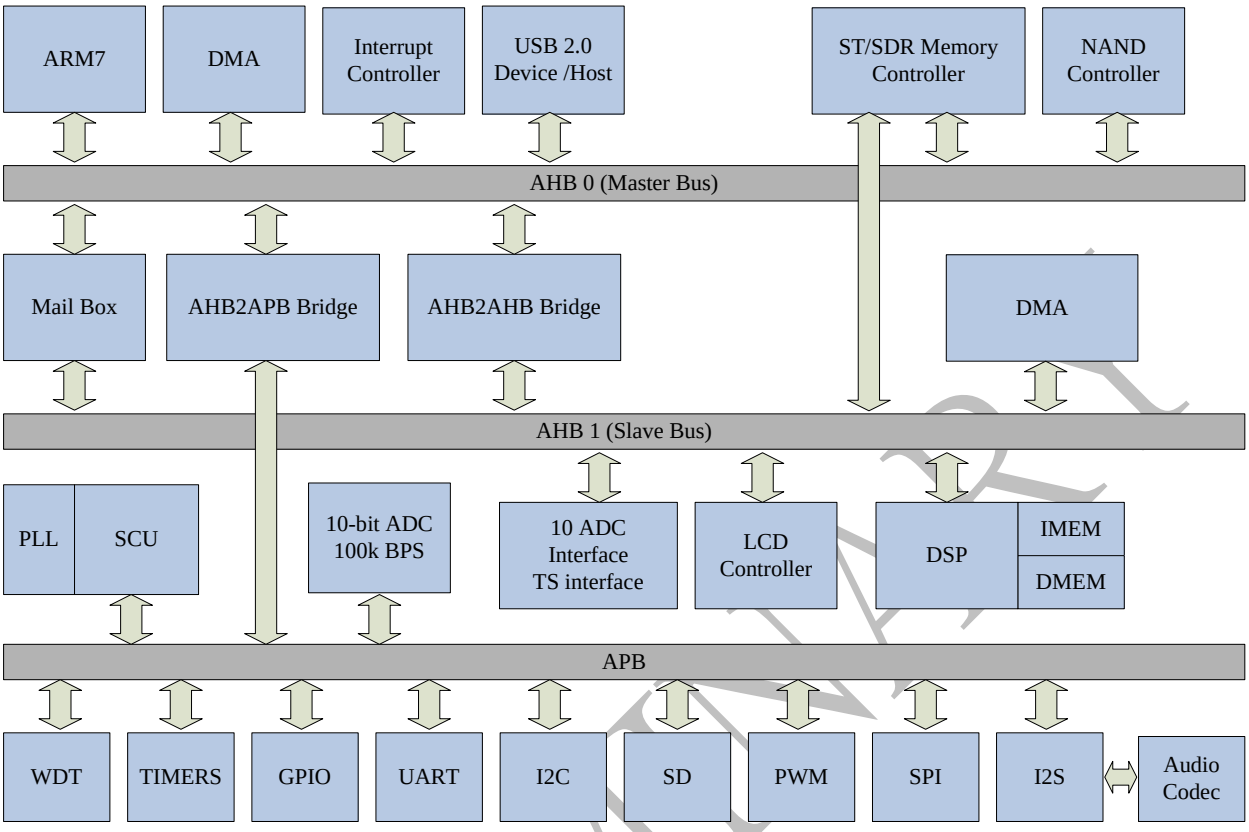
P	power supply pad
IO	IO pad
O	output pad
I	input pad
AI	analog input pad
AO	analgo output pad

PC5/PD0/PD1/PD2/PD3/PD5/PD6/PF0 can not using as input IO port, only can using as output port
B2 Pin is EWAKEUP PIN before June 2008.
UART1 only can using as TX mode, it can not receive data

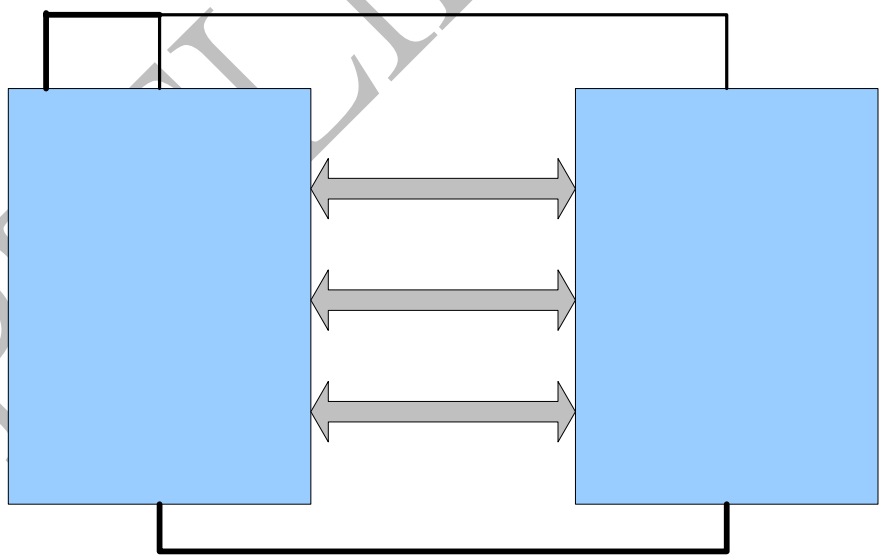
PRELIMINARY

1.4 Architercture

1.4.1 Block Diagram



1.4.2 RK2710-M Diagram



NOTE:

The RK2710-M is pin to pin compatible with RK2710-G, but embeds 8x16 low power SDRAM. The CKE of SDRAM is connecting to VDDIO internal.

The address and data line also pin out in RK2710-G, to reduce EMI and increase SDRAM running frequency, please left these pins float.

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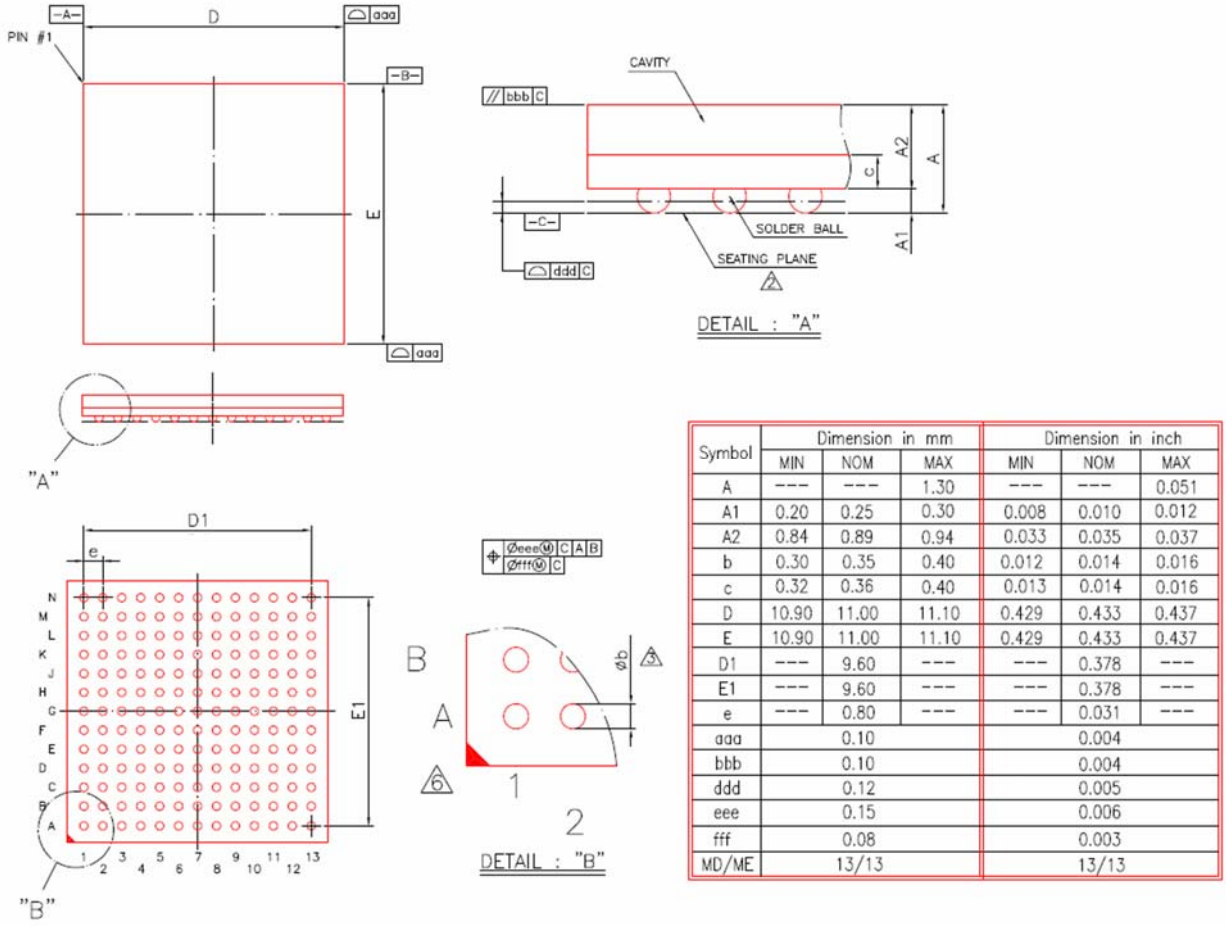
1.5 Package outline

1.5.1 BGA169 Package outline



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	0.84	0.89	0.94	0.033	0.035	0.037
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.32	0.36	0.40	0.013	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	---	9.60	---	---	0.378	---
E1	---	9.60	---	---	0.378	---
e	---	0.80	---	---	0.031	---
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.12			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	13/13			13/13		

PRELI