RK2908 Datasheet

Revision 1.0
July 2011

Revision History

Date	Revision	Description
2011-7-24	1.0	Initial Release

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Chapter 1 Introduction

RK2908 is a low power, high performance processor solution for TV BOX and other digital multimedia applications.

RK2908 integrates an ARM Cortex-A8 with one NEON coprocessor. Many embedded powerful hardware accelerators provide optimized hardware performance for high-end application. RK2908 supports almost full-format video decoder by 1080p@30fps such as H264, H263, RMVB, MPEG2, MPEG4, VC1, AVS, and VP8 etc. Also supports H.264 encoder by 1080P@30fps, high-quality JPEG encoder/decoder and special image preprocessor and postprocessor.

Embedded 2D/3D hardware engine makes RK2908 completely compatible with OpenGL ES2.0, OpenGL ES1.1 and OpenVG graphics standards.

RK2908 has high-performance external memory interface (DDRIII/DDRII/LPDDR) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications as follows:

- 8 banks, 8bits Async NAND FLASH, LBA NANDN Flash, 8bits sync ONFI NAND Flash, all embedded 24bits HW ECC
- 2 ranks, 2GB Memory space, 16bits/32bits DDRIII,DDRII-800,LPDDR-400
- 8bits HS-MMC/SD, 4bits SDIO, 8bits eMMC interface
- 24bits high-performance, 3-layers TFT LCD Controller with post-processor, 1920x1080 maximum display size
- 8bits sensor/CCIR656 interface and 10bits/12bits Raw data interface
- 2ch I2S interface, 8ch I2S interface, PCM/SPDIF interface
- USB OTG 2.0/USB Host2.0/ USB Host 1.0
- RMII/MII interface
- High-speed ADC interface, TS stream interface
- 4x I2C, 4xUART with hardware flow-control, 2x SPI, PWM

This document will provide guideline on how to use RK2908 correctly and efficiently. In them, the chapter 1 and chapter 2 will introduce the features, block diagram, and signal descriptions and system usage of RK2908, the chapter 3 through chapter 46 will describe the full function of each module in detail.

1.1 Features

1.1.1 Microprocessor

- ARM Cortex-A8 processor is a high-performance, low-power, cached application processor that provides full virtual memory capabilities
- Full implementation of the ARM architecture v7-A instruction set
- superscalar processor featuring technology for enhanced code density and performance
- Embedded NEON technology for multimedia and signal processing by executing Advanced SIMD and VFP instruction sets
- Jazelle RCT Java-acceleration technology for efficient support of ahead-of-time and just-in-time compilation of Java and other byte code language
- Thumb-2 technology for greater performance, energy efficiency and code density
- TrustZone technology for secure transactions and DRM
- 13-stage main integer core pipeline and 10-stage NEON media core pipeline
- Dynamic branch prediction with branch target address cache, global history buffer and 8-entry return stack
- MMU and separate instruction and data TLBs of 32 entries each
- 64-bit high-speed AXI interface supporting multiple outstanding transactions
- Integrated 32KB L1 instruction cache , 32KB L1 data cache, 512KB L2 Cache with parity and ECC check
- ETM support for non-invasive debug, support JTAG and 8-wire trace interface
- ARMv7 debug with watch point and breakpoint registers and a 32-bit APB slave interface to a core-sight debug system
- Four separate power domain to support Internal power switch on/off based on

different application scene(Integer core/ETM&DBG/Neon/L2 Cache)
- Maximum frequency can be up to 650MHz@worst case and 1GHz@typical case

1.1.2 Memory Organization

- Internal on-chip memory
  - 10KB Boot Rom
  - 16KB internal SRAM for security and non-security access, detailed size is programmable
  - 4KB internal SRAM shared with Host slave interface (HIF)
  - 2KB internal SRAM shared with NAND controller
- External off-chip memory①
  - DDRIII, DDRII-800, 16/32bits data width, 2 ranks, 1GB(max) address space per rank
  - LPDDR-400, 32bits data width, 2 ranks, 1GB(max) address space per rank
  - Async NAND Flash(include LBA NAND), 8 data width, 8 banks
  - Sync DDR NAND Flash, 8bits data width, 8 banks

1.1.3 Internal Memory

- Internal Boot Rom
  - Size : 10KB
  - Support system boot from the following device :
    - 8bits Async NAND Flash
    - SPI0 interface
    - eMMC interface
  - Support system code download by the following interface:
    - USB OTG
    - UART1
- Internal SRAM
  - Size : 16KB
  - Support security and non-security access
  - Security or non-security space is software programmable , used together with TZMA module
  - Security space can be 0KB, 4KB, 8KB, 12KB, 16KB continuous size

1.1.4 External Memory or Storage device

- Dynamic Memory Interface (DDRIII/DDRII/LPDDR)
  - Compatible with JEDEC standard DDRIII/DDRII/LPDDR SDRAM
  - Data rates of up to 800Mbps(400MHz) for DDRII and up to 400Mbps(200MHz) for LPDDR
  - Support up to 2 ranks (chip selects), maximum 1GB address space per rank
  - 16bits/32bits data width is software programmable
  - 5 host ports with 64bits AXI bus interface for system access, AXI bus clock asynchronous with DDR clock
  - Programmable timing parameters support DDRIII/DDRII/LPDDR SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDRII/LPDDR SDRAM; clock stop and deep power-down for LPDDR SDRAM
  - Programmable ultra-high priority port(port0), typically a CPU port
  - Compensation for board delays and variable latencies through programmable pipelines
  - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Support one low-power work mode: power down DDR PHY and most of DDR IO except two CS and two CKE output signals, make SDRAM still in self-refresh state to prevent data missing.

- NAND Flash Interface
  - Support 8bits async NAND flash, up to 8 banks
  - Support 8bits sync DDR NAND flash, up to 8 banks
  - Support LBA NAND flash in async or sync mode
  - 16bit/1KB HW ECC, compatible with 8bit/512B
  - 24bit/1KB HW ECC, compatible with 12bit/512B
  - For DDR NAND flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 75MHz
  - Embedded two 256x32bits buffers to support ping-pong operation
  - Embedded AHB master interface to do data transfer by DMA method
  - Also support data transfer by AHB slave interface together with external DMAC1

- eMMC Interface
  - Compatible with standard INAND interface
  - Support MMC4.2 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - One AHB slave interface to complete data transfer together with external DMAC1 or CPU
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support host pull-up control,card detection and initialization, write protection
  - Support block size from 1 to 65535Bytes
  - Data bus width is 8bits

- SD/MMC Interface
  - Compatible with SD ver2.00, CE-ATA ver1.1, MMC ver4.2
  - One AHB slave interface to complete data transfer together with external DMAC1 or CPU
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support host pull-up control, card detection and initialization, write protection
  - Support block size from 1 to 65535Bytes
  - Data bus width is flexible to support 1bit/4bits for SD mode and 1bit/4bits/8bits for MMC mode

1.1.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK2908
  - Support soft-reset control for individual components inside RK2908
  - Support flexible clock solution, including clock source, clock MUX, clock frequency division
  - Four embedded PLLs, source can be from two external 24MHz or 27MHz oscillator input, also support two-level cascaded PLL to meet special clock frequency requirement
  - Up to 1.6GHz clock output for ARM PLL, up to 1.0GHz clock output for another three PLLs

- PMU(power management unit)
  - Provide five work modes(slow mode, normal mode, idle mode, stop mode,

power-down mode) to save power by different frequency or automatically clock gating control or power domain on/off control
- Idle mode can be wakeup by any interrupt from every on-chip components or external GPIO
- Stop mode and power-down mode can be wakeup by external dedicated IO
- Provide 9 separately power domains, which can be power up/down by software based on different application scenes

- Timer
  - Four on-chip 32bits Timers with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - timer0 and timer1 are for CPU system domain, timer2 and timer3 are for peri system domain
  - support independent fixed clock for timer0 and timer1 from external 24MHz clock input, asynchronous with APB bus clock
  - support dependent clock for timer2 and timer3 from system, same as APB bus clock

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable 4-bit pre-scalar from apb bus clock
  - Embedded 32-bit timer/counter facility
  - Support single-run or continuous-run PWM mode
  - Support maskable interrupt
  - Provides reference mode and output various duty-cycle waveform
  - Provides capture mode and measure the duty-cycle of input waveform

- Watchdog
  - 32 bits watchdog counter width
  - Counter clock is from APB bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 64-bit multi-layer AXI/AHB composite bus architecture
  - Six embedded AXI interconnect
    - CPU L1 interconnect with two 64-bits AXI masters and six 32/64bits AXI slaves
    - CPU L2 interconnect with one 32-bits AXI master, 32-bits AXI slave and lots of 32-bits AHB /APB slaves
    - Peri interconnect with two 64-bits AXI masters, one 64-bits AXI slave, one 32-bits AXI slave, two 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - Display interconnect with three 64-bits AXI masters, two 32-bits AHB masters and one 64-bits AXI slave
    - GPU and VCODEC interconnect also with one 64-bits AXI master and one 64-bits AXI slave ,they are point-to-point AXI-lite architecture
  - For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.
  - For CPU L1/CPU L2/Peri three interconnects, provide GPV registers to be

programmed by software to support different application scenes

- Interrupt Controller
  - Support 71 interrupt sources input from different components inside RK2908 or GPIO
  - Support 16 software-triggered interrupts
  - Two AXI slave interfaces for shared distributor and cpu to manage individual registers with different intention
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt output (nFIQ and nIRQ) to Cortex-A8, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable
  - Support security extension to make some registers only be accessed in system security mode

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controller , DMAC0 is for CPU system, DMAC1 is for peri system
  - DMAC0 features:
    - 6 channels totally
    - 8 hardware request from peripherals
    - 3 interrupt output
    - Dual APB slave interface for register configure, designated as secure and non-secure
    - Support trustzone technology and programmable secure state for each DMA channel
  - DMAC1 features:
    - 7 channels totally
    - 20 hardware request from peripherals
    - 4 interrupt output
    - Not support trustzone technology

- Security system
  - Support trustzone technology for the following components inside RK2908
    - Cortex-A8, support security and non-security mode, switch by software
    - Interrupt controller, support some registers and dedicated interrupt sources to work only in security mode
    - DMAC0, support some dedicated channels work only in security mode
    - eFuse, only accessed by Cortex-A8 in security mode
    - Internal memory , part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(trustzone memory adapter) and TZPC(trustzone protection controller)

1.1.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264 , AVS , VC-1 , RV , VP8 , Sorenson Spark

- Error detection and concealment support for all video formats
- Output data structure after decoder is YCbCr 4:2:0 semi-planar to have more efficient bus usage, For H.264, YCbCr 4:0:0(monochrome) is also supported
- Minimum image size is 48x48 for all video formats
- H.264 up to HP level 4.2 : 1080p@60fps (1920x1088)[8]
- MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1088)
- MPEG-2 up to MP : 1080p@60fps (1920x1088)
- MPEG-1 up to MP : 1080p@60fps (1920x1088)
- H.263 : 576p@60fps (720x576)
- Sorenson Spark : 1080p@60fps (1920x1088)
- VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
- RV8/RV9/RV10 : 1080p@60fps (1920x1088)
- VP6/VP7/VP8 : 1080p@60fps (1920x1088)
- AVS : 1080p@60fps (1920x1088)
- For AVS, 4:4:4 sampling not supported
- For H.264, Image cropping not supported
- For MPEG-4,GMC(global motion compensation) not supported
- For VC-1, upscaling and range mapping are supported in image post-processor
- For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Encoder only for H.264 (BP@level4.0, MP@level4.0,HP@level4.0) standard
  - Only support I and P slices, not B slices
  - Entropy encoding is CAVLC in BP and CABAC in MP
  - Support error resilience based on constrained intra prediction and slices
  - Maximum MV length is +/- 14 pixels in vertical direction and +/-30 pixels in horizontal direction
  - Motion vector pixel accuracy is up to 1/4 pixels in 720p resolution and 1/2 pixels in 1080p resolution
  - 12 intra prediction modes
  - Number of reference frames is 1
  - Maximum number of slice groups is 1
  - Input data format :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output data format : H.264 byte unit stream and H.264 NAL unit stream
  - Image size is from 96x96 to 1920x1088(Full HD)
  - Maximum frame rate is up to 30fps@1920x1080[8]
  - Bit rate supported is from 10Kbps to 20Mbps

1.1.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Maximum data rate[4] is up to 76million pixels per second
  - Thumbnail decoding and error detection is supported
  - Non-interleaved data order not supported

- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate④ up to 90million pixels per second
  - Support thumbnail insertion with RGB8bits, RGB24bits and JPEG compressed thumbnails

1.1.8 Image Enhancement

- Image pre-processor
  - Only used together with video encoder inside RK2908 , not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT.601 , BT.709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees

- Video stabilization
  - Work in combined mode with video encoder inside RK2908 and stand-alone mode
  - Maximum stabilization displacement in pixels for two sequential input video pictures is +/- 16 pixels
  - Adaptive motion compensation filter
  - Offset around stabilized picture is minimum 8 pixels in standalone mode and 16 pixels in combined mode
  - Support scene detection from video sequence, encodes key frame when scene change noticed

- Image post-processor
  - Combined with video/jpeg decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from a camera interface or other image data stored in external memory
  - Input data format :
    - any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
  - Ouput data format:
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2

- Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB 32bit(8-8-8-8),RGB 16bit(5-6-5),ARGB 16bit(4-4-4-4)
- Input image size:
  - Combined mode : from 48x48 to 8176x8176 (66.8Mpixels)
  - Stand-alone mode : width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
  - Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
- Support image up-scaling :
  - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Maximum output width is 3x input width
  - Maximum output height is 3x input height, and 2.5x input height when running RV/VP7/VP8 format decoder
- Support image down-scaling:
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Unlimited down-scaling ratio
- Not allowed to perform horizontal up-scaling and vertical down-scaling at the same time
- Support YCbCr to RGB color conversioin, compatible with BT.601-5 ,BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering for 4,5,6bit RGB channel precision
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
  - 8bit alpha value+YCbCr4:4:4,big-endian channel order being AYCbCr, 8bits each
  - 8bit alpha value+24bit RGB, big-endian channel order being ARGB,8bits each
- Support de-interlacing with conditional spatial de-interlace filtering, only compatible with YCbCr4:2:0 input format
- Support RGB image contrast / brightness / color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

1.1.9 Graphics Engine

- Compatible with OpenGL ES2.0 , OpenGL ES1.1, OpenVG1.1, DirectFB, GDI/DirectDraw, EGL1.4
- Support shader model3.0
- Geometry rate : 60M tri/s
- Depth-only Pixel rate : 600M pix/s
- Textured Pixel rate : 600M pix/s
- Vertex rate : 300M vert/s
- 2D Graphics Engine :
  - Bit Blit, Stretch Blit, Filter Blit
  - Rectangle fill and clear
  - Line drawing
  - Copy bit
  - Filter
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2,ROP3,ROP4 full alpha blending and transparency
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules, chroma key, and pattern mask

- Transparency by monochrome mask
- 32K x 32K raster 2D coordinate system
- 90,180 and 270 degrees rotation on every 2D primitive
- Programmable high quality 9-tap,32-phase filter to support image scaling
- Blending, scaling and rotation are supported in one pass for stretch Blit
- Source format :
  - RGBA4444,5551,8888
  - RGBX4444,5551,8888
  - RGB565
  - UYVY4:2:2, YUY2(4:2:2),YV12(4:2:0)
- Destination formats :
  - RGBA4444,5551,8888
  - RGBX4444,5551,8888
  - RGB565

- 3D Graphics Engine :
  - IEEE 32-bit floating-point pipeline
  - Ultra-threaded, unified vertex and fragment shaders
  - Low CPU loading and low bandwidth at both high and low data rates
  - Up to 12 programmable elements per vertex
  - Dependent texture operation with high-performance
  - Alpha blending
  - Support video texture
  - Depth and stencil compare
  - Support for 8 fragment shader simultaneous textures
  - Support for 12 vertex shader simultaneous textures
  - Point sampling,bit-linear sampling,tri-linear filtering and cubic textures
  - Resolve and fast clear
  - 8k x 8k texture size and 8k x 8k rendering target

1.1.10 Video IN/OUT

- Camera Interface
  - Support CMOS type image sensor interface
  - Support CCIR656 interface
  - Support CCIR656 YCbCr 4:2:2 raster video input for 8bit mode in 525/60 NTSC and 625/50 PAL video system
  - Data input clock is 27MHz for CCIR656 and 24MHz/48MHz for sensor, and max up to 96MHz for raw data
  - Provide YUV 4:2:2/4:2:0 output
  - Support up to 3856x2764 resolution and maximum 10M pixels
  - Support YUYV/UYVY format input
  - Support 10/12-bit raw data input
  - In sensor mode, support software-programmable vsync and href high active or low active
  - Embedded AXI 64bits master interface to improve performance, also compatible with AHB 32bits master interface

- Display Interface
  - Image Post-Processor (IPP)
    - memory to memory mode
    - input data format and size
      - RGB888 : 16x16 to 8191x8191
      - RGB565 : 16x16 to 8191x8191
      - YUV422/YUV420 : 16x16 to 8190x8190
      - YUV444 : 16x16 to 8190x8190
    - pre scaler
      - integer down-scaling(ratio: 1/2,1/3,1/4,1/5,1/6,1/7,1/8) with linear filter

- deinterlace(up to 1080i) to support YUV422&YUV420 input format
- post scaler
  - down-scaling with 1/2 ~ 1 arbitary non-integer ratio
  - up-scaling with 1~4 arbitary non-integer ratio
  - 4-tap vertical, 2-tap horizontal filter
  - The max output image width of post scaler is 4096
- Support rotation with 90/180/270 degrees and x-mirror, y-mirror

- LCD Controller
  - Display Interface
    - Parallel RGB LCD Interface:
      24bit(RGB888)
      18bit(RGB666)
      16bit(RGB565)
    - Serial RGB LCD Interface:
      3x8bit (RGB delta support)
      3x8bit + dummy
      16bit + 8bit
    - MCU LCD interface:
      I-8080 (up to 24-bit RGB)
      Hold/Auto/Bypass modes
    - TV interface : ITU-R BT.656(8-bits, 480i/576i/1080i)
  - Display Process
    - One background layer: programmable 24-bit color
    - One video layer(win0)
      - ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444, AYCbCr
      - maximum resolution is 1920x1080
      - virtual display
      - 1/8 to 8 scaling-down and scaling-up engine with arbitrary non-integer ratio
      - 256 level alpha blending(no scaling in ARGB/AYCbCr mode)
      - transparency color key
      - deflicker support for interlace output
      - sharp/smooth filter
    - One graphic layer(win1)
      - RGB888, ARGB888, RGB565
      - maximum resolution is 1920x1080
      - virtual display
      - 256 level alpha blending
      - transparency color key
    - One OSD layer(win2)
      - 1/2/4/8bpp palette mode
      - maximum resolution is 1920x1080
      - 8-bit alpha Alpha
      - transparency color key
    - Hardware cursor(HWC)
      - 32x32x2bpp
      - 3-color and transparent mode
      - 2-color + transparency + tran_invert mode
      - 16 level alpha blending
  - 3 x 256 x 8 bits display LUTs
  - Graphic layer and video layer overlay exchangeable
  - Support color space conversion : YCbCr-to-RGB(rec601-mpeg/ rec601-jpeg/rec709) and RGB-to-YCbCr
  - Support replication(16-bit to 24-bit) and dithering(24-bit to 16-bit/18-bit) operation
  - Blank and black display
  - Standby mode

1.1.11 Audio Interface

- I2S/PCM with 8ch
  - Compatible audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Embedded 4 TX FIFO and 1 RX FIFO with 32x32bits size
  - Support I2S normal , left-justified , right-justified three data formats in I2S mode
  - Support early , late1 , late2 , late3 four data formats in PCM mode
  - For I2S mode only, support software-configurable channel number(TX : 2/4/6/8; RX:2)
  - For PCM mode only, support software-configurable channel number(TX : 2/4/6/8; RX:2)
  - In master TX mode, Support I2S and PCM work simultaneously in condition of same audio data and same sample rate , and only use two channels separately for I2S and PCM
  - Support SCLK and LRCK polarity software-configurable
  - SCLK can be even-divided by 2 to 64 from i2s main clock

- I2S/PCM with 2ch
  - Compatible audio data width from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Embedded 1 TX FIFO and 1 RX FIFO with 32x32bits size
  - Support I2S normal mode, I2S left-justified mode , I2S right-justified mode
  - Support PCM early mode , late1 mode, late2 mode , late3 mode
  - I2S and PCM cannot be used at the same time
  - Support SCLK and LRCK polarity software-configurable
  - SCLK can be even-divided by 2 to 64 from i2s main clock

- SPDIF
  - Embedded one 32x32bits buffer
  - Provides audio data with biphase encode
  - Support stereo voice replay with 2 channels
  - Support software configurable sample rates (48KHz, 44.1KHz, 32KHz)
  - Support audio data width 16bits/20bits/24bits
  - Frame frequency is 128x audio data sample rates

1.1.12 Connectivity

- SDIO interface
  - Compatible with SDIO ver1.00
  - One AHB slave interface to complete data transfer together with external DMAC1 or CPU
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support host pull-up control, card detection and initialization, write protection
  - Support block size from 1 to 65535Bytes
  - Data bus width is flexible to support 1bit/4bits
  - Support SDIO suspend and resume operation
  - Support SDIO read wait

- High-speed ADC & TS stream interface

- Only support one-channel (only I, not Q channel) 8bits/10bits data input
- DMA-based and interrupt-based operation
- Support 8bits TS stream data receive
- Support PID filter operation
  - Combined with high-speed ADC interface to implement filter from original TS data
  - Provide PID filter up to 64 channels PID simultaneously
  - Support sync-byte detection in transport packet head
  - Support packet lost mechanism in condition of limited bandwidth

- MAC 10/100M Ethernet Controller
  - IEEE802.3u compliant Ethernet Media Access Controller(MAC)
  - 10Mbps and 100Mbps compatible
  - Automatic retry and automatic collision frame deletion
  - Full duplex support
  - PAUSE full-duplex flow-control support
  - Address filtering(broadcast, multicast, logical, physical)
  - Support RMII(Reduced MII) and MII(Media Independent Interface) mode
  - In RMII mode, clock can be from RK2908 or external Ethernet PHY

- SPI Controller
  - Two on-chip SPI controller inside RK2908
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- UART Controller
  - Four on-chip UART controller inside RK2908
  - DMA-based or interrupt-based operation
  - Embedded two 32Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Support IrDA1.0 SIR(115.2Kbps) mode for UART1
  - Auto flow control mode is only for UART0,UART2,UART3

- I2C controller
  - Four on-chip I2C controller in RK2908
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - 7 groups of GPIO (GPIO0~GPIO6) , 32 GPIOs per group, totally have 180 GPIOs
  - All of GPIOs can be used to generate interrupt to cortex-A8
  - In power-down mode, status(IO direction and output level) of GPIO0~GPIO5 can be controlled by another registers in always-on domain
  - Totally 66 GPIOs(GPIO0,GPIO4,GPIO6) can be used to wakeup system from stop mode or power-down mode
  - All of pull-up GPIOs are software-programmable for pull-up resistor or not
  - All of pull-down GPIOs are software-programmable for pull-down resistor or not
  - All of GPIOs are pull-up or pull-down in default except GPIO1[5] MUX with PWM3

after power-on-reset
- All of GPIOs are always in input direction in default after power-on-reset

- USB Host1.1
  - Compatible with USB host1.1 specification
  - Only supports full-speed transfer up to 12Mbps
  - Provides 6 host mode channels
  - Support periodic out channel

- USB Host2.0
  - Compatible with USB host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 3 host mode channels

- USB OTG2.0
  - Compatible with USB otg2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 6 device mode endpoints in addition to control endpoint 0
  - Support up to 4 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Provides 6 host mode channels
  - Support periodic out channel in host mode

1.1.13 Others

- SAR-ADC(Successive Approximation Register)
  - 4-channel single-ended 10-bit SAR analog-to-digital converter
  - Conversion speed range is from 0.1 to 1 MSPS
  - SAR-ADC clock must be less than 1MHz
  - DNL less than ±1 LSB , INL less than ±2.0 LSB
  - Power down current is about 1uA
  - 2.5V Power supply for analog interface

- eFuse
  - 1024bits (128x8) high-density electrical Fuse
  - Programming condition : VQPS must be 2.5V(±10%)
  - Program time is about 4~6us
  - Read condition : VQPS must be 0V or floating or 2.5V(±10%)
  - Provide power-down and standby mode

- Package Type
  - TFBGA432 (body: 16mm x 16mm ; ball size : 0.3mm ; ball pitch : 0.65mm)

Notes : ① : DDRII and LPDDR are not used simultaneously as well as async and sync DDR NAND flash
② : In RK2908, Video decoder and encoder are not used simultaneously because of shared internal buffer
③ : Actual maximum frame rate will depend on the clock frequency and system bus performance
④ : Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.2 Block Diagram

The following diagram shows the basic block diagram for RK2908.

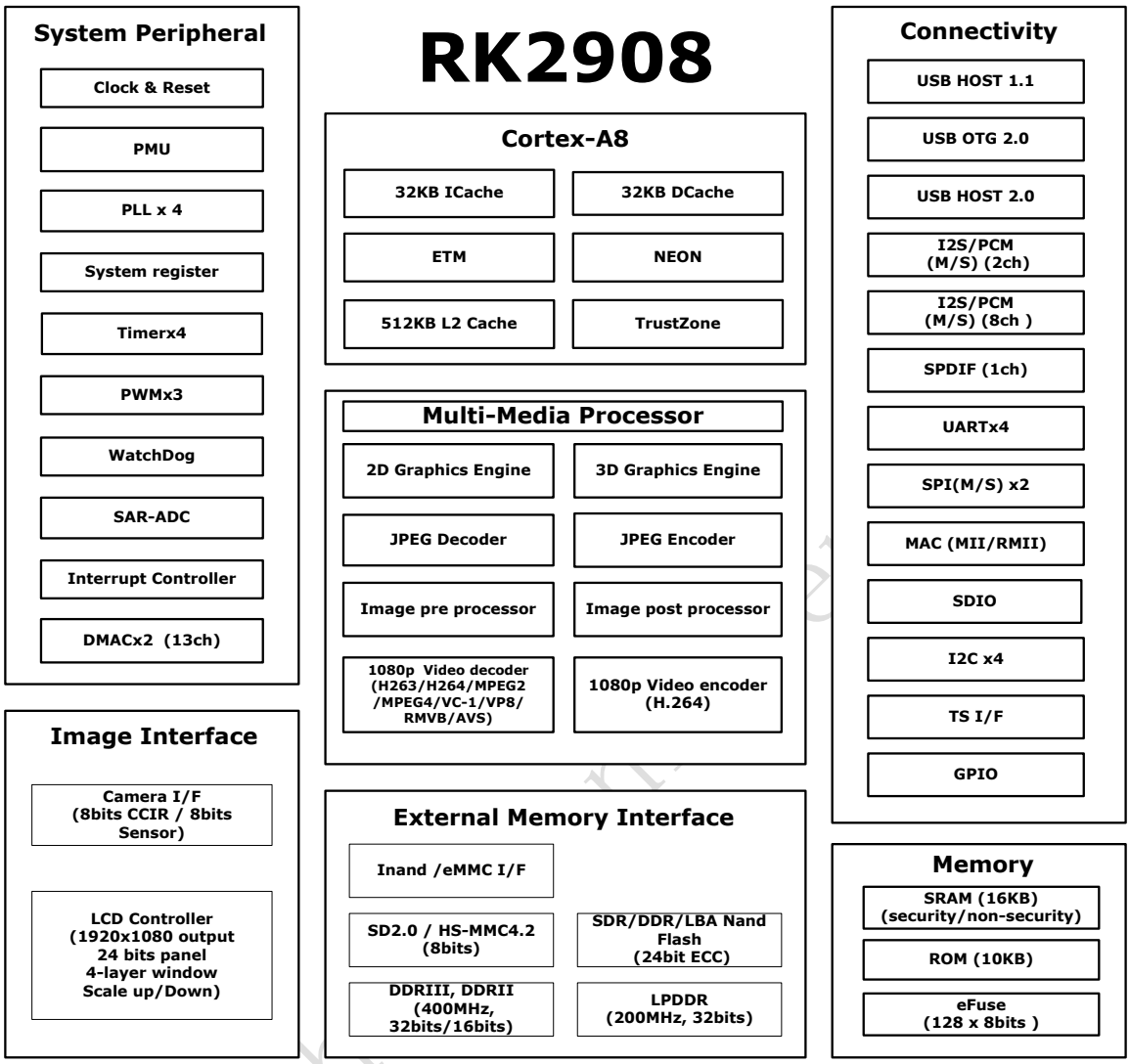


Fig. 1-1 RK2908 Block Diagram

Chapter 2 Package Description

2.1 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12
A	GPIO0_A[0]	GPIO6_B[4]	NP	GPIO6_A[4]	GPIO6_A[0]	NP	GPIO1_B[6]/UART0_SIN	GPIO3_A[4]/I2S1_SDO	NP	GPIO6_B[5]	GPIO2_B[6]/I2C0_SDA	NP
B	GPIO4_A[1]	GPIO0_A[2]	GPIO5_A[1]	GPIO6_B[0]	GPIO6_A[6]	GPIO6_A[2]	GPIO1_C[0]/UART0_CTS_N/SDMMC1_DETECT_N	GPIO2_B[0]/UART2_SIN	GPIO3_A[2]/I2S1_LRCK_RX	GPIO5_D[5]/SDMMC0_PWR_EN	GPIO5_D[3]/I2C2_SDA	GPIO1_A[5]/EMMC_PWR_EN/PWM3
C	NP	GPIO2_B[5]/UART3_RTS_N/I2C3_SCL	GPIO4_A[3]	GPIO0_A[4]	GPIO6_B[2]	GPIO2_B[4]/UART3_CTS_N/I2C3_SDA	GPIO2_B[2]/UART3_SIN	NP	GPIO2_A[6]/UART2_CTS_N	GPIO3_A[1]/I2S1_SCLK	GPIO6_B[7]	GPIO2_A[2]/SDMMC0_DETECT_N
D	GPIO6_A[3]	GPIO6_A[1]	GPIO1_C[1]/UART0_RTS_N/SDMMC1_WRITE_PRT	NP	NP	GPIO6_A[7]	GPIO2_B[1]/UART2_SOUT	NP	GPIO5_D[6]/SDMMC1_PWR_EN	GPIO2_A[4]/UART1_SIN	NP	GPIO1_A[3]/EMMC_DETECT_N/SPI1_CSN1
E	GPIO6_A[5]	GPIO6_B[3]	GPIO5_A[0]	NP	NP	NP	GPIO6_B[1]	NP	GPIO2_A[7]/UART2_RTS_N	GPIO6_B[6]	NP	GPIO1_B[5]/PWM0
F	NP	GPIO5_A[2]	GPIO0_A[1]	GPIO0_A[3]	NP	AHVDD_APLL	AHVSS_APLL	NP	GPIO3_A[5]/I2S1_LRCK_TX	GPIO3_A[0]/I2S1_CLK	NP	GPIO2_A[3]/SDMMC0_WRITE_PRT/PWM2/UART1_SIR_OUT
G	XOUT24M	XIN24M	GND	AVDD_PLL	AVSS_PLL	DVDD_PLL	DVSS_PLL	NP	GPIO5_D[2]/PWM1/UART1_SIR_IN	GPIO2_A[5]/UART1_SOUT	NP	GPIO5_D[4]/I2C2_SCL
H	XOUT27M	XIN27M	NP	NP	NP	NP	NP	GPIO2_B[3]/UART3_SOUT	GPIO2_B[7]/I2C0_SCL	VDDCORE	VDDCORE	VDDCORE
J	NP	TDI	TMS	VDDIO0	GPIO4_A[4]	VDDIO5	GPIO1_B[7]/UART0_SOUT	GPIO3_A[3]/I2S1_SDI	VDDCORE	NP	NP	VDDCORE
K	DQ[2]	NPOR	TRST_N	TCK	TDO	GPIO4_A[2]	GND	DVDDR	NP	GND	GND	GND
L	DQ[17]	DQ[16]	DQ[3]	NP	NP	NP	NP	GND	NP	GND	GND	GND
M	NP	DQ[19]	DQ[18]	DQ[1]	DQ[0]	DM[0]	VREF0	DVDDR	VDDCORE	GND	GND	GND

13	14	15	16	17	18	19	20	21	22	23	24	
NP	GPIO1_A[6]/I2C1_SDA	GPIO6_C[2]	NP	GPIO0_A[6]/MII_MD	GPIO2_C[7]/SPI1_RXD	NP	GPIO3_D[1]	GPIO3_C[2]_DATA[13]	NP	VREF_OUT	GPIO5_B[5]/HSADC_DATA8/TS_VALID	A
GPIO4_A[5]/OTG0_DRV_VBUS	GPIO6_C[6]	GPIO6_C[0]	GPIO3_D[4]	GPIO3_D[2]	GPIO2_C[2]/SPI0_TXD	GPIO3_C[7]	GPIO3_A[7]	RECOVER	GPIO5_A[4]/TS_SYNC	GPIO5_B[1]/HSADC_DATA4	GPIO5_A[7]/HSADC_DATA2	B
GPIO4_D[0]	GPIO4_D[2]	GPIO6_D[2]	GPIO6_D[0]	NP	GPIO2_C[5]/SPI1_CSN0	GPIO2_C[3]/SPI0_RXD	VDDIO3	GPIO5_B[3]/HSADC_DATA6	GPIO5_A[5]/HSADC_DATA0	GPIO4_C[7]/RMII_RXD0/MII_RXD0	NP	C
GPIO4_D[4]	NP	GPIO1_A[4]/EMMC_WRITE_PRT/SPI0_CSN1	GPIO6_C[4]	NP	GPIO2_C[6]/SPI1_TXD	GPIO3_C[3]	NP	NP	GPIO5_B[4]/HSADC_DATA7	GPIO4_C[5]/RMII_CRS_DVALID/MII_RXD_VALID	GPIO4_C[2]/RMII_TXD1/MII_TXD1	D
GPIO4_D[5]	NP	GPIO6_C[7]	GPIO4_A[7]/SPDIF_TX	NP	GPIO2_C[0]/SPI0_CLK	NP	NP	NP	GPIO5_B[2]/HSADC_DATA5	GPIO4_D[6]/I2S0_LRCK_TX0	GPIO4_C[0]/RMII_CLKOUT/RMII_CLKIN	E
GPIO4_D[1]	NP	GPIO4_A[6]/HOST20_DRV_VBUS	GPIO2_C[1]/SPI0_CSN0	NP	GPIO3_C[6]	GPIO3_D[0]	NP	GPIO5_A[3]/MII_TX_CLKIN	GPIO2_D[2]/I2S0_LRCK_RX/MII_TX_ERR	GPIO2_D[6]/I2S0_SDO2/MII_TXD2	NP	F
GPIO4_D[3]	NP	GPIO1_A[7]/I2C1_SCL	GPIO5_D[7]	NP	GPIO5_B[6]/HSADC_DATA9/TS_FAIL	GPIO4_C[3]/RMII_TXD0/MII_TXD0	GPIO4_C[4]/RMII_RX_ERR/MII_RX_ERR	GPIO4_C[6]/RMII_RXD1/MII_RXD1	GPIO2_D[0]/I2S0_CLK/MII_RX_CLKIN	GPIO2_A[0]/SDMMC0_DATA6	GPIO2_D[4]/I2S0_SDO0/MII_RXD2	G
GPIO6_C[5]	VDDIO4	GPIO6_C[1]	GPIO6_D[1]	GPIO3_C[5]	NP	NP	NP	NP	NP	GPIO1_D[4]/SDMMC0_DATA2	GPIO1_D[6]/SDMMC0_DATA4	H
VDDCORE	NP	NP	GPIO6_C[3]	GPIO3_A[6]	GPIO2_D[1]/I2S0_SCLK/MII_CRS	GPIO4_D[7]/I2S0_LRCK_TX1	GPIO4_C[1]/RMII_TX_EN/MII_TX_EN	GPIO1_D[5]/SDMMC0_DATA3	GPIO1_D[0]/SDMMC0_CLKOUT	GPIO1_D[2]/SDMMC0_DATA0	NP	J
GND	GND	GND	NP	GPIO2_C[4]/SPI1_CLK	GPIO2_D[5]/I2S0_SDO1/MII_RXD3	GPIO2_D[3]/I2S0_SDI/MII_COL	GPIO2_D[7]/I2S0_SDO3/MII_TXD3	GPIO2_A[1]/SDMMC0_DATA7	VDDIO2	GPIO1_C[4]/SDMMC1_DATA1	GPIO1_C[6]/SDMMC1_DATA3	K
GND	GND	GND	NP	GPIO0_A[7]/MII_MDCLK	NP	NP	NP	NP	GPIO3_B[4]/EMMC_DATA2	GPIO3_C[0]/EMMC_DATA6	GPIO1_C[2]/SDMMC1_CMD	L
GND	GND	GND	VDDCORE	GPIO3_D[3]	GPIO0_D[3]/FLASH_CSN2	GPIO1_D[7]/SDMMC0_DATA5	GPIO1_C[5]/SDMMC1_DATA2	GPIO0_D[7]/FLASH_CSN6	GPIO3_B[2]/EMMC_DATA0	GPIO3_B[6]/EMMC_DATA4	NP	M

N	NP	DQS_B[2]	DQS[2]	DQ[4]	DQS_B[0]	DQS[0]	DVDDR	GND	GND	GND	GND	GND
P	DQ[20]	DQ[21]	DM[2]	NP	NP	NP	NP	DVDDR	NP	GND	GND	GND
R	DQ[22]	DQ[23]	BA[0]	DQ[7]	DQ[6]	DQ[5]	DVDDR	GND	NP	GND	GND	GND
T	NP	ZQ_PIN	BA[1]	BA[2]	A[1]	A[0]	VREF1	DVDDR	GND	NP	NP	VDDCORE
U	CS_B0	CKE0	NP	NP	NP	NP	NP	GND	DVDDR	GND	VDDIO_LCD0	VDDIO_LCD1
V	CK_B	CK	VREF_IN	A[2]	CKE1	RESET	DQ[11]	NP	VREF2	DVDDR	NP	LCDC_DEN
W	NP	CS_B1	A[3]	A[4]	NP	DQ[8]	DM[1]	NP	DQ[12]	LCDC_DATA[3]	NP	LCDC_DATA[9]
Y	ODT0	WE_B	A[6]	NP	NP	NP	DQS_B[1]	NP	DQ[13]	LCDC_DATA[1]	NP	LCDC_DCLK
AA	RAS_B	CAS_B	A[5]	NP	NP	DQ[10]	DQS[1]	NP	DQ[14]	LCDC_DATA[4]	NP	LCDC_DATA[7]
AB	NP	ODT1	A[11]	A[14]	DQ[9]	DQ[25]	DM[3]	NP	DQ[15]	LCDC_DATA[0]	LCDC_DATA[6]	LCDC_DATA[5]
AC	A[7]	A[9]	A[15]	A[13]	DQ[26]	DQ[24]	DQS_B[3]	DQ[28]	DQ[30]	LCDC_DATA[2]	LCDC_HSYNC	LCDC_DATA[8]
AD	A[8]	A[10]	NP	A[12]	DQ[27]	NP	DQS[3]	DQ[29]	NP	DQ[31]	LCDC_VSYNC	NP
	1	2	3	4	5	6	7	8	9	10	11	12

GND	GND	GND	VDDCORE	GPIO6_D[3]	FLASH_WRN	GPIO1_D[3]/SDMMC0_DATA1	GPIO1_C[3]/SDMMC1_DATA0	FLASH_CLE	FLASH_WP	GPIO3_B[1]/EMMC_CMD	NP	N
GND	GND	GND	NP	GPIO5_B[7]/HSADC_CLKOUT/GPS_CLK	NP	NP	NP	NP	FLASH_DATA[5]	FLASH_DATA[3]	FLASH_DATA[4]	P
GND	GND	GND	NP	GPIO5_B[0]/HSADC_DATA3	GPIO3_B[5]/EMMC_DATA3	GPIO3_B[7]/EMMC_DATA5	GPIO3_B[0]/EMMC_CLKOUT	GPIO0_D[5]/FLASH_CSN4	GPIO0_A[5]/FLASH_DQS	FLASH_DATA[1]	FLASH_DATA[2]	R
VDDCORE	NP	NP	VDDCORE	GPIO5_A[6]/HSADC_DATA1	GPIO1_D[1]/SDMMC0_CMD	FLASH_RDY	GPIO3_B[3]/EMMC_DATA1	GPIO0_D[6]/FLASH_CSN5	FLASH_DATA[7]	EFUSE_VQPS	NP	T
LCDC_DATA[21]	VIP_DATAIN[7]	VIP_DATAIN[11]	VDDIO1	GPIO1_C[7]/SDMMC1_CLKOUT	NP	NP	NP	NP	NP	HOST20_VSSAC	FLASH_DATA[0]	U
LCDC_DATA[15]	NP	LCDC_DATA[23]	GPIO1_B[4]/VIP_CLKOUT	NP	GPIO1_A[0]/FLASH_CSN7/MDDR_TQ	FLASH_DATA[6]	GPIO0_D[2]/FLASH_CSN1	FLASH_RDN	FLASH_ALE	HOST20_DVDD	HOST20_DVSS	V
LCDC_DATA[17]	NP	VIP_DATAIN[5]	GPIO1_B[1]/VIP_DATAIN[1]	NP	GPIO3_C[1]/EMMC_DATA7	VDDA_SARADC	NP	OTG0_ID	OTG0_VSSA	HOST20_VSSA	NP	W
LCDC_DATA[13]	NP	VIP_HREF	GPIO1_B[3]/VIP_DATAIN[3]	NP	SARADC_AIN[1]	NP	NP	NP	OTG0_VDD33	HOST20_VDD33	HOST20_VDD25	Y
LCDC_DATA[11]	NP	LCDC_DATA[19]	VIP_DATAIN[9]	NP	SARADC_AIN[3]	FLASH_CSN0	NP	NP	OTG0_DVSS	OTG0_DVDD	HOST20_RKELVIN	AA
LCDC_DATA[14]	LCDC_DATA[20]	VIP_DATAIN[10]	VDDIO_VIP	NP	GPIO1_B[2]/VIP_DATAIN[2]	VDDIO_FLASH0	GPIO0_D[4]/FLASH_CSN3	OTG0_VBUS	SARADC_AIN[0]	OTG0_VSSAC	NP	AB
LCDC_DATA[10]	LCDC_DATA[16]	VIP_DATAIN[4]	VIP_DATAIN[6]	VIP_VSYNC	VIP_CLKIN	GPIO1_B[0]/VIP_DATAIN[0]	OTG0_VDD25	OTG0_DP	SARADC_AIN[2]	HOST20_DP	USBHOST_DP	AC
NP	LCDC_DATA[12]	LCDC_DATA[18]	NP	LCDC_DATA[22]	VIP_DATAIN[8]	NP	OTG0_RKELVIN	OTG0_DM	NP	HOST20_DM	USBHOST_DN	AD
13	14	15	16	17	18	19	20	21	22	23	24	

Fig. 2-1 RK2908 Ball Mapping Diagram

2.2 Pin Number Order

Table 2-1 RK2908 Pin Number Order Information

Ball #	Pin Name	Ball #	Pin Name
A1	GPIO0_A[0]	B1	GPIO4_A[1]
A2	GPIO6_B[4]	B2	GPIO0_A[2]
A3	NP	B3	GPIO5_A[1]
A4	GPIO6_A[4]	B4	GPIO6_B[0]
A5	GPIO6_A[0]	B5	GPIO6_A[6]
A6	NP	B6	GPIO6_A[2]
A7	GPIO1_B[6]/UART0_SIN	B7	GPIO1_C[0]/UART0_CTS_N/SDMMC1_DETECT_N
A8	GPIO3_A[4]/I2S1_SDO	B8	GPIO2_B[0]/UART2_SIN
A9	NP	B9	GPIO3_A[2]/I2S1_LRCK_RX
A10	GPIO6_B[5]	B10	GPIO5_D[5]/SDMMC0_PWR_EN
A11	GPIO2_B[6]/I2C0_SDA	B11	GPIO5_D[3]/I2C2_SDA
A12	NP	B12	GPIO1_A[5]/EMMC_PWR_EN/PWM3
A13	NP	B13	GPIO4_A[5]/OTG0_DRV_VBUS
A14	GPIO1_A[6]/I2C1_SDA	B14	GPIO6_C[6]
A15	GPIO6_C[2]	B15	GPIO6_C[0]
A16	NP	B16	GPIO3_D[4]
A17	GPIO0_A[6]/MII_MD	B17	GPIO3_D[2]
A18	GPIO2_C[7]/SPI1_RXD	B18	GPIO2_C[2]/SPI0_TXD
A19	NP	B19	GPIO3_C[7]
A20	GPIO3_D[1]	B20	GPIO3_A[7]
A21	GPIO3_C[2]	B21	RECOVER
A22	NP	B22	GPIO5_A[4]/TS_SYNC
A23	VREF_OUT	B23	GPIO5_B[1]/HSADC_DATA4
A24	GPIO5_B[5]/HSADC_DATA8/TS_VALID	B24	GPIO5_A[7]/HSADC_DATA2
C1	NP	D1	GPIO6_A[3]
C2	GPIO2_B[5]/UART3_RTS_N/I2C3_SCL	D2	GPIO6_A[1]
C3	GPIO4_A[3]	D3	GPIO1_C[1]/UART0_RTS_N/SDMMC1_WRITE_PRT
C4	GPIO0_A[4]	D4	NP
C5	GPIO6_B[2]	D5	NP
C6	GPIO2_B[4]/UART3_CTS_N/I2C3_SDA	D6	GPIO6_A[7]
C7	GPIO2_B[2]/UART3_SIN	D7	GPIO2_B[1]/UART2_SOUT
C8	NP	D8	NP
C9	GPIO2_A[6]/UART2_CTS_N	D9	GPIO5_D[6]/SDMMC1_PWR_EN
C10	GPIO3_A[1]/I2S1_SCLK	D10	GPIO2_A[4]/UART1_SIN
C11	GPIO6_B[7]	D11	NP
C12	GPIO2_A[2]/SDMMC0_DETECT_N	D12	GPIO1_A[3]/EMMC_DETECT_N/SPI1_CSN1
C13	GPIO4_D[0]	D13	GPIO4_D[4]
C14	GPIO4_D[2]	D14	NP
C15	GPIO6_D[2]	D15	GPIO1_A[4]/EMMC_WRITE_PRT/SPI0_CSN1
C16	GPIO6_D[0]	D16	GPIO6_C[4]
C17	NP	D17	NP

C18	GPIO2_C[5]/SPI1_CSN0	D18	GPIO2_C[6]/SPI1_TXD
C19	GPIO2_C[3]/SPI0_RXD	D19	GPIO3_C[3]
C20	VDDIO3	D20	NP
C21	GPIO5_B[3]/HSADC_DATA6	D21	NP
C22	GPIO5_A[5]/HSADC_DATA0	D22	GPIO5_B[4]/HSADC_DATA7
C23	GPIO4_C[7]/RMII_RXD0/MII_RXD0	D23	GPIO4_C[5]/RMII_CRS_DVALID/MII_RXD_VALID
C24	NP	D24	GPIO4_C[2]/RMII_TXD1/MII_TXD1
E1	GPIO6_A[5]	F1	NP
E2	GPIO6_B[3]	F2	GPIO5_A[2]
E3	GPIO5_A[0]	F3	GPIO0_A[1]
E4	NP	F4	GPIO0_A[3]
E5	NP	F5	NP
E6	NP	F6	AHVDD_APLL
E7	GPIO6_B[1]	F7	AHVSS_APLL
E8	NP	F8	NP
E9	GPIO2_A[7]/UART2_RTS_N	F9	GPIO3_A[5]/I2S1_LRCK_TX
E10	GPIO6_B[6]	F10	GPIO3_A[0]/I2S1_CLK
E11	NP	F11	NP
E12	GPIO1_B[5]/PWM0	F12	GPIO2_A[3]/SDMMC0_WRITE_PRT/PWM2/UART1_SIR_OUT
E13	GPIO4_D[5]	F13	GPIO4_D[1]
E14	NP	F14	NP
E15	GPIO6_C[7]	F15	GPIO4_A[6]/HOST20_DRV_VBUS
E16	GPIO4_A[7]/SPDIF_TX	F16	GPIO2_C[1]/SPI0_CSN0
E17	NP	F17	NP
E18	GPIO2_C[0]/SPI0_CLK	F18	GPIO3_C[6]
E19	NP	F19	GPIO3_D[0]
E20	NP	F20	NP
E21	NP	F21	GPIO5_A[3]/MII_TX_CLKIN
E22	GPIO5_B[2]/HSADC_DATA5	F22	GPIO2_D[2]/I2S0_LRCK_RX/MII_TX_ERR
E23	GPIO4_D[6]/I2S0_LRCK_TX0	F23	GPIO2_D[6]/I2S0_SDO2/MII_TXD2
E24	GPIO4_C[0]/RMII_CLKOUT/RMII_CLKIN	F24	NP
G1	XOUT24M	H1	XOUT27M
G2	XIN24M	H2	XIN27M
G3	GND	H3	NP
G4	AVDD_PLL	H4	NP
G5	AVSS_PLL	H5	NP
G6	DVDD_PLL	H6	NP
G7	DVSS_PLL	H7	NP
G8	NP	H8	GPIO2_B[3]/UART3_SOUT
G9	GPIO5_D[2]/PWM1/UART1_SIR_IN	H9	GPIO2_B[7]/I2C0_SCL
G10	GPIO2_A[5]/UART1_SOUT	H10	VDDCORE
G11	NP	H11	VDDCORE
G12	GPIO5_D[4]/I2C2_SCL	H12	VDDCORE
G13	GPIO4_D[3]	H13	GPIO6_C[5]

G14	NP	H14	VDDIO4
G15	GPIO1_A[7]/I2C1_SCL	H15	GPIO6_C[1]
G16	GPIO5_D[7]	H16	GPIO6_D[1]
G17	NP	H17	GPIO3_C[5]
G18	GPIO5_B[6]/HSADC_DATA9/TS_FAIL	H18	NP
G19	GPIO4_C[3]/RMII_TXD0/MII_TXD0	H19	NP
G20	GPIO4_C[4]/RMII_RX_ERR/MII_RX_ERR	H20	NP
G21	GPIO4_C[6]/RMII_RXD1/MII_RXD1	H21	NP
G22	GPIO2_D[0]/I2S0_CLK/MII_RX_CLKIN	H22	NP
G23	GPIO2_A[0]/SDMMC0_DATA6	H23	GPIO1_D[4]/SDMMC0_DATA2
G24	GPIO2_D[4]/I2S0_SDO0/MII_RXD2	H24	GPIO1_D[6]/SDMMC0_DATA4
J1	NP	K1	DQ[2]
J2	TDI	K2	NPOR
J3	TMS	K3	TRST_N
J4	VDDIO0	K4	TCK
J5	GPIO4_A[4]	K5	TDO
J6	VDDIO5	K6	GPIO4_A[2]
J7	GPIO1_B[7]/UART0_SOUT	K7	GND
J8	GPIO3_A[3]/I2S1_SDI	K8	DVDDR
J9	VDDCORE	K9	NP
J10	NP	K10	GND
J11	NP	K11	GND
J12	VDDCORE	K12	GND
J13	VDDCORE	K13	GND
J14	NP	K14	GND
J15	NP	K15	GND
J16	GPIO6_C[3]	K16	NP
J17	GPIO3_A[6]	K17	GPIO2_C[4]/SPI1_CLK
J18	GPIO2_D[1]/I2S0_SCLK/MII_CRS	K18	GPIO2_D[5]/I2S0_SDO1/MII_RXD3
J19	GPIO4_D[7]/I2S0_LRCK_TX1	K19	GPIO2_D[3]/I2S0_SDI/MII_COL
J20	GPIO4_C[1]/RMII_TX_EN/MII_TX_EN	K20	GPIO2_D[7]/I2S0_SDO3/MII_TXD3
J21	GPIO1_D[5]/SDMMC0_DATA3	K21	GPIO2_A[1]/SDMMC0_DATA7
J22	GPIO1_D[0]/SDMMC0_CLKOUT	K22	VDDIO2
J23	GPIO1_D[2]/SDMMC0_DATA0	K23	GPIO1_C[4]/SDMMC1_DATA1
J24	NP	K24	GPIO1_C[6]/SDMMC1_DATA3
L1	DQ[17]	M1	NP
L2	DQ[16]	M2	DQ[19]
L3	DQ[3]	M3	DQ[18]
L4	NP	M4	DQ[1]
L5	NP	M5	DQ[0]
L6	NP	M6	DM[0]
L7	NP	M7	VREF0
L8	GND	M8	DVDDR
L9	NP	M9	VDDCORE
L10	GND	M10	GND

L11	GND	M11	GND
L12	GND	M12	GND
L13	GND	M13	GND
L14	GND	M14	GND
L15	GND	M15	GND
L16	NP	M16	VDDCORE
L17	GPIO0_A[7]/MII_MDCLK	M17	GPIO3_D[3]
L18	NP	M18	GPIO0_D[3]/FLASH_CSN2
L19	NP	M19	GPIO1_D[7]/SDMMC0_DATA5
L20	NP	M20	GPIO1_C[5]/SDMMC1_DATA2
L21	NP	M21	GPIO0_D[7]/FLASH_CSN6
L22	GPIO3_B[4]/EMMC_DATA2	M22	GPIO3_B[2]/EMMC_DATA0
L23	GPIO3_C[0]/EMMC_DATA6	M23	GPIO3_B[6]/EMMC_DATA4
L24	GPIO1_C[2]/SDMMC1_CMD	M24	NP
N1	NP	P1	DQ[20]
N2	DQS_B[2]	P2	DQ[21]
N3	DQS[2]	P3	DM[2]
N4	DQ[4]	P4	NP
N5	DQS_B[0]	P5	NP
N6	DQS[0]	P6	NP
N7	DVDDR	P7	NP
N8	GND	P8	DVDDR
N9	GND	P9	NP
N10	GND	P10	GND
N11	GND	P11	GND
N12	GND	P12	GND
N13	GND	P13	GND
N14	GND	P14	GND
N15	GND	P15	GND
N16	VDDCORE	P16	NP
N17	GPIO6_D[3]	P17	GPIO5_B[7]/HSADC_CLKOUT/GPS_CLK
N18	FLASH_WRN	P18	NP
N19	GPIO1_D[3]/SDMMC0_DATA1	P19	NP
N20	GPIO1_C[3]/SDMMC1_DATA0	P20	NP
N21	FLASH_CLE	P21	NP
N22	FLASH_WP	P22	FLASH_DATA[5]
N23	GPIO3_B[1]/EMMC_CMD	P23	FLASH_DATA[3]
N24	NP	P24	FLASH_DATA[4]
R1	DQ[22]	T1	NP
R2	DQ[23]	T2	ZQ_PIN
R3	BA[0]	T3	BA[1]
R4	DQ[7]	T4	BA[2]
R5	DQ[6]	T5	A[1]
R6	DQ[5]	T6	A[0]
R7	DVDDR	T7	VREF1

R8	GND	T8	DVDDR
R9	NP	T9	GND
R10	GND	T10	NP
R11	GND	T11	NP
R12	GND	T12	VDDCORE
R13	GND	T13	VDDCORE
R14	GND	T14	NP
R15	GND	T15	NP
R16	NP	T16	VDDCORE
R17	GPIO5_B[0]/HSADC_DATA3	T17	GPIO5_A[6]/HSADC_DATA1
R18	GPIO3_B[5]/EMMC_DATA3	T18	GPIO1_D[1]/SDMMC0_CMD
R19	GPIO3_B[7]/EMMC_DATA5	T19	FLASH_RDY
R20	GPIO3_B[0]/EMMC_CLKOUT	T20	GPIO3_B[3]/EMMC_DATA1
R21	GPIO0_D[5]/FLASH_CSN4	T21	GPIO0_D[6]/FLASH_CSN5
R22	GPIO0_A[5]/FLASH_DQS	T22	FLASH_DATA[7]
R23	FLASH_DATA[1]	T23	EFUSE_VQPS
R24	FLASH_DATA[2]	T24	NP
U1	CS_B0	V1	CK_B
U2	CKE0	V2	CK
U3	NP	V3	VREF_IN
U4	NP	V4	A[2]
U5	NP	V5	CKE1
U6	NP	V6	RESET
U7	NP	V7	DQ[11]
U8	GND	V8	NP
U9	DVDDR	V9	VREF2
U10	GND	V10	DVDDR
U11	VDDIO_LCD0	V11	NP
U12	VDDIO_LCD1	V12	LCDC_DEN
U13	LCDC_DATA[21]	V13	LCDC_DATA[15]
U14	VIP_DATAIN[7]	V14	NP
U15	VIP_DATAIN[11]	V15	LCDC_DATA[23]
U16	VDDIO1	V16	GPIO1_B[4]/VIP_CLKOUT
U17	GPIO1_C[7]/SDMMC1_CLKOUT	V17	NP
U18	NP	V18	GPIO1_A[0]/FLASH_CSN7/MDDR_TQ
U19	NP	V19	FLASH_DATA[6]
U20	NP	V20	GPIO0_D[2]/FLASH_CSN1
U21	NP	V21	FLASH_RDN
U22	NP	V22	FLASH_ALE
U23	HOST20_VSSAC	V23	HOST20_DVDD
U24	FLASH_DATA[0]	V24	HOST20_DVSS
W1	NP	Y1	ODT0
W2	CS_B1	Y2	WE_B
W3	A[3]	Y3	A[6]
W4	A[4]	Y4	NP

W5	NP	Y5	NP
W6	DQ[8]	Y6	NP
W7	DM[1]	Y7	DQS_B[1]
W8	NP	Y8	NP
W9	DQ[12]	Y9	DQ[13]
W10	LCDC_DATA[3]	Y10	LCDC_DATA[1]
W11	NP	Y11	NP
W12	LCDC_DATA[9]	Y12	LCDC_DCLK
W13	LCDC_DATA[17]	Y13	LCDC_DATA[13]
W14	NP	Y14	NP
W15	VIP_DATAIN[5]	Y15	VIP_HREF
W16	GPIO1_B[1]/VIP_DATAIN[1]	Y16	GPIO1_B[3]/VIP_DATAIN[3]
W17	NP	Y17	NP
W18	GPIO3_C[1]/EMMC_DATA7	Y18	SARADC_AIN[1]
W19	VDDA_SARADC	Y19	NP
W20	NP	Y20	NP
W21	OTG0_ID	Y21	NP
W22	OTG0_VSSA	Y22	OTG0_VDD33
W23	HOST20_VSSA	Y23	HOST20_VDD33
W24	NP	Y24	HOST20_VDD25
AA1	RAS_B	AB1	NP
AA2	CAS_B	AB2	ODT1
AA3	A[5]	AB3	A[11]
AA4	NP	AB4	A[14]
AA5	NP	AB5	DQ[9]
AA6	DQ[10]	AB6	DQ[25]
AA7	DQS[1]	AB7	DM[3]
AA8	NP	AB8	NP
AA9	DQ[14]	AB9	DQ[15]
AA10	LCDC_DATA[4]	AB10	LCDC_DATA[0]
AA11	NP	AB11	LCDC_DATA[6]
AA12	LCDC_DATA[7]	AB12	LCDC_DATA[5]
AA13	LCDC_DATA[11]	AB13	LCDC_DATA[14]
AA14	NP	AB14	LCDC_DATA[20]
AA15	LCDC_DATA[19]	AB15	VIP_DATAIN[10]
AA16	VIP_DATAIN[9]	AB16	VDDIO_VIP
AA17	NP	AB17	NP
AA18	SARADC_AIN[3]	AB18	GPIO1_B[2]/VIP_DATAIN[2]
AA19	FLASH_CSN0	AB19	VDDIO_FLASH0
AA20	NP	AB20	GPIO0_D[4]/FLASH_CSN3
AA21	NP	AB21	OTG0_VBUS
AA22	OTG0_DVSS	AB22	SARADC_AIN[0]
AA23	OTG0_DVDD	AB23	OTG0_VSSAC
AA24	HOST20_RKELVIN	AB24	NP
AC1	A[7]	AD1	A[8]

AC2	A[9]	AD2	A[10]
AC3	A[15]	AD3	NP
AC4	A[13]	AD4	A[12]
AC5	DQ[26]	AD5	DQ[27]
AC6	DQ[24]	AD6	NP
AC7	DQS_B[3]	AD7	DQS[3]
AC8	DQ[28]	AD8	DQ[29]
AC9	DQ[30]	AD9	NP
AC10	LCDC_DATA[2]	AD10	DQ[31]
AC11	LCDC_HSYNC	AD11	LCDC_VSYNC
AC12	LCDC_DATA[8]	AD12	NP
AC13	LCDC_DATA[10]	AD13	NP
AC14	LCDC_DATA[16]	AD14	LCDC_DATA[12]
AC15	VIP_DATAIN[4]	AD15	LCDC_DATA[18]
AC16	VIP_DATAIN[6]	AD16	NP
AC17	VIP_VSYNC	AD17	LCDC_DATA[22]
AC18	VIP_CLKIN	AD18	VIP_DATAIN[8]
AC19	GPIO1_B[0]/VIP_DATAIN[0]	AD19	NP
AC20	OTG0_VDD25	AD20	OTG0_RKELVIN
AC21	OTG0_DP	AD21	OTG0_DM
AC22	SARADC_AIN[2]	AD22	NP
AC23	HOST20_DP	AD23	HOST20_DM
AC24	USBHOST_DP	AD24	USBHOST_DN

2.3 RK2908 power/ground IO descriptions

Table 2-2 RK2908 Power/Ground IO informations

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	G3，L8，L10，L11，L12，L13，L14，L15，N8，N9，N10，N11，N12，N13，N14，N15，R8，R10，R11，R12，R13，R14，R15，U8，U10，K7，K10，K11，K12，K13，K14，K15，M10，M11，M12，M13，M14，M15，P10，P11，P12，P13，P14，P15，T9，		0		Internal Core Ground and DDR IO，digital IO Ground
VDDCORE	J9，J12，J13，N16，H10，H11，H12，M9，M16，T12，T13，T16，	1.08	1.2	1.32	Internal Core Power (@ CPU frequency <= 1GHz)
VDDIO1,VDDIO2,VDDI	J4,U16,K22,C20,H14,J6	3	3.3	3.6	Digital GPIO，USB11 HOST Power

O3,VDDIO4,VDDIO5		1.62	1.8	1.98	
VDDIO_LCD0	U11	3 1.62	3.3 1.8	3.6 1.98	LCDC Digital IO Power
VDDIO_LCD1	U12	3 1.62	3.3 1.8	3.6 1.98	
VDDIO_VIP	AB16	3 1.62	3.3 1.8	3.6 1.98	Camera Digital IO Power
VDDIO_FLASH0	AB19	3 1.62	3.3 1.8	3.6 1.98	Nand Flash Digital IO Power
VDDR	N7，R7，U9，K8，M8，P8，T8，V10，	1.7 1.65	1.8 1.8	1.9 1.95	DDRII，LPDDR IO Power
AHVDD_APLL	F6	2.25	2.5	2.75	ARM PLL(1.6GHz) Analog Power
AHVSS_APLL	F7		0		ARM PLL(1.6GHz) Analog Ground
AVDD_DPLL	G4	1.08	1.2	1.32	DDR PLL(1.0GHz) Analog Power
AVSS_DPLL	G5		0		DDR PLL(1.0GHz) Analog Ground
DVDD_DPLL	G6	1.08	1.2	1.32	DDR PLL Digital Power
DVSS_DPLL	G7		0		DDR PLL Digital Ground
VDDA_SARADC	W19	2.25	2.5	2.75	SAR-ADC Analog Power
OTG0_VSSAC	AB23		0		USB OTG Analog Ground
OTG0_DVSS	AA22		0		USB OTG Digital Ground
OTG0_DVDD	AA23	1.116	1.2	1.32	USB OTG Digital Power
OTG0_VDD25	AC20	2.325	2.5	2.75	USB OTG Analog Power
OTG0_VSSA	W22		0		USB OTG Analog Ground
OTG0_VDD33	Y22	3.069	3.3	3.63	USB OTG Analog Power
HOST20_VDD33	Y23	3.069	3.3	3.63	USB Host2.0 Analog Power
HOST20_VSSA	W23		0		USB Host2.0 Analog Ground
HOST20_VDD25	Y24	2.325	2.5	2.75	USB Host2.0 Analog Power
HOST20_DVDD	V23	1.116	1.2	1.32	USB Host2.0 Digital Power
HOST20_DVSS	V24		0		USB Host2.0 Digital Ground
HOST20_VSSAC	U23		0		USB Host2.0 Analog Ground

2.3.1 RK2908 function IO descriptions

Table 2-3 RK2908 IO descriptions

Power supply⑤	Pin Name	func0	func1	func2	func3	Pad types①	Drive②	pull up/down	Reset state⑨
PLL Domain	AHVSS_APLL	Analog Ground				AG	N/A	N/A	N/A
	AHVDD_APLL	2.5V				AP	N/A	N/A	N/A
	AVSS_DPLL	Analog Ground				AG	N/A	N/A	N/A
	AVDD_DPLL	1.2V				AP	N/A	N/A	N/A
	DVDD_DPLL	1.2V				DP	N/A	N/A	N/A
	DVSS_DPLL	Digital Ground				DG	N/A	N/A	N/A
VDDR	DQ[0:31]	DQ[0]				I/O	N/A	N/A	I
	A[0:14]	A[0]				O	N/A	N/A	O
	DM[0]	DM[0]				O	N/A	N/A	O
	DM[1]	DM[1]				O	N/A	N/A	O
	DM[2]	DM[2]				O	N/A	N/A	O
	DM[3]	DM[3]				O	N/A	N/A	O
	BA[0]	BA[0]				O	N/A	N/A	O
	BA[1]	BA[1]				O	N/A	N/A	O
	BA[2]	BA[2]				O	N/A	N/A	O
	DQS_B[0]	DQS_b[0]				I/O	N/A	N/A	I
	DQS_B[1]	DQS_b[1]				I/O	N/A	N/A	I
	DQS_B[2]	DQS_B[2]				I/O	N/A	N/A	I
	DQS_B[3]	DQS_B[3]				I/O	N/A	N/A	I
	DQS[0]	DQS[0]				I/O	N/A	N/A	I
	DQS[1]	DQS[1]				I/O	N/A	N/A	I
	DQS[2]	DQS[2]				I/O	N/A	N/A	I
	DQS[3]	DQS[3]				I/O	N/A	N/A	I
	VREF0	VREF4				DP	N/A	N/A	N/A
	VREF1	VREF4				DP	N/A	N/A	N/A
	VREF2	VREF				DP	N/A	N/A	N/A

	ZQ_PIN	ZQ_PIN				A	N/A	N/A	N/A
	VREF_IN	VREF_IN				I	N/A	N/A	I
	CKE0	CKE0				O	N/A	N/A	O
	CKE1	CKE1				O	N/A	N/A	O
	CS_B0	CS_B0				O	N/A	N/A	O
	CS_B1	CS_B1				O	N/A	N/A	O
	CK	CK				O	N/A	N/A	O
	CK_B	CK_B				O	N/A	N/A	O
	ODT0	ODT0				O	N/A	N/A	O
	ODT1	ODT1				O	N/A	N/A	O
	WE_B	WE_B				O	N/A	N/A	O
	RAS_B	RAS_B				O	N/A	N/A	O
	CAS_B	CAS_B				O	N/A	N/A	O
	RESET	RESET				O	N/A	N/A	O
VDDIO_LCD0 VDDIO_LCD1	LCDC_DATA[0:23]	LCDC_DATA[0]				I/O	12	Down	I Down
	LCDC_HSYNC	LCDC_HSYNC				O	12	Down	O Down
	LCDC_DCLK	LCDC_DCLK				O	12	Down	O Down
	LCDC_VSYNC	LCDC_VSYNC				I/O	12	Down	I Down
	LCDC_DEN	LCDC_DEN				I/O	12	Down	I Down
VDDIO_VIP	VIP_DATAIN[4:11]	VIP_DATAIN[4]				I	8	Down	I Down
	VIP_VSYNC	VIP_VSYNC				I	8	Down	I Down
	VIP_HREF	VIP_HREF				I	8	Down	I Down
	VIP_CLKIN	VIP_CLKIN				I	8	Down	I Down
	GPIO1_B[4]	GPIO1_B[4]	vip_clkout			I/O	12	Down	I Down
	GPIO1_B[0]	GPIO1_B[0]	vip_data0			I/O	8	Down	I Down
	GPIO1_B[1]	GPIO1_B[1]	vip_data1			I/O	8	Down	I Down
	GPIO1_B[2]	GPIO1_B[2]	vip_data2			I/O	8	Down	I Down
	GPIO1_B[3]	GPIO1_B[3]	vip_data3			I/O	8	Down	I Down
SARADC Domain	SARADC_AIN[0]	SARADC_AIN[0]				A	N/A	N/A	N/A

	SARADC_AIN[1]	SARADC_AIN[1]				A	N/A	N/A	N/A
	SARADC_AIN[2]	SARADC_AIN[2]				A	N/A	N/A	N/A
	SARADC_AIN[3]	SARADC_AIN[3]				A	N/A	N/A	N/A
	VDDA_SARADC	SARADC power supply and reference voltage input 2.5V				AP	N/A	N/A	N/A
USB OTG2.0 Domain	OTG0_VSSAC	Analog Ground				AG	N/A	N/A	N/A
	OTG0_DVSS	Digital Ground				DG	N/A	N/A	N/A
	OTG0_DVDD	1.2V				DP	N/A	N/A	N/A
	OTG0_VDD25	2.5V				AP	N/A	N/A	N/A
	OTG0_DM	OTG0_DM				A	N/A	N/A	N/A
	OTG0_RKELVIN	OTG0_RKELVIN				A	N/A	N/A	N/A
	OTG0_DP	OTG0_DP				A	N/A	N/A	N/A
	OTG0_VSSA	Analog Ground				AG	N/A	N/A	N/A
	OTG0_VBUS	OTG0_VBUS				A	N/A	N/A	N/A
	OTG0_VDD33	3.3V				AP	N/A	N/A	N/A
	OTG0_ID	OTG0_ID				A	N/A	N/A	N/A
	HOST20_VDD33	3.3V				AP	N/A	N/A	N/A
	HOST20_VSSA	Analog Ground				AG	N/A	N/A	N/A
	HOST20_DP	HOST20_DP				A	N/A	N/A	N/A
	HOST20_RKELVIN	HOST20_RKELVIN				A	N/A	N/A	N/A
	HOST20_DM	HOST20_DM				A	N/A	N/A	N/A
	HOST20_VDD25	2.5V				AP	N/A	N/A	N/A
	HOST20_DVDD	1.2V				DP	N/A	N/A	N/A
	HOST20_DVSS	Digital Ground				DG	N/A	N/A	N/A
	HOST20_VSSAC	Analog Ground				AG	N/A	N/A	N/A
VDDIO1 Domain	USBHOST_DN	USBHOST_DN				A	N/A	N/A	N/A
	USBHOST_DP	USBHOST_DP				A	N/A	N/A	N/A
	EFUSE_VQPS	EFUSE_VQPS				A	N/A	N/A	N/A
VDDIO_FLASH0	FLASH_DATA[0:7]	FLASH_DATA[0:7]				I/O	8	Down	I Down

	FLASH_RDY	FLASH_RDY				I	8	Up	I Up
	FLASH_ALE	FLASH_ALE				O	8	Down	O Down
	FLASH_CLE	FLASH_CLE				O	8	Down	O Down
	FLASH_RDN	FLASH_RDN				O	8	Up	O Up
	FLASH_WRN	FLASH_WRN				O	8	Up	O Up
	FLASH_WP	FLASH_WP				O	8	Down	O Down
	FLASH_CSN0	FLASH0_CSN				O	8	Up	O Up
	GPIO0_D[2]	GPIO0_D[2]	flash_csn1			I/O	8	Up	I Up
	GPIO0_D[3]	GPIO0_D[3]	flash_csn2			I/O	8	Up	I Up
	GPIO0_D[4]	GPIO0_D[4]	flash_csn3			I/O	8	Up	I Up
	GPIO0_D[5]	GPIO0_D[5]	flash_csn4			I/O	8	Up	I Up
	GPIO0_D[6]	GPIO0_D[6]	flash_csn5			I/O	8	Up	I Up
	GPIO0_D[7]	GPIO0_D[7]	flash_csn6			I/O	8	Up	I Up
	GPIO1_A[0]	GPIO1_A[0]	flash_csn7	mddr_tq		I/O	8	Up	I Up
	GPIO0_A[5]	GPIO0_A[5]	flash_dqs			I/O	8	Up	I Up
VDDIO	XIN24M	XIN24M				I	N/A	N/A	I
	XOUT24M	XOUT24M				O	N/A	N/A	O
	XIN27M	XIN27M				I	N/A	N/A	I
	XOUT27M	XOUT27M				O	N/A	N/A	O
	TRST_N	TRST_N				I	8	Down	I Down
	TDI	TDI				I	8	Up	I Up
	TCK	TCK				I	8	Up	I Up
	TMS	TMS				I/O	8	Up	I Up
	TDO	TDO				O	8	Down	O Down
	RECOVER	System recover input, high input				I	N/A	Down	I Down
	REF_OUT	DDR reference voltage output				I/O	N/A	N/A	N/A
	NPOR	NPOR				I	8	Down	I Down
	GPIO3_B[1]	GPIO3_B[1]	emmc_cmd			I/O	8	Up	I Up

GPIO3_B[0]	GPIO3_B[0]	emmc_clkout			I/O	12	Down	I Down
GPIO3_B[2]	GPIO3_B[2]	emmc_data0			I/O	8	Up	I Up
GPIO3_B[3]	GPIO3_B[3]	emmc_data1			I/O	8	Up	I Up
GPIO3_B[4]	GPIO3_B[4]	emmc_data2			I/O	8	Up	I Up
GPIO3_B[5]	GPIO3_B[5]	emmc_data3			I/O	8	Up	I Up
GPIO3_B[6]	GPIO3_B[6]	emmc_data4			I/O	8	Up	I Up
GPIO3_B[7]	GPIO3_B[7]	emmc_data5			I/O	8	Up	I Up
GPIO3_C[0]	GPIO3_C[0]	emmc_data6			I/O	8	Up	I Up
GPIO3_C[1]	GPIO3_C[1]	emmc_data7			I/O	8	Up	I Up
GPIO1_C[2]	GPIO1_C[2]	sdio_cmd			I/O	8	Up	I Up
GPIO1_C[3]	GPIO1_C[3]	sdio_data0			I/O	8	Up	I Up
GPIO1_C[4]	GPIO1_C[4]	sdio_data1			I/O	8	Up	I Up
GPIO1_C[5]	GPIO1_C[5]	sdio_data2			I/O	8	Up	I Up
GPIO1_C[6]	GPIO1_C[6]	sdio_data3			I/O	8	Up	I Up
GPIO1_C[7]	GPIO1_C[7]	sdio_clkout			I/O	12	Down	I Down
GPIO1_D[0]	GPIO1_D[0]	sdmmc_clkout			I/O	12	Down	I Down
GPIO1_D[1]	GPIO1_D[1]	sdmmc_cmd			I/O	8	Up	I Up
GPIO1_D[2]	GPIO1_D[2]	sdmmc_data0			I/O	8	Up	I Up
GPIO1_D[3]	GPIO1_D[3]	sdmmc_data1			I/O	8	Up	I Up
GPIO1_D[4]	GPIO1_D[4]	sdmmc_data2			I/O	8	Up	I Up
GPIO1_D[5]	GPIO1_D[5]	sdmmc_data3			I/O	8	Up	I Up
GPIO1_D[6]	GPIO1_D[6]	sdmmc_data4			I/O	8	Up	I Up
GPIO1_D[7]	GPIO1_D[7]	sdmmc_data5			I/O	8	Up	I Up
GPIO2_A[0]	GPIO2_A[0]	sdmmc_data6			I/O	8	Up	I Up
GPIO2_A[1]	GPIO2_A[1]	sdmmc_data7			I/O	8	Up	I Up
GPIO2_D[0]	GPIO2_D[0]	i2s0_clk	mii_rx_clkin		I/O	12	Down	I Down
GPIO2_D[1]	GPIO2_D[1]	i2s0_sclk	mii_crs		I/O	8	Down	I Down
GPIO2_D[2]	GPIO2_D[2]	i2s0_lrck_rx	mii_tx_err		I/O	8	Down	I Down
GPIO2_D[3]	GPIO2_D[3]	i2s0_sdi	mii_col		I/O	8	Down	I Down

GPIO2_D[4]	GPIO2_D[4]	i2s0_sdo0	mii_rxd2		I/O	8	Down	I Down
GPIO2_D[5]	GPIO2_D[5]	i2s0_sdo1	mii_rxd3		I/O	8	Down	I Down
GPIO2_D[6]	GPIO2_D[6]	i2s0_sdo2	mii_txd2		I/O	8	Down	I Down
GPIO2_D[7]	GPIO2_D[7]	i2s0_sdo3	mii_txd3		I/O	8	Down	I Down
GPIO4_D[6]	GPIO4_D[6]	i2s0_lrck_tx0			I/O	8	Down	I Down
GPIO4_D[7]	GPIO4_D[7]	i2s0_lrck_tx1			I/O	8	Down	I Down
GPIO4_C[0]	GPIO4_C[0]	rmii_clkout	rmii_clkin		I/O	12	Down	I Down
GPIO4_C[1]	GPIO4_C[1]	rmii_tx_en	mii_tx_en		I/O	8	Down	I Down
GPIO4_C[2]	GPIO4_C[2]	rmii_txd1	mii_txd1		I/O	8	Down	I Down
GPIO4_C[3]	GPIO4_C[3]	rmii_txd0	mii_txd0		I/O	8	Down	I Down
GPIO4_C[5]	GPIO4_C[5]	rmii_crs_dvalid	mii_rxd_valid		I/O	8	Down	I Down
GPIO4_C[6]	GPIO4_C[6]	rmii_rxd1	mii_rxd1		I/O	8	Down	I Down
GPIO4_C[7]	GPIO4_C[7]	rmii_rxd0	mii_rxd0		I/O	8	Down	I Down
GPIO5_A[3]	GPIO5_A[3]	mii_tx_clkin			I/O	8	Up	I Up
GPIO5_A[5]	GPIO5_A[5]	hsadc_data0			I/O	8	Down	I Down
GPIO5_A[6]	GPIO5_A[6]	hsadc_data1			I/O	8	Down	I Down
GPIO5_A[7]	GPIO5_A[7]	hsadc_data2			I/O	8	Down	I Down
GPIO5_B[0]	GPIO5_B[0]	hsadc_data3			I/O	8	Down	I Down
GPIO5_B[1]	GPIO5_B[1]	hsadc_data4			I/O	8	Down	I Down
GPIO5_B[2]	GPIO5_B[2]	hsadc_data5			I/O	8	Down	I Down
GPIO5_B[3]	GPIO5_B[3]	hsadc_data6			I/O	8	Down	I Down
GPIO5_B[4]	GPIO5_B[4]	hsadc_data7			I/O	8	Down	I Down
GPIO5_B[5]	GPIO5_B[5]	hsadc_data8/ts_valid			I/O	8	Down	I Down
GPIO5_B[6]	GPIO5_B[6]	hsadc_data9/ts_fail			I/O	8	Down	I Down
GPIO5_A[4]	GPIO5_A[4]	ts_sync			I/O	8	Down	I Down
GPIO5_B[7]	GPIO5_B[7]	hsadc_clkout	gps_clk		I/O	8	Down	I Down
GPIO3_C[3]	GPIO3_C[3]				I/O	8	Down	I Down
GPIO3_C[5]	GPIO3_C[5]				I/O	8	Down	I Down
GPIO3_C[2]	GPIO3_C[2]				I/O	8	Down	I Down

GPIO3_A[6]	GPIO3_A[6]				I/O	8	Down	I Down
GPIO3_A[7]	GPIO3_A[7]				I/O	8	Down	I Down
GPIO3_C[6]	GPIO3_C[6]				I/O	8	Down	I Down
GPIO3_C[7]	GPIO3_C[7]				I/O	8	Down	I Down
GPIO3_D[0]	GPIO3_D[0]				I/O	8	Down	I Down
GPIO3_D[1]	GPIO3_D[1]				I/O	8	Down	I Down
GPIO2_C[1]	GPIO2_C[1]	spi0_csn0			I/O	8	Up	I Up
GPIO2_C[2]	GPIO2_C[2]	spi0_txd			I/O	8	Down	I Down
GPIO2_C[0]	GPIO2_C[0]	spi0_clk			I/O	12	Down	I Down
GPIO2_C[3]	GPIO2_C[3]	spi0_rxd			I/O	8	Down	I Down
GPIO2_C[4]	GPIO2_C[4]	spi1_clk			I/O	12	Down	I Down
GPIO2_C[5]	GPIO2_C[5]	spi1_csn0			I/O	8	Up	I Up
GPIO2_C[6]	GPIO2_C[6]	spi1_txd			I/O	8	Down	I Down
GPIO2_C[7]	GPIO2_C[7]	spi1_rxd			I/O	8	Down	I Down
GPIO4_A[7]	GPIO4_A[7]	spdif_tx			I/O	8	Down	I Down
GPIO0_A[6]	GPIO0_A[6]	mii_md			I/O	8	Down	I Down
GPIO0_A[7]	GPIO0_A[7]	mii_mdclk			I/O	8	Down	I Down
GPIO3_D[2]	GPIO3_D[2]				I/O	8	Up	I Up
GPIO3_D[3]	GPIO3_D[3]				I/O	8	Up	I Up
GPIO3_D[4]	GPIO3_D[4]				I/O	8	Up	I Up
GPIO5_D[7]	GPIO5_D[7]				I/O	8	Up	I Up
GPIO6_D[0]	GPIO6_D[0]				I/O	8	Down	I Down
GPIO6_D[1]	GPIO6_D[1]				I/O	8	Down	I Down
GPIO6_D[2]	GPIO6_D[2]				I/O	8	Down	I Down
GPIO6_D[3]	GPIO6_D[3]				I/O	8	Down	I Down
GPIO6_C[0]	GPIO6_C[0]				I/O	8	Down	I Down
GPIO6_C[1]	GPIO6_C[1]				I/O	8	Down	I Down
GPIO6_C[2]	GPIO6_C[2]				I/O	8	Down	I Down
GPIO6_C[3]	GPIO6_C[3]				I/O	8	Down	I Down

GPIO6_C[4]	GPIO6_C[4]				I/O	8	Down	I Down
GPIO6_C[5]	GPIO6_C[5]				I/O	8	Down	I Down
GPIO6_C[6]	GPIO6_C[6]				I/O	8	Down	I Down
GPIO6_C[7]	GPIO6_C[7]				I/O	8	Down	I Down
GPIO1_A[6]	GPIO1_A[6]	i2c1_sda			I/O	8	Up	I Up
GPIO1_A[7]	GPIO1_A[7]	i2c1_scl			I/O	8	Up	I Up
GPIO4_A[5]	GPIO4_A[5]	otg0_drv_vbus			I/O	8	Down	I Down
GPIO4_A[6]	GPIO4_A[6]	HOST20_drv_vbus			I/O	8	Down	I Down
GPIO4_D[0]	GPIO4_D[0]				I/O	8	Up	I Up
GPIO4_D[1]	GPIO4_D[1]				I/O	8	Up	I Up
GPIO4_D[2]	GPIO4_D[2]				I/O	8	Up	I Up
GPIO4_D[3]	GPIO4_D[3]				I/O	8	Up	I Up
GPIO4_D[4]	GPIO4_D[4]	trace_clk			I/O	8	Down	I Down
GPIO4_D[5]	GPIO4_D[5]	trace_ctl			I/O	8	Down	I Down
GPIO1_A[3]	GPIO1_A[3]	emmc_detect_n	spi1_csn1		I/O	8	Up	I Up
GPIO1_A[4]	GPIO1_A[4]	emmc_write_prt	spi0_csn1		I/O	8	Up	I Up
GPIO1_A[5]	GPIO1_A[5]	emmc_pwr_en	pwm3		I/O	8	Down	I
GPIO1_B[5]	GPIO1_B[5]	pwm0			I/O	8	Down	I Down
GPIO2_A[2]	GPIO2_A[2]	sdmmc_detect_n			I/O	8	Up	I Up
GPIO2_A[3]	GPIO2_A[3]	sdmmc_write_prt	pwm2	uart1_sir_out_n	I/O	8	Down	I Down
GPIO2_A[4]	GPIO2_A[4]	uart1_sin			I/O	8	Down	I Down
GPIO2_A[5]	GPIO2_A[5]	uart1_sout			I/O	8	Down	I Down
GPIO2_B[6]	GPIO2_B[6]	i2c0_sda			I/O	8	Up	I Up
GPIO2_B[7]	GPIO2_B[7]	i2c0_scl			I/O	8	Up	I Up
GPIO5_D[3]	GPIO5_D[3]	i2c2_sda			I/O	8	Up	I Up
GPIO5_D[4]	GPIO5_D[4]	i2c2_scl			I/O	8	Up	I Up
GPIO6_B[5]	GPIO6_B[5]				I/O	8	Down	I Down
GPIO6_B[6]	GPIO6_B[6]				I/O	8	Down	I Down
GPIO6_B[7]	GPIO6_B[7]				I/O	8	Down	I Down

	GPIO5_D[2]	GPIO5_D[2]	pwm1	uart1_sir_in		I/O	8	Down	I Down
	GPIO5_D[5]	GPIO5_D[5]	sdmmc_pwr_en			I/O	8	Down	I Down
	GPIO5_D[6]	GPIO5_D[6]	sdio_pwr_en			I/O	8	Down	I Down
VDDIO	GPIO3_A[0]	GPIO3_A[0]	i2s1_clk			I/O	12	Down	I Down
	GPIO3_A[1]	GPIO3_A[1]	i2s1_sclk			I/O	8	Down	I Down
	GPIO3_A[2]	GPIO3_A[2]	i2s1_lrck_rx			I/O	8	Down	I Down
	GPIO3_A[3]	GPIO3_A[3]	i2s1_sdi			I/O	8	Down	I Down
	GPIO3_A[4]	GPIO3_A[4]	i2s1_sdo			I/O	8	Down	I Down
	GPIO3_A[5]	GPIO3_A[5]	i2s1_lrck_tx			I/O	8	Down	I Down
	GPIO2_A[6]	GPIO2_A[6]	uart2_cts_n			I/O	8	Up	I Up
	GPIO2_A[7]	GPIO2_A[7]	uart2_rts_n			I/O	8	Up	I Up
	GPIO2_B[0]	GPIO2_B[0]	uart2_sin			I/O	8	Down	I Down
	GPIO2_B[1]	GPIO2_B[1]	uart2_sout			I/O	8	Down	I Down
	GPIO2_B[2]	GPIO2_B[2]	uart3_sin			I/O	8	Down	I Down
	GPIO2_B[3]	GPIO2_B[3]	uart3_sout			I/O	8	Down	I Down
	GPIO2_B[4]	GPIO2_B[4]	uart3_cts_n	i2c3_sda		I/O	8	Up	I Up
	GPIO2_B[5]	GPIO2_B[5]	uart3_rts_n	i2c3_scl		I/O	8	Up	I Up
	GPIO1_B[6]	GPIO1_B[6]	uart0_sin			I/O	8	Down	I Down
	GPIO1_B[7]	GPIO1_B[7]	uart0_sout			I/O	8	Down	I Down
	GPIO1_C[0]	GPIO1_C[0]	uart0_cts_n	sdio_detect_n		I/O	8	Up	I Up
	GPIO1_C[1]	GPIO1_C[1]	uart0_rts_n	sdio_write_prt		I/O	8	Up	I Up
	GPIO6_A[0]	GPIO6_A[0]				I/O	8	Down	I Down
	GPIO6_A[1]	GPIO6_A[1]				I/O	8	Down	I Down
	GPIO6_A[2]	GPIO6_A[2]				I/O	8	Down	I Down
	GPIO6_A[3]	GPIO6_A[3]				I/O	8	Down	I Down
	GPIO6_A[4]	GPIO6_A[4]				I/O	8	Down	I Down
	GPIO6_A[5]	GPIO6_A[5]				I/O	8	Down	I Down
	GPIO6_A[6]	GPIO6_A[6]				I/O	8	Down	I Down
	GPIO6_A[7]	GPIO6_A[7]				I/O	8	Down	I Down

	GPIO6_B[0]	GPIO6_B[0]				I/O	8	Down	I Down
	GPIO6_B[1]	GPIO6_B[1]				I/O	8	Down	I Down
	GPIO6_B[2]	GPIO6_B[2]				I/O	8	Down	I Down
	GPIO6_B[3]	GPIO6_B[3]				I/O	8	Down	I Down
	GPIO6_B[4]	GPIO6_B[4]				I/O	8	Down	I Down
	GPIO5_A[0]	GPIO5_A[0]				I/O	8	Up	I Up
	GPIO5_A[1]	GPIO5_A[1]				I/O	8	Up	I Up
	GPIO5_A[2]	GPIO5_A[2]				I/O	8	Up	I Up
	GPIO0_A[0]	GPIO0_A[0]				I/O	8	Up	I Up
	GPIO0_A[1]	GPIO0_A[1]				I/O	8	Up	I Up
	GPIO0_A[2]	GPIO0_A[2]				I/O	8	Up	I Up
	GPIO0_A[3]	GPIO0_A[3]				I/O	8	Up	I Up
	GPIO0_A[4]	GPIO0_A[4]				I/O	8	Up	I Up
	GPIO4_A[1]	GPIO4_A[1]				I/O	8	Up	I Up
	GPIO4_A[2]	GPIO4_A[2]				I/O	8	Up	I Up
	GPIO4_A[3]	GPIO4_A[3]				I/O	8	Up	I Up
	GPIO4_A[4]	GPIO4_A[4]				I/O	8	Down	I Down

Notes :

①: Pad types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: Output Drive Unit is mA , only Digital IO have drive value

③: Reset state : I = input without any pull resistor , O = output without any pull resistor ,
I Up = input with weak pullup resistor , I Down = Input with weak pulldown resistor
O Up =output with weak pullup resistor ,O Down =output with weak pulldown resistor

④: It is die location. For examples, "Left side" means that all the related IOs are always in left side of die

⑤: Power supply means that all the related IOs is in these IO power domain. If multiple powers is included, they are connected together in one IO power ring

2.4 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 RK2908 IO function description list

Interface	Pin Name	Direction	Description
MISC	RECOVER	I	System recover input, when loader detect high input, system enter recover mode
	NPOR	I	Power on reset for chip

Interface	Pin Name	Direction	Description
Debug	TRST_N	I	JTAG interface reset input
	TCK	I	JTAG interface clock input/SWD interface clock input
	TDI	I	JTAG interface TDI input
	TMS	I/O	JTAG interface TMS input/SWD interface data out
	TDO	O	JTAG interface TDO output

Interface	Pin Name	Direction	Description
ETM Trace	trace_clk	O	Cortex-A8 ETM trace port clk
	trace_ctl	O	Cortex-A8 ETM trace port control
	trace_data*i*(*i*=0~7)	O	Cortex-A8 ETM trace port data

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	sdmmc_clkout	O	sdmmc card clock.
	sdmmc_cmd	I/O	sdmmc card command output and reponse input.
	sdmmc_data*i* (*i*=0~7)	I/O	sdmmc card data input and output.
	sdmmc_detect_n	I	sdmmc card detect signal, a 0 represents presence of card.
	sdmmc_write_prt	I	sdmmc card write protect signal, a 1 represents write is protected.
	sdmmc_pwr_en	O	sdmmc card power-enable control signal

Interface	Pin Name	Direction	Description
SDIO Host Controller	sdio_clkout	O	sdio card clock.
	sdio_cmd	I/O	sdio card command output and reponse input.
	sdio_data*i* (*i*=0~3)	I/O	sdio card data input and output.
	sdio_detect_n	I	sdio card detect signal, a 0 represents presence of card.
	sdio_write_prt	I	sdio card write protect signal, a 1 represents write is protected.
	sdio_pwr_en	O	sdio card power-enable control signal

Interface	Pin Name	Direction	Description
eMMC Interface	emmc_clkout	O	emmc card clock.
	emmc_cmd	I/O	emmc card command output and reponse input.
	emmc_data*i* (*i*=0~7)	I/O	emmc card data input and output.
	emmc_detect_n	I	emmc card detect signal, a 0 represents presence of card.
	emmc_write_prt	I	emmc card write protect signal, a 1 represents write is protected.
	emmc_pwr_en	O	emmc card power-enable control signal

Interface	Pin Name	Direction	Description
DMC	CK	O	Active-high clock signal to the memory device.
	CK_B	O	Active-low clock signal to the memory device.
	CKE*i* (*i*=0,1)	O	Active-high clock enable signal to the memory device for two chip select.
	CS_B*i* (*i*=0,1)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RAS_B	O	Active-low row address strobe to the memory device.
	CAS_B	O	Active-low column address strobe to the memory device.
	WE_B	O	Active-low write enable strobe to the memory device.
	BA[2:0]	O	Bank address signal to the memory device.
	A[15:0]	O	Address signal to the memory device.
	DQ[31:0]	I/O	Bidirectional data line to the memory device.
	DQS[3:0]	I/O	Active-high bidirectional data strobes to the memory device.
	DQS_B[3:0]	I/O	Active-low bidirectional data strobes to the memory device.
	DM[3:0]	O	Active-low data mask signal to the memory device.
	ODT*i* (*i*=0,1)	O	On-Die Termination output signal for two chip select.
	VREF_IN	I	DDR reference voltage input
	VREF*i* (*i*=0,1,2)	N/A	Reference Voltage input for three regions of DDR IO
	ZQ_PIN	N/A	ZQ calibration pad which connects 240ohm±1% resistor
	mddr_tq	I	LPDDR temperature output signal to DDR controller
	DLL_TEST_PIN[1:0]	O	DLL digital test output.
	ANALOG_TEST_PIN	N/A	DLL analog test output.

Interface	Pin Name	Direction	Description

NandC	IO_FLASH_WP	O	Flash write-protected signal
	IO_FLASH_ALE	O	Flash address latch enable signal
	IO_FLASH_CLE	O	Flash command latch enable signal
	IO_FLASH_WRN	O	Flash write enable and clock signal
	IO_FLASH_RDN	O	Flash read enable and write/read signal
	IO_FLASH_DATA[*i*](i=0~7)	I/O	Low 8bits of flash data inputs/outputs signal
	flash_data*i*(*i*=8~15)	I/O	High 8bits of flash data inputs/outputs signal
	flash_dqs	I/O	Flash data strobe signal
	IO_FLASH_RDY	I	Flash ready/busy signal
	IO_FLASH0_CSN	O	Flash chip enable signal for chip 0
	flash_csn*i*(*i*=1~7)	O	Flash chip enable signal for chip i, i=1~7

Interface	Pin Name	Direction	Description
HSADC Interface	hsadc_clkout	O	hsadc/tsi/gps reference clock
	hsadc_data*i* (*i*=0~9)	I	hsadc(i=0~9)/tsi(i=0~7)/gps data(i=0,1)
	ts_sync	I	ts synchronizer signal

Interface	Pin Name	Direction	Description
I2S/PCM0 Controller (8 channel)	i2s0_clk	O	I2S/PCM0 clock source
	i2s0_sclk	I/O	I2S/PCM0 serial clock
	i2s0_lrck_rx	I/O	I2S/PCM0 left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s0_sdi	I	I2S/PCM0 serial data input
	i2s0_sdo*i* *(i=0,1,2,3)*	O	I2S/PCM0 serial data ouput
	i2s0_lrck_tx*i* *(i=0,1)*	I/O*(i=0)* O(*i=1)*	I2S/PCM0 left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode *(i=0)* and the beginning of a group of left & right channels in PCM mode *(i=0,1)*

Interface	Pin Name	Direction	Description
I2S/PCM1 Controller (2 channel)	i2s1_clk	O	I2S/PCM1 clock source
	i2s1_sclk	I/O	I2S/PCM1 serial clock
	i2s1_lrck_rx	I/O	I2S/PCM1 left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s1_sdi	I	I2S/PCM1 serial data input
	i2s1_sdo	O	I2S/PCM1 serial data ouput
	i2s1_lrck_tx	I/O	I2S/PCM1 left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

Interface	Pin Name	Direction	Description
SPDIF transmitter	spdif_tx	O	spdif biphase data ouput

Interface	Pin Name	Direction	Description

SPI Controller	spi*x*_clk *(x=0,1)*	I/O	spi serial clock
	spi*x*_csn*y* *(x=0,1) (y=0,1)*	I/O	spi chip select signal,low active
	spi*x*_txd *(x=0,1)*	O	spi serial data output
	spi*x*_rxd *(x=0,1)*	I	spi serial data input

Interface	Pin Name	Direction	Description
LCDC	LCDC_DCLK	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	LCDC_VSYNC	O	LCDC RGB interface vertival sync pulse, MCU i80 interface CSN signal
	LCDC_HSYNC	O	LCDC RGB interface horizontial sync pulse, MCU i80 interface WEN signal
	LCDC_DEN	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	LCDC_DATA[23:0]	I/O	LCDC data output/input

Interface	Pin Name	Direction	Description
Camera IF	VIP_CLKIN	I	Camera interface input pixel clock
	vip_clkout	O	Camera interface output work clock
	VIP_VSYNC	I	Camera interface vertical sync signal
	VIP_HREF	I	Camera interface horizontial sync signal
	vip_data[3:0]	I	Camera interface low 4-bit input pixel data
	VIP_DATAIN[11:4]	I	Camera interface high 8-bit input pixel data

Interface	Pin Name	Direction	Description
MII/RMII	rmii_clkout	O	RMII REC_CLK output
	rmii_clkin	I	RMII REF_CLK input
	rmii_tx_en	O	rmii transfer enable
	rmii_txd1	O	rmii transfer data
	rmii_txd0	O	rmii transfer data
	rmii_rx_err	I	rmii receive error
	rmii_crs_dvalid	I	rmii carrier sense / receive data valid input
	rmii_rxd1	I	rmii receive data
	rmii_rxd0	I	rmii receive data
	mii_col	I	mii collision detect
	mii_crs	I	mii carrier sense detect
	mii_rx_clkin	I	mii receive clock from emac phy
	mii_rxd3	I	mii receive data
	mii_rxd2	I	mii receive data
	mii_rxd1	I	mii receive data
	mii_rxd0	I	mii receive data
	mii_rx_err	I	mii receive error
	mii_rxd_valid	I	mii receive data valid
	mii_tx_clkin	I	mii transfer clock from emac phy

	mii_txd3	O	mii transfer data
	mii_txd2	O	mii transfer data
	mii_txd1	O	mii transfer data
	mii_txd0	O	mii transfer data
	mii_tx_en	O	mii transfer data enable
	mii_tx_err	O	mii transfer error
	mii_md	I/O	mii management interface data
	mii_mdclk	O	mii management interface clock

Interface	Pin Name	Direction	Description
PWM	pwm3	I/O	Pulse Width Modulation output
	pwm2	I/O	Pulse Width Modulation output
	pwm1	I/O	Pulse Width Modulation output
	pwm0	I/O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock
	i2c1_sda	I/O	I2C1 data
	i2c1_scl	I/O	I2C1 clock
	i2c2_sda	I/O	I2C2 data
	i2c2_scl	I/O	I2C2 clock
	i2c3_sda	I/O	I2C3 data
	i2c3_scl	I/O	I2C3 clock

Interface	Pin Name	Direction	Description
UART	uart0_sin	I	UART0 searial data input
	uart0_sout	O	UART0 searial data output
	uart0_cts_n	I	UART0 clear to send
	uart0_rts_n	O	UART0 request to send
	uart1_sir_out_n	O	UART1 IRDA SIR data output
	uart1_sin	I	UART1 searial data input
	uart1_sout	O	UART1 searial data output
	uart1_sir_in	I	UART1 IRDA SIR data input
	uart2_cts_n	I	UART2 clear to send
	uart2_rts_n	O	UART2 request to send
	uart2_sin	I	UART2 searial data input
	uart2_sout	O	UART2 searial data output
	uart3_sin	I	UART3 searial data input
	uart3_sout	O	UART3 searial data output
	uart3_cts_n	I	UART3 clear to send
	uart3_rts_n	O	UART3 request to send

Interface	Pin Name	Direction	Description
USB OTG	OTG0_DM	N/A	USB OTG 2.0 Data signal DM
	OTG0_RKELVIN	N/A	USB OTG 2.0 Transmitter Kelvin Connection to

			Resistor Tune Pin
	OTG0_DP	N/A	USB OTG 2.0 Data signal DP
	OTG0_VBUS	N/A	USB OTG 2.0 5-V power supply pin
	otg0_drv_vbus	O	USB OTG 2.0 drive VBUS

Interface	Pin Name	Direction	Description
USB Host 2.0	HOST20_DM	N/A	USB HOST 2.0 Data signal DM
	HOST20_RKELVIN	N/A	USB HOST 2.0 Transmitter Kelvin Connection to Resistor Tune Pin
	HOST20_DP	N/A	USB HOST 2.0 Data signal DP
	HOST20_VBUS	N/A	USB HOST 2.0 5-V power supply pin
	HOST20_drv_vbus	O	USB HOST 2.0 drive VBUS

Interface	Pin Name	Direction	Description
USB Host 1.1	USBHOST_DN	N/A	UHOST DN data-line
	USBHOST_DP	N/A	UHOST DP data-line

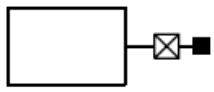
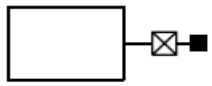
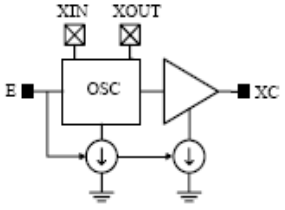
Interface	Pin Name	Direction	Description
SAR-ADC	SARADC_AIN[i] (i=0~3)	N/A	SAR-ADC input signal for 4 channel

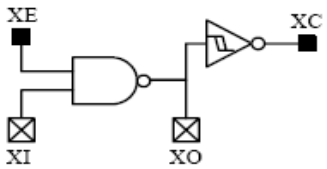
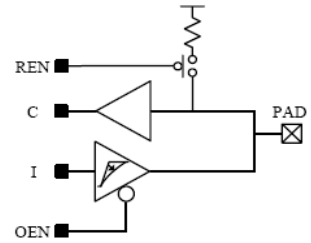
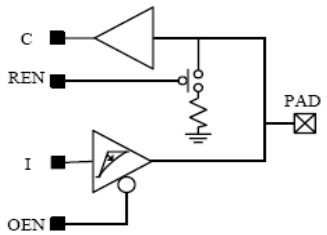
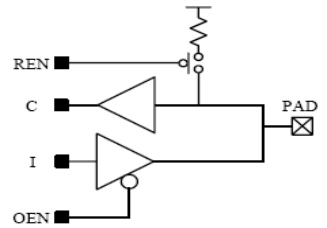
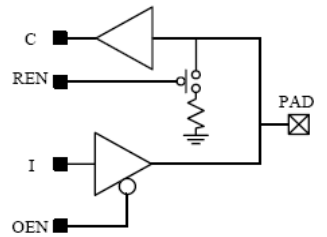
Interface	Pin Name	Direction	Description
eFuse	EFUSE_VQPS	N/A	eFuse program and sense power

2.4.1 RK2908 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO .

Table 2-5 RK2908 IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VQPS
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[3:0]
C		32.768KHz Crystal Oscillator IO with high enable	XIN32K/XOUT32K

D		Crystal Oscillator with high enable	XIN24M/XOUT24M XIN27M/XOUT27M
E		Tri-state output pad with input, limited slew rate and enable controlled pull-up	Part of digital GPIO
F		Tri-state output pad with input, limited slew rate and enable controlled pull-down	Part of digital GPIO
G		Tri-state output pad with input, and enable controlled pull-up	Part of digital GPIO
H		Tri-state output pad with input, and enable controlled pull-down	Part of digital GPIO

2.5 Package information

RK2908 package is TFBGA432
(Body: 16mm x 16mm; ball size: 0.3mm; ball pitch: 0.65mm)

2.5.1 Dimension

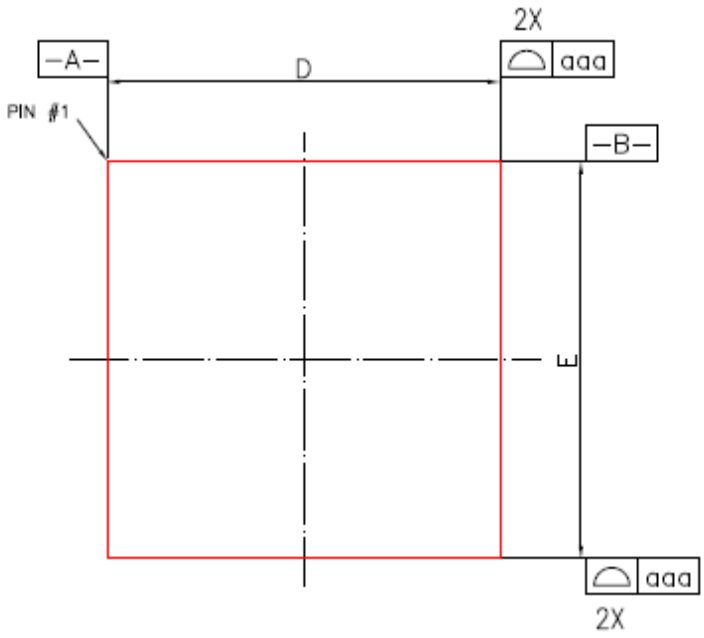


Fig. 2-2 Package Top View

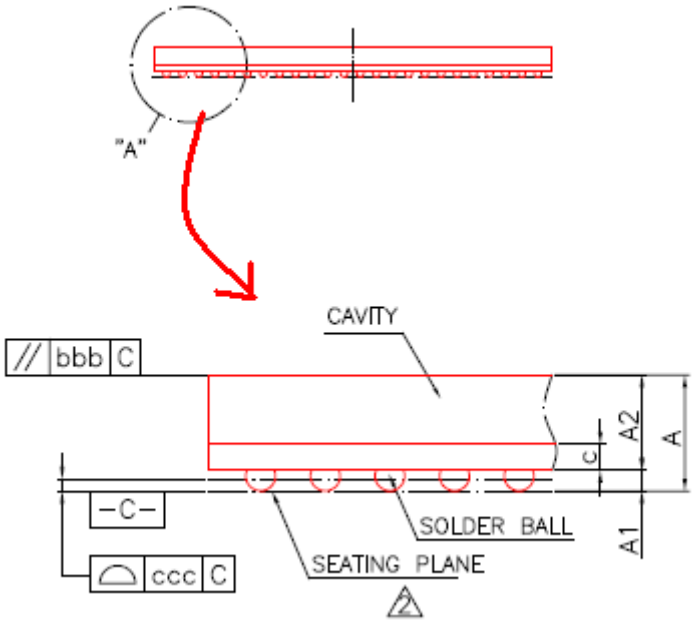


Fig. 2-3 Package Side View

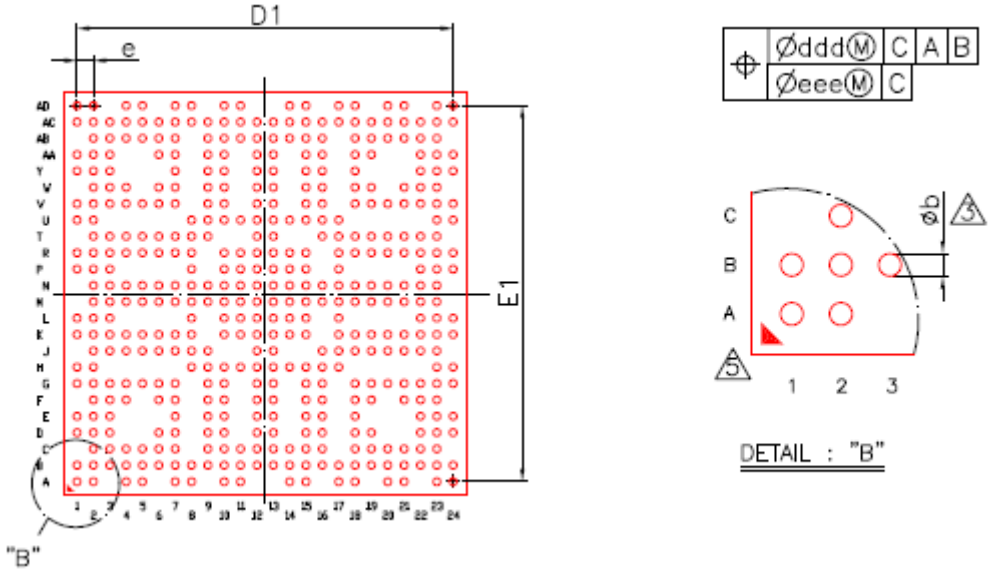


Fig. 2-4 Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	15.90	16.00	16.10	0.626	0.630	0.634
E	15.90	16.00	16.10	0.626	0.630	0.634
D1	---	14.95	---	---	0.589	---
E1	---	14.95	---	---	0.589	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	24/24			24/24		

Fig. 2-5 Package Dimension

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RK2908 absolute maximum ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	VDDCORE, OTG0_DVDD, HOST20_DVDD, DVDD_DPLL,	1.32	V
DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB, DDR IO)	VDDIO0~VDDIO5 VDDIO_LCD0, VDDIO_LCD1, VDDIO_VIP, VDDIO_FLASH0	3.6	V
DC supply voltage for DDR IO	VDDR	1.95	V
DC supply voltage for Analog part of SAR-ADC	VDDA_SARADC	2.75	V
DC supply voltage for Analog part of PLL	AHVDD_APLL AVDD_DPLL,	2.75 1.32	V
DC supply voltage for Analog part of USB OTG/Host2.0	OTG0_VDD25,HOST20_VDD25 OTG0_VDD33,HOST20_VDD33	2.75 3.63	V
Analog Input voltage for SAR-ADC	SARADC_AIN[0：3]	2.75	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Analog input voltage for RKELVIN/ID of USB OTG/Host2.0		2.75	V
Analog Input voltage for DP/DM of USB Host1.1		3.6	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIO		3.6	V
Storage Temperature		150	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

Table 3-2 RK2908 recommended operating conditions

Parameters	Symbol①	Min	Typ	Max	Units
Internal digital logic Power （except USB OTG)	VDDCORE, DVDD_DPLL,	1.08	1.2	1.32	V
Digital GPIO Power(3.3V)	VDDIO0~VDDIO5	3	3.3	3.6	V
Digital GPIO Power(3.3V/1.8V)	VDDIO_LCD0, VDDIO_LCD1 VDDIO_VIP, VDDIO_FLASH0 ,	3 1.62	3.3 1.8	3.6 1.98	V
DDR IO (DDRII mode) Power	VDDR	1.7	1.8	1.9	V
DDR IO (DDRIII mode) Power	VDDR	1.425	1.5	1.575	V
DDR IO (LPDDR mode) Power	VDDR	1.65	1.8	1.95	V
DDR reference supply (VREF) Input	VREF0,VREF1,VREF2	0.49*VDDIO_DDR	0.5*VDDIO_DDR	0.51*VDDIO_DDR	V
DDR External termination voltage		$VREF_i$ - 40mV	$VREF_i$	$VREF_i$ + 40mV	V

		(*i* =0~2)	(*i* =0~2)	(*i* =0~2)	
PLL(1.6GHz) Analog Power	AHVDD_APLL	2.25	2.5	2.75	V
PLL(1.0GHz) Analog Power	AVDD_DPLL	1.08	1.2	1.32	V
SAR-ADC Analog Power	VDDA_SARADC	2.25	2.5	2.75	V
USB OTG/Host2.0 Digital Power	OTG0_DVDD, HOST20_DVDD	1.116	1.2	1.32	V
USB OTG/Host2.0 Analog Power(2.5V)	OTG0_VDD25,HOST20_VDD25	2.325	2.5	2.75	V
USB OTG/Host2.0 Analog Power(3.3V)	OTG0_VDD33,HOST20_VDD33	3.069	3.3	3.63	V
USB OTG/Host2.0 external resistor	REXT	42.768	43.2	43.632	Ohm
PLL input clock frequency		N/A	24 27	N/A	MHz
Operating free air Temperature		-10	25	50	℃

Notes : ① Symbol name is same as the pin name in the io descriptions

3.3 DC Characteristics

Table 3-3 RK2908 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	V_{il}	-0.3	0	0.8	V
	Input High Voltage	V_{ih}	2	3.3	3.6	V
	Output Low Voltage	V_{ol}	N/A	0	0.4	V
	Output High Voltage	V_{oh}	2.4	3.3	N/A	V
	Threshold Point	V_t	1.41	1.54	1.68	V
	Threshold Point with Pullup Resistor Enabled	V_{tpu}	1.4	1.52	1.67	V
	Threshold Point with Pulldown Resistor Enabled	V_{tpd}	1.42	1.55	1.69	V
	Pullup Resistor	R_{pu}	34	50	80	Kohm
	Pulldown Resistor	R_{pd}	35	51	84	Kohm
Digital GPIO @1.8V	Input Low Voltage	V_{il}	-0.3	0	0.63	V
	Input High Voltage	V_{ih}	1.17	1.8	3.6	V
	Output Low Voltage	V_{ol}	N/A	0	0.45	V
	Output High Voltage	V_{oh}	1.35	1.8	N/A	V
	Threshold Point	V_t	0.8	0.89	0.98	V
	Threshold Point with Pullup Resistor Enabled	V_{tpu}	0.79	0.88	0.97	V
	Threshold Point with Pulldown Resistor Enabled	V_{tpd}	0.8	0.89	0.98	V
	Pullup Resistor	R_{pu}	64	111	204	Kohm
	Pulldown Resistor	R_{pd}	60	106	202	Kohm
DDR IO @DDRIII mode	Input High Voltage	V_{ih_ddr}	V_{REF} + 0.1		V_{DDQ}	V
	Input Low Voltage	V_{il_ddr}	VSS-0.3		V_{REF} - 0.1	V
	Output High Voltage	V_{oh_ddr}	0.8*VDDQ			V

	Output Low Voltage	V_{ol_ddr}			0.2*V_{DDQ}	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	R_{tt}	100 54 36	120 60 40	140 66 44	Ohm
DDR IO @DDRII mode	Input High Voltage	V_{ih_ddr}	$V_{REF\ i}$ + 0.125 (i=0~2)	1.8	VDDIO_DDR$_i$ + 0.3 (i=0~6)	V
	Input Low Voltage	V_{il_ddr}	-0.3	0	V_{REFi} - 0.125 (i=0~2)	V
	Output High Voltage	V_{oh_ddr}	VDDIO_DDR$_i$ - 0.28 (i=0~6)	1.8	N/A	V
	Output Low Voltage	V_{ol_ddr}	N/A	0	0.28	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	R_{tt}	120 60 40	150 75 50	180 90 60	Ohm
DDR IO @LPDDR mode	Input High Voltage	V_{ih_ddr}	0.7*VDDIO_DDR$_i$ (i=0~6)	1.8	N/A	V
	Input Low Voltage	V_{il_ddr}	N/A	0	0.3*VDDIO_DDR$_i$ (i=0~6)	V
PLL	Input High Voltage	V_{ih_pll}	0.8*DVDD_$_i$PLL (i=A,D,CG)	DVDD_$_i$PLL (i=A,D,CG)	DVDD_$_i$PLL (i=A,D,CG)	V
	Input Low Voltage	V_{il_pll}	0	0	0.2*DVDD_$_i$PLL (i=A,D,CG)	V
USB Host1.1 IO	Input High Voltage	V_{ih_uhost}	2	3.3	N/A	V
	Input Low Voltage	V_{il_uhost}	N/A	0	0.8	V

3.4 Electrical Characteristics for General IO

Table 3-4 RK2908 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	I_i	Vin = 3.3V or 0V	-10	N/A	10	uA
	Tri-state output leakage current	I_{oz}	Vout = 3.3V or 0V	-10	N/A	10	uA
	High level input current	I_{ih}	Vin = 3.3V, pulldown disabled	TBD	N/A	TBD	uA
			Vin = 3.3V, pulldown enabled	39	65	94	uA
	Low level input current	I_{il}	Vin = 0V, pullup disabled	TBD	N/A	TBD	uA
			Vin = 0V, pullup enabled	41	66	97	uA
Digital GPIO @1.8V	Input leakage current	I_i	Vin = 1.8V or 0V	-10	N/A	10	uA
	Tri-state output leakage current	I_{oz}	Vout = 1.8V or 0V	-10	N/A	10	uA
	High level input current	I_{ih}	Vin = 1.8V, pulldown disabled	TBD	N/A	TBD	uA
			Vin = 1.8V, pulldown enabled	9	17	30	uA
	Low level input current	I_{il}	Vin = 0V, pullup disabled	TBD	N/A	TBD	uA
			Vin = 0V, pullup enabled	8.8	16	28	uA

3.5 Electrical Characteristics for PLL

Table 3-5 RK2908 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL(1.6G) ②	Input clock frequency	F_{in}	$F_{in} = F_{ref} * NR$ ① @2.5V/1.2V	10	24/27	400	MHz
	Comparison frequency	F_{ref}	$F_{ref} = F_{in}/NR$ @2.5V/1.2V	10	N/A	50	MHz
	VCO operating range	F_{vco}	$F_{vco} = F_{ref} * NF$ ① @2.5V/1.2V	800	N/A	1600	MHz
	Output clock frequency	F_{out}	$F_{out} = F_{vco}/NO$ ① @2.5V/1.2V	100	N/A	1600	MHz
	Lock time	T_{lt}	@ 2.5V/1.2V	N/A	N/A	0.2	ms
	Power consumption (normal mode)	N/A	F_{in} = 50MHz, F_{out} = 1600MHz, @2.5V/1.2V, 25 ℃	N/A	2.3	N/A	mW
	Power consumption (bypass mode)	N/A	BP=HIGH , PD= LOW , F_{in} = 50MHz, F_{out} = 50MHz, @2.5V/1.2V, 25 ℃	N/A	85.6	N/A	uW
	Power consumption (power-down mode)	N/A	PD=HIGH, @2.75V/1.32V, 125 ℃	N/A	1.36	N/A	uW
PLL(1.0G) ②	Input clock frequency	F_{in}	$F_{in} = F_{ref} * NR$ ① @1.2V	10	24/27	400	MHz
	Comparison frequency	F_{ref}	$F_{ref} = F_{in}/NR$ @1.2V	10	N/A	50	MHz
	VCO operating range(high-band)	F_{vco}	$F_{vco} = F_{ref} * NF$ ① @1.2V	500	N/A	1000	MHz
	VCO operating range(low-band)			300	N/A	600	MHz
	Output clock frequency(high-band)	F_{out}	$F_{out} = F_{vco}/NO$ ① @1.2V	62.5	N/A	1000	MHz
	Output clock frequency(low-band)			37.5	N/A	600	MHz
	Lock time	T_{lt}	@ 1.2V	N/A	N/A	0.2	ms
	Power consumption (normal mode)	N/A	F_{in} = 50MHz, F_{out} = 1000MHz, High-band, @1.32V, 125 ℃	N/A	1.46	N/A	mW
	Power consumption (bypass mode)	N/A	BP=HIGH , PD= LOW , F_{in} = 50MHz, F_{out} = 50MHz, @1.32V, 125 ℃	N/A	13.38	N/A	uW
	Power consumption (power-down mode)	N/A	PD=HIGH, @1.32V, 125 ℃	N/A	1.41	N/A	uW

Notes : ①: *NR is the input divider value;*
NF is the feedback divider value;
NO is the output divider value

②: *PLL(1.6G) is ARM PLL with AHVDD_APLL and DVDD_DPLL power supply ;*
PLL(1.0G) is DDR PLL/CODEC PLL/GENERAL PLL with AVDD_DPLL and DVDD_DPLL power supply

3.6 Electrical Characteristics for SAR-ADC

Table 3-6 RK2908 Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution			N/A	10	N/A	Bits
Conversion speed	F_s	The duty cycle should be between 40%~60%	0.1	N/A	1	MSPS
Differential Non Linearity	DNL		N/A	±1	N/A	LSB
Integral Nn Linearity	INL		N/A	±2	N/A	LSB
Gain Error	E_{gain}		-8	N/A	8	LSB
Offset Error	E_{offset}		-8	N/A	8	mV

Analog Supply Current(VDDA_SARADC)			N/A	250	N/A	uA
Input Voltage range	Vin		0		2.5	V
Digital Supply Current			N/A	20	N/A	uA
Power Down Current			N/A	1	N/A	uA
Power up time			N/A	7	N/A	$1/F_S$

3.7 Electrical Characteristics for USB OTG/Host2.0 Interface

Table 3-7 RK2908 Electrical Characteristics for USB OTG/Host2.0 Interface

Parameters		Test condition	Min	Typ	Max	Units
HS transmit, maximum transition density (all 0's data in DP/DM)	Current From USB DVDD	75℃ , OTG0_VDD25 , HOST20_VDD25=2.5V, OTG0_VDD33, HOST20_VDD33= 3.3V, OTG0_DVDD, HOST20_DVDD = 1.2V , 15-cm USB cable attached to DP/DM	N/A	4.11	N/A	mA
	Current From USB VDD33		N/A	2.68	N/A	mA
	Current From USB VDD25		N/A	22.7	N/A	mA
HS transmit, minimum transition density (all 1's data in DP/DM)	Current From USB DVDD		N/A	3.98	N/A	mA
	Current From USB VDD33		N/A	2.64	N/A	mA
	Current From USB VDD25		N/A	15	N/A	mA
HS idle mode	Current From USB DVDD		N/A	6.22	N/A	mA
	Current From USB VDD33		N/A	2.67	N/A	mA
	Current From USB VDD25		N/A	5.99	N/A	mA
FS transmit, maximum transition density (all 0's data in DP/DM)	Current From USB DVDD		N/A	2.66	N/A	mA
	Current From USB VDD33		N/A	16.4	N/A	mA
	Current From USB VDD25		N/A	6.04	N/A	mA
LS transmit, maximum transition density (all 0's data in DP/DM)	Current From USB DVDD		N/A	3.34	N/A	mA
	Current From USB VDD33		N/A	15.3	N/A	mA
	Current From USB VDD25		N/A	6.22	N/A	mA
Suspend mode	Current From USB DVDD		N/A	1.83	N/A	uA
	Current From USB VDD33		N/A	0.1	N/A	uA
	Current From USB VDD25		N/A	15.2	N/A	uA
Sleep mode	Current From USB DVDD		N/A	0.141	N/A	mA
	Current From USB VDD33		N/A	0.1	N/A	uA
	Current From USB VDD25		N/A	0.629	N/A	mA

3.8 Electrical Characteristics for USB Host1.1 Interface

Table 3-8 RK2908 Electrical Characteristics for USB Host1.1 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Units
FS current (standby mode)			N/A	0.5	N/A	uA
FS current (input mode)			N/A	450	N/A	uA
FS current (output mode)			N/A	450	N/A	uA
Transceiver pad capacitance		Pad to ground	N/A	N/A	20	pF
Driver output resistance		steady state drive	N/A	10	N/A	Ohm

3.9 Electrical Characteristics for DDR IO

Table 3-9 RK2908 Electrical Characteristics for DDR IO

Parameters	Symbol	Test condition	Min	Typ	Max	Units

DDR IO @DDRII mode	VDDR standby current, ODT OFF		@ 1.8V , 125℃	0	0	1.24	mA
	Input leakage current, SSTL mode, unterminated		@ 1.8V , 125℃	0	0	0.42	uA
DDR IO @LPDDR mode	Input leakage current		@ 1.8V , 125℃	3.23	57.965	435.1	nA
	VDD(1.2V) quiescent current		@ 1.2V , 125℃	0.01	0.01	3.51	uA
	VDDR quiescent current		@ 1.8V , 125℃	0	0	1.15	uA

3.10 Electrical Characteristics for eFuse

Table 3-10 RK2908 Electrical Characteristics for eFuse

Parameters	Symbol	Test condition	Min	Typ	Max	Units
read current for EFUSE_VQPS	I_{load_vqps}	STROBE high	0.004	0.014	0.365	uA
read current for EFUSE_VQPS	I_{active_vqps}	normal read 10MHz	0.003	0.012	0.368	uA
standby current for EFUSE_VQPS	$I_{standby\_vqps}$		0.006	0.007	0.376	uA
power-down current for EFUSE_VQPS	I_{pd_vqps}		0.006	0.008	0.396	uA

Chapter 4 Hardware Guideline

4.1 Reference design for RK2908 oscillator PCB connection

Totally RK2908 may use two oscillators. Their typical clock frequency is 24MHz and 27MHz. The two oscillators will provide input clock to four on-chip PLLs, it is software-programmable to select one input clock from oscillator to PLLs.

- External reference circuit for oscillators with 24MHz and 27MHz input

In the following diagram, the value for RF, Rd, C1, C2 must be adjusted a little to improve performance of oscillator based on real crystal model. Especially C1 and C2 value is advised to meet formula (C1 * C2)/ (C1+C2) = ~8pF.

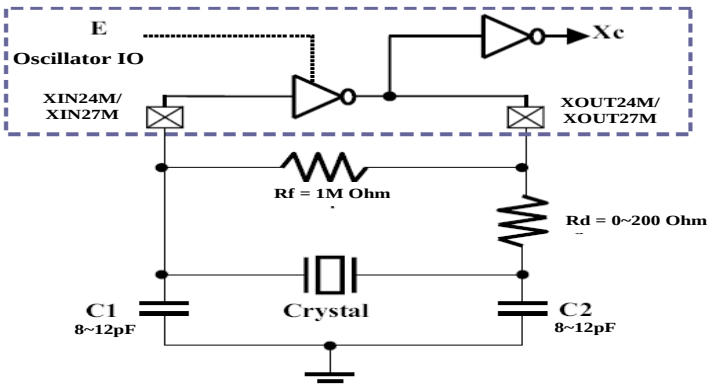


Fig. 4-1 External reference circuit for 24MHz/27MHz oscillators

4.2 Reference design for PLL PCB connection

The following reference design is suitable for two types of PLL in RK2908, one is ARM PLL with 1.6GHz, another is three PLLs with 1.0GHz, and the difference is that they have different value for C1/C2/C3/C4 components, since these values are related with PLL VCO maximum oscillating frequency (Fvco).

For 1.6GHz PLL, the AVDD/AVSS is mapped to AHVDD_APLL/AHVSS_APLL; DVDD/DVSS is mapped to DVDD_DPLL/DVSS_DPLL; for 1.0GHz PLLs, the AVDD/AVSS is mapped to AVDD_DPLL/AVSS_DPLL, DVDD/DVSS is mapped to DVDD_DPLL/DVSS_DPLL.

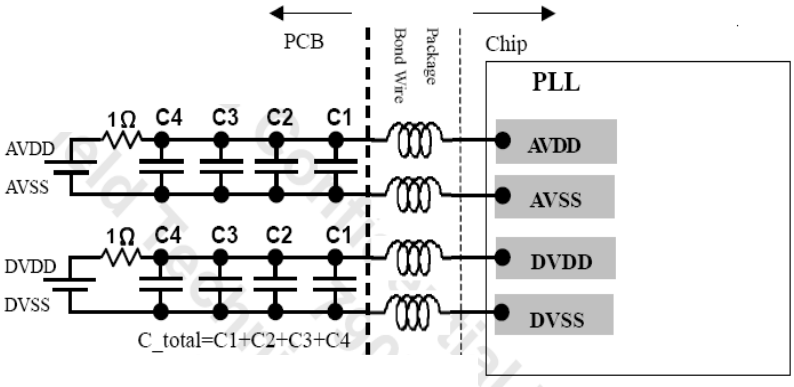


Fig. 4-2 External reference circuit for PLL

In the above circuit, 1 Ohm resistor of the filter is recommended for loading PLL current based on IR drop consideration. For capacitors C1/C2/C3/C4, SMD ceramic high-frequency capacitors are selected, and C1, C2, C3 must be chosen with the same series of product and dimension. Serial resonance frequency (SRF) of C1 is close to PLL Fvco (1.6GHz and 1.0GHz), after C1 value is decided, we can get C2/C3/C4 value based on the following formula:

C2 = 2*C1
C3 = 2*C2
C4 = C_total – (C1+C2+C3)
Fc_filter = 1/ (2*pi*R*C_total) <100 KHz

Another, please pay more attention to the following remindment :

- Total parasitic inductance, including of wire bond+PCB trace length, should be as small as possible by using shorter bonding wire and PCB trace.
- All capacitors should be placed as close to power and GNC pins as possible and shorten the current loop as short as possible.
- Use wide traces for power and ground paths. Keep adjacent digital signals and power traces away from AVDD/AVSS to avoid coupling noise.

4.3 Reference design for USB OTG/Host2.0 connection

In RK2908 there are USB OTG and USB Host2.0 interface, it is same interface for them in fact. The following diagram shows external reference design. Of course, for USB Host2.0 some signals can be removed based on different application.

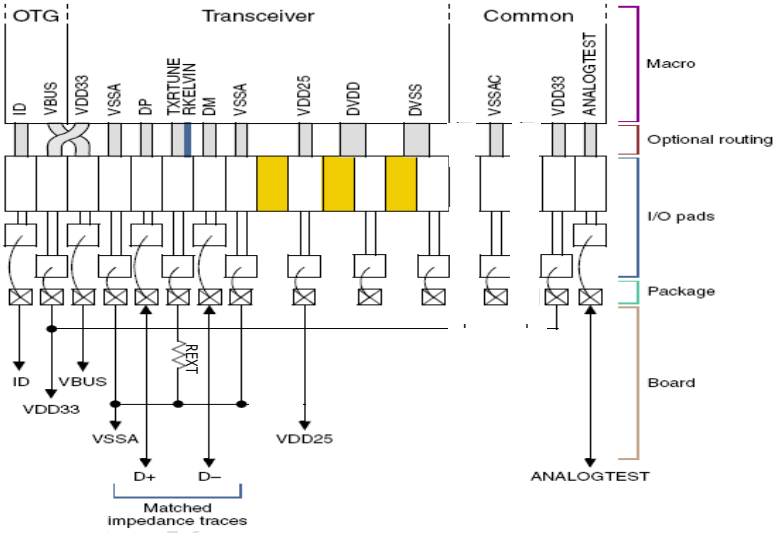


Fig. 4-3 RK2908 USB OTG/Host2.0 interface reference connection

4.4 RK2908 Power up/down sequence requirement

For all of the power supply in RK2908, there is no any specific requirement of power up/down sequence except power supply between core logic and DDRII/LPDDR IO or digital GPIO, between USB OTG/Host2.0 power supply.

- Power supply sequence for core logic(VDDCORE) and DDRII/LPDDR

It is generally recommended that the VDDCORE and VDDIO_DDR*i* be powered-up together, and it is also acceptable for VDDCORE supply to power-up a very short time before the VDDIO_DDR*i* supply. If VDDIO_DDR*i* supply must power-up before the VDDCORE supply, it is advised to keep the time between these two events less than 100ms to limit excessive VDDIO_DDR*i* current draws.

- Power supply sequence for core logic(VDDCORE) and digital GPIO power①

It is generally recommended that "turn on the higher GPIO voltage first and then the lower core voltage" so that the crowbar current would not occur on the power-up stage.

Also it is acceptable that "turn on the lower core voltage first and then higher GPIO voltage" only if the GPIO control pins are set to a fixed state. However, the ramp-up time for them cannot be less than 10us.

There is no requirement on the power-down sequence for two above groups. Customers can decide which voltage to be down first based on the application need.

- Power supply sequence for USB OTG/Host2.0
  Please follow the following sequence for power up and recommended ramp-up time is more than 10us
  DVDD (1.2V) -> VDD25 (2.5V) -> VDD33 (3.3V)
  For power down sequence, just reverse with power up sequence.
  VDD33 (3.3V) -> _VDD25 (2.5V) -> _DVDD (1.2V)

Notes :①: Digital GPIO power include VDDIOi (i=0~5) , VDDIO_VIP, VDDIO_LCDC0, VDDIO_FLASHj,.

4.5 RK2908 Power on reset descriptions

The following figure shows power-on-reset sequence. External power-on-reset input signal NPOR is released after stabilization of oscillator input clock XIN24M or XIN27M . Internal signal sysrstn is generated after NPOR is filtered glitch , which can filter out 5 clock cycles(24MHz or 27MHz) for low pulse of NPOR, so 208ns or 185ns low pulse of NPOR will not be recognized as valid power-on-reset signal for RK2908.

To make PLLs work normally, the internal power down signal(pllpd) for PLLs must be high after power-on-reset, and maintains high level for more than 1us after sysrstn is deasserted. After pllpd is deasserted, PLLs will consume up to 200us to lock.

So the system will wait about 208us, then deactive internal reset signal chiprstn, which is used to control generation logic of all the clock inside CRU.

After 256 cycles or about 10.7us , rstn_pre for reset signal of all internal IPs will be deasserted , in other words, about 10.7us of clock has been generated before reset of every internal module is released.

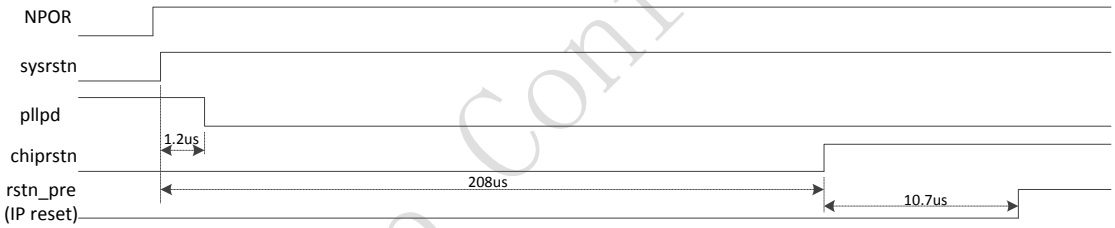


Fig. 4-4 RK2908 reset signals sequence