

# **RK3026 BRIEF**

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## Revision History

This document is now Production Data.

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2013-08-28	1.0	Initial Release
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## chapter 1 Introduction

### 1.1 Overview

RK3026 is a low power, high performance processor solution for tablet, and other digital multimedia applications, and integrates Dual-core Cortex-A9 with separately Neon and FPU coprocessor ,and also with 256KB L2 Cache.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3026 supports almost full-format video decoder by 1080p@60fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder and special image preprocessor and postprocessor .

Embedded 3D GPU makes RK3026 completely compatible with OpenGL ES1.1 and 2.0, OpenVG 1.1 etc. Special 2D hardware engine with MMU will maximize display performance.

RK3026 has high-performance external memory interface(DDR3/LVDDR3) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications as follows :

- Support 8bits async Nand Flash, sync Toggle Nand Flash, LBA Nand Flash and sync ONFI Nand Flash, 4 banks,all embedded up to 60bits hardware ECC
- 2 ranks, 1GB Memory space, 16bits DDR3-1066, LVDDR3-1066
- Support 8bits eMMC
- One-channels SD/MMC interface to support 4bits MMC4.41, SD3.0 or SDIO3.0
- 4-layers TFT LCD Controller, 24bits data, 1920x1080 maximum display size
- 18/24 bits LVDS output, and comply with the Standard TIA/EIA-644-A LVDS
- One-channel, 8bits CCIR656 interface and 8bits Raw data interface
- One I2S/PCM interface
- One USB OTG 2.0 and one USB Host2.0 interface
- 3x I2C, 1xUART with hardware flow-control , 1x SPI , 2x PWM
- Audio Codec with Mono Microphone interface

### 1.2 Features

#### 1.2.1 MicroProcessor

- Dual-core ARM Cortex-A9 processor is a high-performance, low-power, cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- Integrated timer and watchdog timer in CPU
- Integrated 32KB L1 instruction cache , 32KB L1 data cache, 4-way set associative
- 256KB unified L2 Cache
- coresight debug solution
  - Invasive debug
- One isolated voltage domain to support DVFS
- Maximum frequency can be up to 1.0GHz@1.1V, 25°C

### 1.2.2 Memory Organization

- Internal on-chip memory
  - 16KB BootRom
  - 8KB internal SRAM
- External off-chip memory<sup>®</sup>
  - DDR3-1066, 16bits data width, 2 ranks, 1GB(max) address space per rank
  - LVDDR3-1066, 16bits data width, 2 ranks, 1GB(max) address space per rank
  - Async/ Sync Toggle/ Sync ONFI Nand Flash(include LBA Nand), 8bits data width, 4 banks

### 1.2.3 Internal Memory

- Internal BootRom
  - Size : 16KB
  - Support system boot from the following device :
    - ◆ 8bits Async Nand Flash
    - ◆ SPI interface
    - ◆ eMMC interface
    - ◆ SDMMC interface
  - Support system code download by the following interface:
    - ◆ USB OTG
    - ◆ UART1
- Internal SRAM
  - Size : 8KB

### 1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/LVDDR3)
  - Compatible with JEDEC standard DDR3/ LVDDR3 SDRAM
  - Data rates of up to 1066Mbps(533MHz) for DDR3/LVDDR3
  - Support up to 2 ranks (chip selects), maximum 1GB address space per rank
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/ LVDDR3 SDRAM;
  - Compensation for board delays and variable latencies through programmable pipelines
  - Programmable output and ODT impedance with dynamic PVT compensation
- Nand Flash Interface
  - Support 8bits async/toggle/syncnandflash, up to 4 banks
  - Support LBA nandflash
  - 16bits, 24bits, 40bits, 60bits hardware ECC
  - For DDR nandflash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 66.5MHz
  - For async/togglenandflash, support configurable interface timing , maximum data rate is 16bit/cycle
  - Embedded AHB master interface to do data transfer by DMA method
  - Also support data transfer by AHB slave interface together with external DMAC
- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection

- Embedded clock frequency division control to provide programmable baud rate
- Support block size from 1 to 65535Bytes
- 8bits data bus width
- SD/MMC Interface
  - Compatible with SD2.0, MMC ver4.41
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

#### 1.2.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3026
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components
  - Support flexible clock solution, including clock source, clock mux, clock frequency division
  - One oscillator with 24MHz clock and 4 embedded PLLs
- Timer
  - On-chip 64bits Timers with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - 24MHz/PCLK clock input for operating domain, and PCLK input for bus interface domain.
- PWM
  - On-chip PWMs with interrupt-based operation
  - Programmable 4-bit pre-scalar from apb bus clock
  - Embedded 32-bit timer/counter facility
  - Support single-run or continuous-run PWM mode
  - Provides reference mode and output various duty-cycle waveform
- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from apb bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - ◆ Generate a system reset
    - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period
- Bus Architecture
  - QoS function is supported to improve the utility of bus bandwidth
- Interrupt Controller
  - Support 3 PPI interrupt source and 96 SPI interrupt sources input from different components inside RK3026
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt output (nFIQ and nIRQ) to per Cortex-A9, both are low-level

sensitive

- Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC

- Linked list DMA function is supported to complete scatter-gather transfer
- Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
- Signals the occurrence of various DMA events using the interrupt output signals
- Mapping relationship between each channel and different interrupt outputs is software-programmable
- One embedded DMA controller in periph system
- DMAC features:
  - ◆ 8 channels totally
  - ◆ 13 hardware request from peripherals
  - ◆ 2 interrupt output
  - ◆ Not support trustzone technology

### 1.2.6 Video CODEC

- Video Decoder

- Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, VC-1, RV, VP6/VP8, Sorenson Spark
- Error detection and concealment support for all video formats
- Output data structure after decoder is YCbCr 4:2:0 semi-planar to have more efficient bus usage, For H.264, YCbCr 4:0:0(monochrome) is also supported
- Minimum image size is 48x48 for all video formats
- H.264 up to HP level 4.2 : 1080p@60fps (1920x1080)<sup>®</sup>
- MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1080)
- MPEG-2 up to MP : 1080p@60fps (1920x1080)
- MPEG-1 up to MP : 1080p@60fps (1920x1080)
- H.263 : 576p@60fps (720x576)
- Sorenson Spark : 1080p@60fps (1920x1080)
- VC-1 up to AP level 3 : 1080p@30fps (1920x1080)
- RV8/RV9/RV10 : 1080p@60fps (1920x1080)
- VP6/VP8 : 1080p@60fps (1920x1080)
- For H.264, Image cropping not supported
- For MPEG-4, GMC(global motion compensation) not supported
- For VC-1, upscaling and range mapping are supported in image post-processor
- For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder

- Encoder only for H.264 ([BP@level4.0](#), [MP@level4.0](#), [HP@level4.0](#)) standard
- Only support I and P slices, not B slices
- Entropy encoding is CAVLC in BP and CABAC in MP
- Support error resilience based on constrained intra prediction and slices
- Maximum MV length is +/- 14 pixels in vertical direction and +/-30 pixels in horizontal direction
- Motion vector pixel accuracy is up to 1/4 pixels in 720p resolution and 1/2 pixels in 1080p resolution
- 12 intra prediction modes
- Number of reference frames is 1
- Maximum number of slice groups is 1
- Input data format :
  - ◆ YCbCr 4:2:0 planar
  - ◆ YCbCr 4:2:0 semi-planar



- ◆ YCbYCr 4:2:2
- ◆ CbYCrY 4:2:2 interleaved
- ◆ RGB444 and BGR444
- ◆ RGB555 and BGR555
- ◆ RGB565 and BGR565
- ◆ RGB888 and BRG888
- ◆ RGB101010 and BRG101010
- Output data format : H.264 byte unit stream and H.264 NAL unit stream
- Image size is from 96x96 to 1920x1080(Full HD)
- Maximum frame rate is up to 30fps@1920x1080<sup>®</sup>
- Bit rate supported is from 10Kbps to 20Mbps

### 1.2.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Maximum data rate is up to 76million pixels per second
- JPEG encoder
  - Input raw image :
    - ◆ YCbCr 4:2:0 planar
    - ◆ YCbCr 4:2:0 semi-planar
    - ◆ YCbYCr 4:2:2
    - ◆ CbYCrY 4:2:2 interleaved
    - ◆ RGB444 and BGR444
    - ◆ RGB555 and BGR555
    - ◆ RGB565 and BGR565
    - ◆ RGB888 and BRG888
    - ◆ RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate<sup>®</sup> up to 90million pixels per second

### 1.2.8 Image Enhancement(inside video encoder/decoder in ON2)

- Image pre-processor(embedded inside video encoder)
  - Only used together with HD video encoder inside RK3026 , not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT.601 , BT.709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees
- Video stabilization(embedded inside video encoder)
  - Work in combined mode with HD video encoder inside RK30xx and stand-alone mode
  - Adaptive motion compensation filter
  - Support scene detection from video sequence, encodes key frame when scene change noticed
- Image post-processor(embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth

- Also work as a stand-alone mode, its input data is from a camera interface or other image data stored in external memory
- Input data format :
  - ◆ any format generated by video decoder in combined mode
  - ◆ YCbCr 4:2:0 semi-planar
  - ◆ YCbCr 4:2:0 planar
  - ◆ YCbYCr 4:2:2
  - ◆ YCrYCb 4:2:2
  - ◆ CbYCrY 4:2:2
  - ◆ CrYCbY 4:2:2
- Output data format:
  - ◆ YCbCr 4:2:0 semi-planar
  - ◆ YCbYCr 4:2:2
  - ◆ YCrYCb 4:2:2
  - ◆ CbYCrY 4:2:2
  - ◆ CrYCbY 4:2:2
  - ◆ Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888, RGB565, ARGB4444 etc.
- Input image size:
  - ◆ Combined mode : from 48x48 to 8176x8176 (66.8Mpixels)
  - ◆ Stand-alone mode : width from 48 to 8176, height from 48 to 8176, and maximum size limited to 16.7Mpixels
  - ◆ Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8, vertical step size 2)
- Support image up-scaling :
  - ◆ Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
  - ◆ Arbitrary non-integer scaling ratio separately for both dimensions
  - ◆ Maximum output width is 3x input width
  - ◆ Maximum output height is 3x input height
- Support image down-scaling:
  - ◆ Arbitrary non-integer scaling ratio separately for both dimensions
  - ◆ Unlimited down-scaling ratio
- Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering for 4,5,6bit RGB channel precision)
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
  - ◆ 8bit alpha +YUV444, big endian channel order with AYUV8888
  - ◆ 8bit alpha +24bit RGB, big endian channel order with ARGB8888
- Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
- Support RGB image contrast / brightness / color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

### 1.2.9 Image Enhancement(New IEP lite module)

- Image format support
  - Input data: XRGB/RGB565/YUV420/YUV422
  - Output data: ARGB/RGB565/YUV420/YUV422
  - ARGB/XRGB/RGB565/YUV swap
  - UV SP/P

- BT601\_l/BT601\_f/BT709\_l/BT709\_f color space conversion
- RGB dither up/down
- YUV up/down sampling
- Max source image resolution: 8192x8192
- Max scaled image resolution: 4096x4096
- YUV enhancement &denoise
  - Hue, Saturation, Brightness, Contrast adjustment
- RGB enhancement &denoise
  - Contrast enhancement
  - Color enhancement
  - Gamma adjustment
- High quality scale
  - Averaging filter down-scaling
  - Bi-cubic up-scaling
  - Arbitrary non-integer horizontal & vertical scaling ratio range from 1/16 to 16
- De-interlace
  - 3x5 Y motion detection matrix
  - Source width up to 1920
  - Configed high frequency de-interlace
  - I4O2 (Input 4 field,output 2 frame) /I4O1B/I4O1T/I2O1B/I2O1T mode
- Interface
  - Configed direct path to LCDC if source width no more than 1920
  - 32bit AHB bus slave
  - 64bit AXI bus master
  - Combined interrupt output

#### 1.2.10 Graphics Engine

- 3D Graphics Engine :
  - High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
  - Embedded 4shader cores with shared hierarchical tiler
  - Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
  - Provide MMU and L2 Cache with 32KB size
  - Triangle rate : 30M triangles/s
  - Pixel rate: 300 pixels/s @ 150MHz
- 2D Graphics Engine(RGA module) :
  - Pixel rate: 300M pixel/s without scale, 150M pixel/s with bilinear scale, 66.5M pixel/s with bicubic scale.
  - Bit Blit with Strength Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules , chroma key, and pattern mask
  - 8K x 8K raster 2D coordinate system
  - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
  - Programmable bicubic filter to support image scaling
  - Blending, scaling and rotation are supported in one pass for stretch blit
  - Source formats :
    - ◆ ABGR8888, XBGR8888, ARGB8888, XRGB8888

- ◆ RGB888, RGB565
- ◆ RGBA5551, RGBA4444
- ◆ YUV420 planar, YUV420 semi-planar
- ◆ YUV422 planar, YUV422 semi-planar
- ◆ BPP8, BPP4, BPP2, BPP1
- Destination formats :
  - ◆ ABGR8888, XBGR888, ARGB8888, XRGB888
  - ◆ RGB888, RGB565
  - ◆ RGBA5551, RGBA4444
  - ◆ YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
  - ◆ YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

### 1.2.11 Video IN/OUT

- Camera Interface
  - Support up to 5M pixels
  - 8bits CCIR656(PAL/NTSC) interface
  - 8bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support image crop with arbitrary windows
- Display Interface
  - Support LCD or TFT interfaces up to 1920x1080
  - Parallel RGB LCD Interface :
    - RGB666(18bits) ,RGB565(15bits)
  - MCU LCD interface: i-8080, Hold/Auto/Bypass modes
  - TV Interface: ITU-R BT.656(8-bit, 480i/576i/1080i)
  - Max output resolution 1920x1080
  - 4 display layers :
    - ◆ One background layer with programmable 24bits color
    - ◆ One video layer (win0)
      - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
      - maximum resolution is 1920x1080,support virtual display
      - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
      - 256 level alpha blending
      - Support transparency color key
      - 3D display support
      - Direct path support
    - ◆ One video layer (win1)
      - RGB888, ARGB888, RGB565, 1/2/4/8bpp
      - Support virtual display
      - 256 level alpha blending (pre-multiplied alpha support)
      - Support transparency color key
      - Direct path support
    - ◆ Hardware cursor(win3)
      - 2BPP , two transparent modes
      - Support two size: 32x32 and 64x64
      - 16 level alpha blending
  - Win0 and Win1 layer overlay exchangeable
  - 3 x 256 x 8 bits display LUTs
  - Support color space conversion :
    - YUV2RGB(rec601-mpeg/rec601-jpeg/rec709) and RGB2YUV
  - Deflicker support for interlace output
  - Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation

- Blank and blank display
- Standby mode
- Support non-scaler and scaler output(max up to 1024x768)
- LVDS interface
  - 135MHz clock support
  - 28:4 data sub\_channel compression at data rates up to 945 Mbps per channel
  - Support VGA,SVGA,XGA and single pixel SXGA
  - PLL requires no external components
  - Comply with the Standard TIA/EIA-644-A LVDS standard
  - Support alternative LVDS output or LVTTTL output

#### 1.2.12 Audio Interface

- I2S/PCM
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM cannot be used at the same time
- Audio Codec
  - 18 to 24 bit High Order Sigma-Delta modulation for DAC for >93 dB SNR configurable
  - 16 to 18 bit High Order Sigma-Delta modulation for ADC for >90 dB SNR configurable
  - Digital interpolation and decimation filter integrated
  - Microphone in and Speaker out Interface
  - On-Chip Analog Post Filter and digital filters
  - Single-ended or differential Input and Output
  - Sampling Rate of 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz
  - Support 16ohm to 32ohm Head Phone and Speaker Phone Output
  - Mono, Stereochannel supported
  - Optional Fractional PLL available that support 6Mhz to 20Mhz clock input to any clockoutput that meets 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz and 128 time oversampling ratio.

#### 1.2.13 Connectivity

- SDIO interface
  - Compatible with SDIO 2.0 protocol
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - 4bits data bus width
- SPI Controller
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode
- UartController
  - DMA-based or interrupt-based operation
  - UART0 Embeds two 64Bytes FIFO for TX and RX operation respectively
  - UART1/UART2 Embedded two 32Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start,stop and parity

- Support different input clock for uart operation to get up to 4Mbps or other special baud rate
- Support non-integer clock divides for baud clock generation
- Support auto flow control mode
- I2C controller
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode
- GPIO
  - All of GPIOs can be used to generate interrupt to Cortex-A9
  - All of pullup GPIOs are software-programmable for pullup resistor or not
  - All of pulldown GPIOs are software-programmable for pulldown resistor or not
  - All of GPIOs are always in input direction in default after power-on-reset
- USB Host2.0
  - Compatible with usb host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode
- USB OTG2.0
  - Compatible with usb otg2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

#### 1.2.14 Others

- SAR-ADC(Successive Approximation Register)
  - 10-bit SAR analog-to-digital converter
  - Sample rate  $F_s$  is 200KHz
  - SAR-ADC clock must be large than  $11 \cdot F_s$ , recommend is  $11 \cdot F_s$
  - DNL less than 1 LSB , INL less than 2.0 LSB
  - Power supply is 3.3V ( $\pm 10\%$ ) for analog interface, power dissipation is less than 900uW
- eFuse
  - two 256bits (32x8) high-density electrical Fuse
  - Programming condition :  $V_P$  must be 2.5V( $\pm 10\%$ )
  - Program time is 10us.
  - Read condition :  $V_P$  must be 2.5V( $\pm 10\%$ )
  - Provide inactive mode

Notes : ① : DDR3/LVDDR3 are not used simultaneously as well as async and sync ddrnand flash

②: Actual maximum frame rate will depend on the clock frequency and system bus performance

③: Actual maximum data rate will depend on the clock frequency and JPEG compression rate

### 1.3 Block Diagram

The following diagram shows the basic block diagram for RK3026.

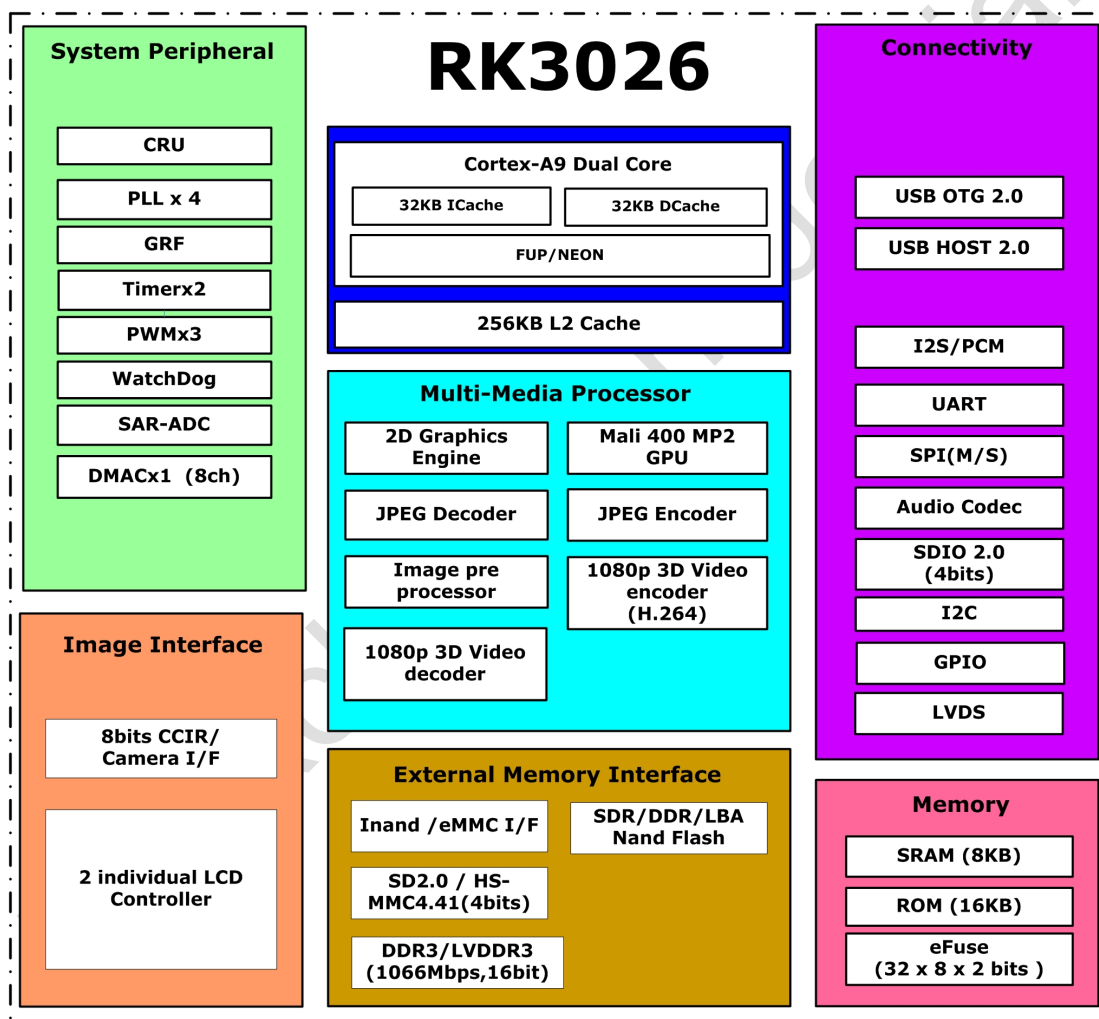


Fig.1- 1 RK3026 Block Diagram