RK3066 Datasheet brief

Revision 1.0
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Revision History

Date	Revision	Description
2011-10-30	0.0	Initial Release
2012-02-15	1.0	Add package information

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CHAPTER 1 Introduction

1.1 Overview

RK3066 is a low power, high performance processor solution for mobile phones, personal mobile internet device and other digital multimedia applications, and integrates dual-core Cortex-A9 with separately NEON and FPU coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3066 supports almost full-format video decoder by 1080p@60fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/ decoder and special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3066 completely compatible with OpenGL ES2.0 and 1.1, OpenVG 1.1. Even support high quality 3D video replay. Special 2D hardware engine with MMU will maximize display performance.

RK3066 has high-performance external memory interface (DDR3/ LVDDR3/LPDDR/ LPDDR2) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

This document will provide guideline on how to use RK3066 correctly and efficiently. In them , the chapter 1 and chapter 2 will introduce the features, block diagram, signal descriptions and system usage of RK3066, the chapter 3 through chapter 45 will describe the full function of each module in detail.

1.2 Features

1.2.1 Processor

- Dual-core ARM Cortex-A9 MPCore processor is a high-performance, low-power, cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- SCU ensures memory coherency between the two CPUs
- Integrated timer and watchdog timer per CPU
- Integrated 32KB L1 instruction cache , 32KB L1 data cache, 4-waty set associative
- 512KB unified L2 Cache
- Trustzone technology support
- Full coresight debug solution
  - Debug and trace visibility of whole systems
  - ETM trace support
  - Invasive and non-invasive debug
- Four separate power domain to support Internal power switch on/off and externally turn on/off based on different application scenario
  - PD_A9_0: 1st Cortex-A9 + Neon + FPU + L1 I/D Cache
  - PD_A9_1: 2nd Cortex-A9 + Neon + FPU + L1 I/D Cache
  - PD_DBG: CoreSight-DK for Cortex-A9
  - PD_SCU: SCU + L2 Cache controller, and including PD_A9_0, PD_A9_1, PD_DGB
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
  - 10KB BootRom

- 64KB internal SRAM for security and non-security access, detailed size is programmable
- 2KB internal SRAM shared with NandC

- External off-chip memory①
  - DDR3/LVDDR3, 16/32bits data width, 2 ranks, 2GB(max) address space per rank
  - LPDDR, 32bits data width, 2 ranks, 2GB(max) address space per rank
  - LPDDR2, 32bits data width, 2 ranks, 2GB(max) address space per rank
  - Async SRAM/Nor Flash, 8/16bits data width,2banks,1MB(max) address space per bank
  - Async Nand Flash(include LBA Nand), 8/16bits data width, 8 banks
  - Sync DDR Nand Flash , 8bits data width, 8 banks

1.2.3 Internal Memory

- Internal BootRom
  - Size : 10KB
  - Support system boot from the following device :
    - 8bits/16bits Async Nand Flash
    - SPI0 interface
    - eMMC interface
  - Support system code download by the following interface:
    - USB OTG
    - UART0 in CPU system
- Internal SRAM
  - Size : 64KB
  - Support security and non-security access
- 512KB internal SRAM shared with L2 Cache for Cortex-A9

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/LVDDR3/LPDDR/LPDDR2)
  - Compatible with JEDEC standard DDR3/LVDDR3/LPDDR/LPDDR2 SDRAM
  - Support up to 2 ranks (chip selects), maximum 2GB address space per rank
  - 16bits/32bits data width is software programmable
  - Programmable timing parameters support DDR3/LPDDR/LPDDR2 SDRAM from various vendor
  - Low power modes, such as power-down and self-refresh for DDR3/LVDDR3/ LPDDR/LPDDR2 SDRAM; clock stop and deep power-down for LPDDR/LVDDR3/ LPDDR2 SDRAM
  - Compensation for board delays and variable latencies through programmable pipelines
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Support one low-power work mode: power down DDR PHY and most of DDR IO except two CS and two CKE output signals, make SDRAM still in self-refresh state to prevent data missing.

- Static Memory Interface (ASRAM/Nor Flash)
  - Compatible with standard async SRAM or Nor Flash
  - Support up to 2 banks (chip selects), maximum 1MB address space per bank
  - For bank0, 8bits/16bits data width is software programmable; For bank1, 16bits data width is fixed
  - Support separately data and address bus, also support shared data and address bus to save IO numbers

- Nand Flash Interface
  - Support 8bits/16bits async nand flash, up to 8 banks
  - Support 8bits sync DDR nand flash, up to 8 banks

- Support LBA nand flash in async or sync mode
- Support up to 60bits hardware ECC
- For async nand flash, support configurable interface timing , maximum data rate is 16bit/cycle
- Embedded AHB master interface to do data transfer by DMA method
- Also support data transfer by AHB slave interface together with external DMAC1

- eMMC Interface
  - Compatible with standard INAND interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - One AHB slave interface to complete data transfer together with external DMAC1 or CPU
  - Support CRC generation and error detection
  - Support host pull-up control, card detection and initialization, write protection
  - Support block size from 1 to 65535Bytes
  - Data bus width is 8bits

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.41
  - One AHB slave interface to complete data transfer together with external DMAC1 or CPU
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support host pull-up control, card detection and initialization, write protection
  - Data bus width is flexible to support 1bit/4bits for SD mode and 1bit/4bits/8bits for MMC mode

1.2.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3066
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components
  - Support flexible clock solution, including clock source, clock mux, clock frequency division
  - One oscillator with 24MHz clock and 4 embedded PLLs
  - Up to 1.5GHz clock output for all PLLs

- PMU(power management unit)
  - 7 work modes(slow mode, normal mode, idle mode, deep-idle mode, stop mode, sleep mode, power-off mode) to save power by different frequency or auto metical clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - Separate voltage domains
  - Separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - on-chip 32bits Timers with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable 4-bit pre-scalar from apb bus clock

- Embedded 32-bit timer/counter facility
- Support single-run or continuous-run PWM mode
- Support maskable interrupt
- Provides reference mode and output various duty-cycle waveform
- Provides capture mode and measure the duty-cycle of input waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from APB bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 64-bit multi-layer AXI/AHB/APB composite bus architecture
  - Five embedded AXI interconnect

- Interrupt Controller
  - Support 3 PPI interrupt source and 76 SPI interrupt sources input from different components inside RK3066
  - Support 16 softwre-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt output (nFIQ and nIRQ) to per Cortex-A9, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controller , DMAC0 is for CPU system, DMAC1 is for peri system
  - DMAC0 features:
    - 6 channels totally
    - 11 hardware request from peripherals
    - 2 interrupt output
    - Dual APB slave interface for register config, designated as secure and non-secure
    - Support trustzone technology and programmable secure state for each DMA channel
  - DMAC1 features:
    - 7 channels totally
    - 13 hardware request from peripherals
    - 2 interrupt output
    - Not support trustzone technology

- Security system
  - Support trustzone technology for the following components inside RK3066

1.2.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264, AVS, VC-1, RV, VP6/VP8, Sorenson Spark, MVC
  - Error detection and concealment support for all video formats
  - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
  - H.264 up to HP level 4.2 : 1080p@60fps (1920x1088)③
  - MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1088)
  - MPEG-2 up to MP : 1080p@60fps (1920x1088)
  - MPEG-1 up to MP : 1080p@60fps (1920x1088)
  - H.263 : 576p@60fps (720x576)
  - Sorenson Spark : 1080p@60fps (1920x1088)
  - VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
  - RV8/RV9/RV10 : 1080p@60fps (1920x1088)
  - VP6/VP8 : 1080p@60fps (1920x1088)
  - AVS : 1080p@60fps (1920x1088)
  - MVC : 1080p@60fps (1920x1088)
  - For AVS, 4:4:4 sampling not supported
  - For H.264, Image cropping not supported
  - For MPEG-4,GMC(global motion compensation) not supported
  - For VC-1, upscaling and range mapping are supported in image post-processor
  - For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Support video encoder for H.264 (BP@level4.0, MP@level4.0, HP@level4.0), MVC and VP8
  - Only support I and P slices, not B slices
  - Support error resilience based on constrained intra prediction and slices
  - Input data format :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Image size is from 96x96 to 1920x1088(Full HD)
  - Maximum frame rate is up to 30fps@1920x1080③
  - Bit rate supported is from 10Kbps to 20Mbps

1.2.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar

- Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
- Maximum data rate④ is up to 76million pixels per second

- JPEG encoder
  - Input raw image:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate④ up to 90million pixels per second

1.2.8 Image Enhancement

- Image pre-processor
  - Only used together with HD video encoder inside RK3066 , not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT.601 , BT.709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees

- Video stabilization
  - Work in combined mode with HD video encoder inside RK3066 and stand-alone mode
  - Adaptive motion compensation filter
  - Support scene detection from video sequence, encodes key frame when scene change noticed

- Image post-processor(embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from a camera interface or other image data stored in external memory
  - Input data format :
    - any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
  - Ouput data format:
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
    - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888,RGB565,ARGB4444 etc.

- Input image size:
  - Combined mode : from 48x48 to 8176x8176 (66.8Mpixels)
  - Stand-alone mode : width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
  - Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
- Support image up-scaling :
  - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Maximum output width is 3x input width
  - Maximum output height is 3x input height
- Support image down-scaling:
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Unlimited down-scaling ratio
- Support YUV to RGB color conversioin, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering for 4,5,6bit RGB channel precision
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
  - 8bit alpha +YUV444, big endian channel order with AYUV8888
  - 8bit alpha +24bit RGB, big endian channel order with ARGB8888
- Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
- Support RGB image contrast / brightness / color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in pcture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

- Image Post-Processor (IPP)(standalone)
  - memory to memory mode
  - input data format and size
    - RGB888 : 16x16 to 8191x8191
    - RGB565 : 16x16 to 8191x8191
    - YUV422/YUV420 : 16x16 to 8190x8190
    - YUV444 : 16x16 to 8190x8190
  - pre scaler
    - integer down-scaling(ratio: 1/2,1/3,1/4,1/5,1/6,1/7,1/8) with linear filter
    - deinterlace(up to 1080i) to support YUV422&YUV420 input format
  - post scaler
    - down-scaling with 1/2 ~ 1 arbitary non-integer ratio
    - up-scaling with 1~4 arbitary non-integer ratio
    - 4-tap vertical, 2-tap horizontal filter
    - The max output image width of post scaler is 4096
  - Support rotation with 90/180/270 degrees and x-mirror, y-mirror

1.2.9 Graphics Engine

- 3D Graphics Engine :
  - Compatible with OpenGL ES1.1 and 2.0, OpenVG1.1.
  - Embedded four shader cores with shared hierarchical tiler
  - Unified sharder architecture
  - Provide MMU and L2 Cache with 128KB size
  - Pixel rate: 1G pixel/s

- 2D Graphics Engine :
  - Bit Blit with Strength Blit, Simple Blit and Filter Blit
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules, chroma key, and pattern mask
  - 8K x 8K raster 2D coordinate system
  - Programmable bicubic filter to support image scaling
  - Source format :
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar
    - YUV422 planar, YUV422 semi-planar
    - BPP8, BPP4, BPP2, BPP1
  - Destination formats :
    ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
  - YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.2.10 Video IN/OUT

- Camera Interface
  - 2 independent camera interface controller
  - Support up to 5M pixels
  - 8bits CCIR656(PAL/NTSC) interface
  - 8bits/10bits/12bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support simple image effects such as Arbitrary(sepia), Negative, Art freeze, Embossing etc.
  - Support static histogram statistics and white balance statistics
  - Support image crop with arbitrary windows
  - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio

- Display Interface
  - independent two display controllers for HDMI and TFT dual panel display
  - Support LCD or TFT interfaces up to 1920x1080
  - Support HDMI 1.4 output up to 1080p@30fps
  - Support TV interface with ITU-R BT.656 (8bits, 480i/576i/1080i)
  - Parallel RGB LCD Interface: RGB888(24bits),RGB666(18bits), RGB565(15bits)
  - Serial RGB LCD Interface: 3x8bits with RGB delta support, 3x8bits followed by dummy data, 16bits followed by 8bits
  - MCU LCD interface : i-8080 with up to 24bits RGB
  - 5 display layers :
    - One background layer with programmable 24bits color
    - One video layer (win0)
      - RGB888, ARGB888, RGB565, YUV422, YUV420, AYUV
      - maximum resolution is 1920x1080
      - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
      - 256 level alpha blending
      - Support transparency color key

- Support 3D display
- One video layer (win1)
  - RGB888, ARGB888, RGB565, YUV422, YUV420,AYUV
  - maximum resolution is 1920x1080
  - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
  - 256 level alpha blending
  - Support transparency color key
- One OSD layer(win2)
  - RGB888, ARGB888, RGB565, 1/2/4/8BPP
  - 256 level alpha blending
  - transparency color key
- Hardware cursor(win3)
  - 2BPP
  - Maximum resolution 64x64
  - 3-color and transparent mode
  - 2-color + transparency + tran_invert mode
  - 16 level alpha blending

- Support 180 rotation in combined mode with LCDC or separately mode
- 3 x 256 x 8 bits display LUTs
- Win0 and Win1 layer overlay exchangeable
- Support color space conversion :
  YUV2RGB(rec601-mpeg/rec601-jpeg/rec709) and RGB2YUV
- Deflicker support for interlace output
- Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation

1.2.11 Audio Interface

- I2S/PCM with 8ch
  - Up to 8 channels (4xTX , 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM cannot be used at the same time

- I2S/PCM with 2ch
  - 2 independent 2ch I2S/PCM interface
  - Up to 2 channels (2xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM cannot be used at the same time

- SPDIF
  - Audio resolution : 16bits/20bits/24bits
  - Software configurable sample rates (48KHz, 44.1KHz, 32KHz)
  - Stereo voice replay with 2 channels

1.2.12 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - Support FIFO over-run and under-run prevention by stopping card clock

automatically
- 4bits data bus width

- High-speed ADC & TS stream interface
  - Support dual-channel 8bits/10bits interface
  - DMA-based and interrupt-based operation
  - Support 8bits TS stream interface
  - Support PID filter operation
    - Combined with high-speed ADC interface to implement filter from original TS data
    - Provide PID filter up to 64 channels PID simultaneously
    - Support sync-byte detection in transport packet head
    - Support packet lost mechanism in condition of limited bandwidth

- MAC 10/100M Ethernet Controller
  - IEEE802.3u compliant Ethernet Media Access Controller(MAC)
  - 10Mbps and 100Mbps compatible
  - Automatic retry and automatic collision frame deletion
  - Full duplex support
  - PAUSE full-duplex flow-control support
  - Address filtering(broadcast, multicast, logical, physical)
  - Support only RMII(Reduced MII) mode
  - In RMII mode, clock can be from RK3066 or external ethernet PHY

- SPI Controller
  - Two on-chip SPI controller inside RK3066
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- Uart Controller
  - Four on-chip uart controller inside RK3066
  - DMA-based or interrupt-based operation
  - Embedded two 32Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Auto flow control mode is only for UART0, UART1, UART2

- I2C controller
  - Five on-chip I2C controller in RK3066
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - 6 groups of GPIO (GPIO0~GPIO4, GPIO6), 32 GPIOs per group in GPIO0~GPIO4, and 16GPIOs in GPIO6, totally have 176 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A9
  - GPIO6 can be used to wakeup system from stop/sleep/power-off mode
  - All of pullup GPIOs are software-programmable for pullup resistor or not
  - All of pulldown GPIOs are software-programmable for pulldown resistor

or not
- All of GPIOs are pullup or pulldown in default except GPIO1[5] mux with PWM3 after power-on-reset
- All of GPIOs are always in input direction in default after power-on-reset

- USB Host2.0
  - Compatible with usb host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB otg2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

- HDMI TX 1.4
  - HDMI version 1.4a, HDCP revision 1.4 and DVI version 1.0 compliant transmitter
  - Supports DTV from 480i to 1080i/p HD resolution, and PC from VGA to UXGA
  - Supports 3D and 2k x 4k video resolution output
  - Programmable 2-way color space converter
  - Compliant with EIA/CEA-861D
  - Deep color supported up to 12bit per pixel.
  - xvYCC Enhanced Colorimetry
  - Gamut Metadata transmission
  - Supports RGB, YCbCr digital video input format includes ITU.656
  - 36bit RGB/YCbCr 4:4:4 16/20/24bit YCbCr 4:2:2 8/10/12bit YCbCr 4:2:2 (ITU.601 and 656)
  - Supports standard SPDIF for stereo or compressed audio up to 192KHz
  - Support PCM, Dolby digital, DTS digital audio transmission through 4bits I2S up to 8 channel IEC60958 or IEC61937 compatible
  - 1bit audio format(Super Audio CD)
  - High-bitrate compressed audio formats
  - Master I2C interface for DDC connection
  - Configuration registers programmable via parallel interface
  - Wide range channel speed up to 2.2Gbps
  - Programmable PLL characteristics, channel delay, and transmitter pre-emphasis rate
  - Small ISI jitter by full differential data path

1.2.13 Others

- Temperature Sensor

- SAR-ADC(Successive Approximation Register)
  - 4-channel single-ended 10-bit SAR analog-to-digital converter
  - Conversion speed range is from 0.1 to 1 MSPS
  - SAR-ADC clock must be less than 1MHz
  - DNL less than ±1 LSB , INL less than ±2.0 LSB
  - Power down current is about 1uA

- Power supply is 2.5V (±10%) for analog interface

- eFuse
  - 256bits (32x8) high-density electrical Fuse
  - Programming condition : VQPS must be 2.5V(±10%)
  - Program time is about 4~6us
  - Read condition : VQPS must be 0V or floating or 2.5V(±10%)
  - Provide power-down and standby mode

- Package Type
  - TFBGA453 (body: 19mm x 19mm; ball pitch : 0.8mm)

1.3 Block Diagram

The following diagram shows the basic block diagram for RK3066.

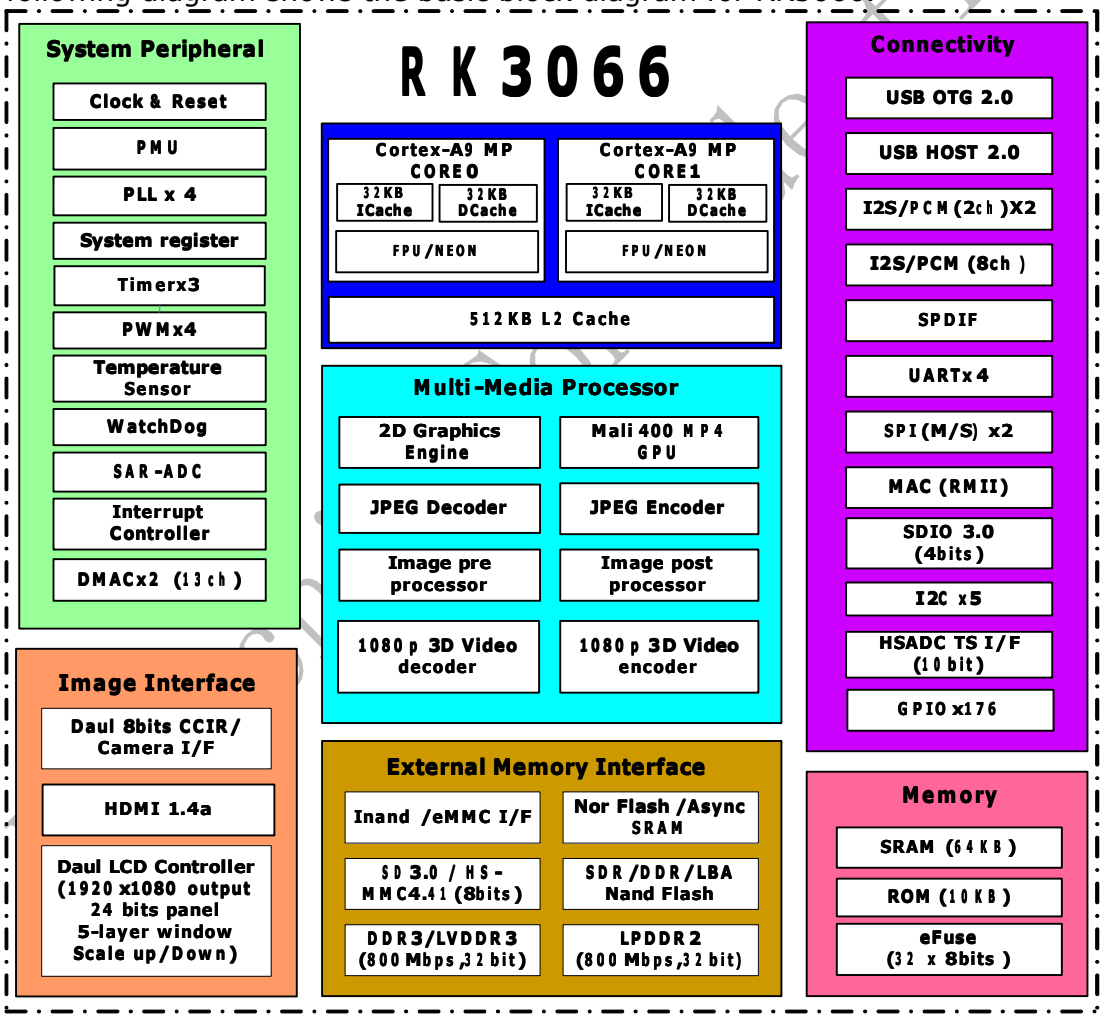

Fig. 1 RK3066 Block Diagram

CHAPTER 2 Package information

2.1 Dimension

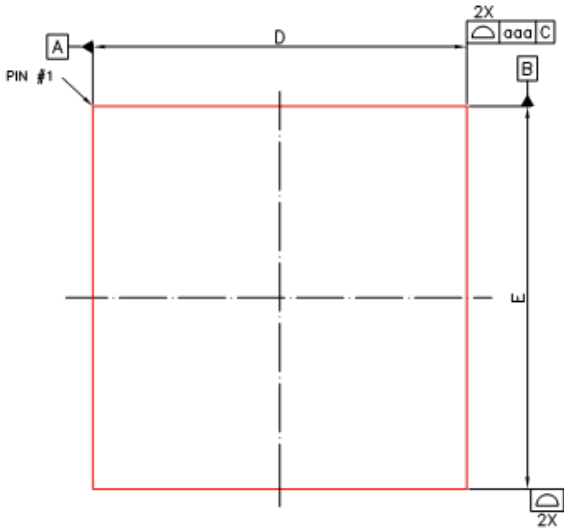

Fig. 2 RK3066 TFBGA453 Package Top View

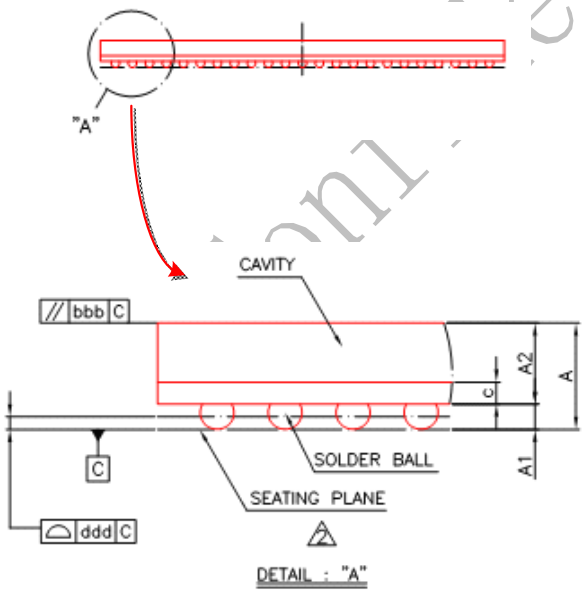

Fig. 2 RK3066 TFBGA453 Package Side View

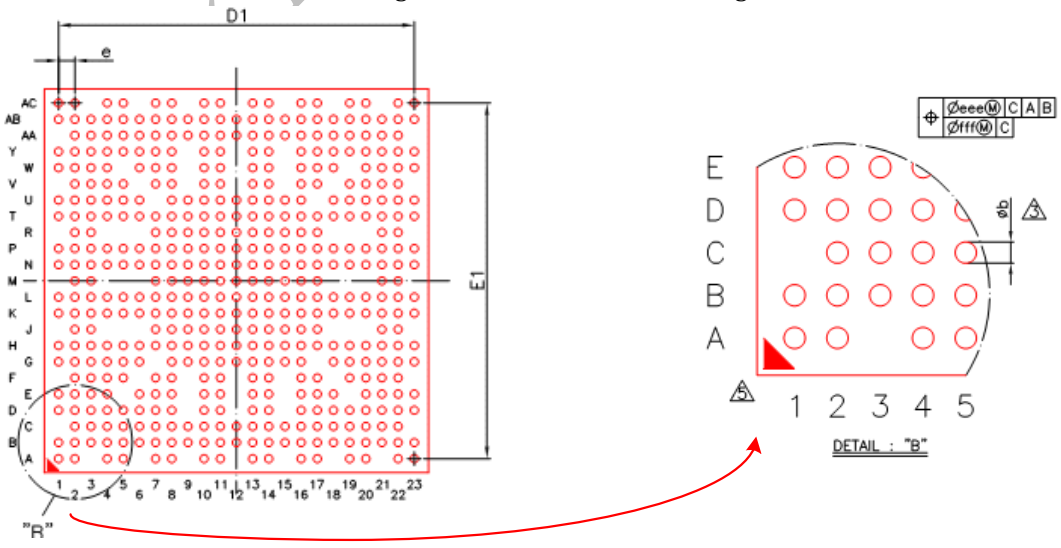

Fig. 4 RK3066 TFBGA453 Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.22	0.26	0.30	0.009	0.010	0.012
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.60	---	---	0.693	---
E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.15			0.006		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23/23			23/23		

Fig. 5 RK3066 TFBGA453 Package Dimension

2.2 Ball Map

Table 1 RK3066 Ball Mapping Diagram

	1	2	3	4	5	6	7	8	9	10	11	12
A	HDMI_TX2	HDMI_TX1	NP	HDMI_TX0	HDMI_TXC	NP	MDQ27	MDQS_B3	NP	MDQ10	MDQS_B1	NP
B	HDMI_TX2N	HDMI_TX1N	HDMI_AVSS	HDMI_TX0N	HDMI_TXCN	HDMI_AVSS	MDQ26	MDQS_3	MDQ8	MDQ11	MDQS_1	MDQ15
C	NP	LCD0_D2	LCD0_D1	LCD0_D0	HDMI_AVSS	HDMI_REXT	MDQ24	MDQ31	MDM1	MDQ9	MDQ14	MRESET
D	LCD0_D4	LCD0_D6	LCD0_D3	LCD0_DEN	LCD0_VSYNC	LCD0_HSYNC	MDQ25	MDQ29	NP	MDQ12	MCKE1	NP
E	LCD0_D12	LCD0_D10	LCD0_D9	LCD0_D7	NP	LCD0_DCLK	MDM3	MDQ28	NP	MDQ30	MDQ13	NP
F	NP	LCD0_D16	LCD0_D11	LCD0_D8	LCD0_D5	NP	HDMIVDD_1V1	HDMIAVDD_2V5	NP	MVDD	MVDD	NP
G	LCD0_D19	LCD0_D18	LCD0_D17	LCD0_D14	LCD0_D13	LCD0_D15	NP	HDMI_AVSS	HDMI_AVSS	MVDD	CVDD_1V1	VSS
H	GPIO2_A2/LCD1_D2/SMC_A6	LCD0_D22	LCD0_D21	LCD0_D20	LCD0_D23	GPIO2_A0/LCD1_D0/SMC_A4	CVDD_1V1	VSS	VSS	VSS	VSS	VSS
J	NP	GPIO2_A1/LCD1_D1/SMC_A5	GPIO2_B5/LCD1_D13/SMC_A17/TS_VALID	NP	NP	NP	LCD0_VCC1	VSS	VSS	VSS	VSS	VSS
K	GPIO2_C4/LCD1_D20/SPI1_CSN0/TS_D1	GPIO2_C3/LCD1_D19/SPI1_CLK/TS_D0	GPIO2_C2/LCD1_D18/SMC_BIS_N1/TS_D5	GPIO2_C1/LCD1_D17/SMC_BIS_N0/TS_D6	GPIO2_B7/LCD1_D15/SMC_A19/TS_D7	GPIO2_B6/LCD1_D14/SMC_A18/TS_SYNC	LCD0_VCC0	VSS	VSS	VSS	VSS	VSS
L	GPIO2_C5/LCD1_D21/SPI1_TXD/TS_D2	GPIO2_C6/LCD1_D22/SPI1_RXD/TS_D3	GPIO2_C7/LCD1_D23/SPI1_CSN1/TS_D4	CIF0_D3	GPIO2_C0/LCD1_D16/GPS_CLK/TS_CLKO	CIF0_D2	LCD1_VCC	VSS	VSS	VSS	VSS	VSS
M	NP	CIF0_D5	CIF0_D4	NP	NP	NP	CIF0_VCC	VSS	VSS	VSS	VSS	VSS
N	CIF0_D6	CIF0_D7	CIF0_D8	CIF0_VSYNC	AVDD	CIF1_VCC	CVDD_1V1	VSS	VSS	VSS	VSS	VSS
P	CIF0_D9	CIF0_HREF	CIF0_CLKIN	GPIO1_B5/CIF0_D1	AVDD	AVDD	VSS	VSS	VSS	VSS	VSS	VSS

R	NP	GPIO1_B3/CIF0_CLKO	GPIO1_B4/CIF0_D0	NP	NP	NP	VSS	VSS	VSS	VSS	VSS	VSS
T	GPIO1_B6/CIF0_D10	GPIO1_B7/CIF0_D11	GPIO3_A2/I2C3_SDA	GPIO1_C4/CIF1_D6/RMII_RX_ERR	AVDD	AVDD	VSS	VSS	VSS	VSS	AVSS_APLL	AVSS_DPLL
U	GPIO3_A3/I2C3_SCL	GPIO1_C0/CIF1_D2/RMII_CLKO	GPIO1_C1/CIF1_D3/RMII_TX_EN	GPIO1_C5/CIF1_D7/RMII_CRS_DVALID	AVDD	AVDD	NP	AVDD	AVDD	APLL_1V1	DPLL_1V1	C/GPLL_1V1
V	NP	GPIO1_C2/CIF1_D4/RMII_TXD1	GPIO1_C3/CIF1_D5/RMII_TXD0	GPIO1_C7/CIF1_D9/RMII_RXD0	AVDD	NP	AVDD	AVDD	NP	AVDD_COM	ADCVDD_2V5	NP
W	GPIO1_C6/CIF1_D8/RMII_RXD1	GPIO1_D0/CIF1_VSYNC/MII_MDCLK	GPIO1_D1/CIF1_HREF/MII_MDCLK	GPIO1_D2/CIF1_CLKIN	NP	ADC_IN0	ADC_IN2	ADC_IN1	NP	GPIO6_B0	GPIO6_A0	NP
Y	GPIO1_D7/CIF1_CLKO	GPIO1_D6/CIF1_D11	GPIO3_A5/I2C4_SCL	GPIO3_A4/I2C4_SDA	GPIO6_A4	GPIO6_A5	NPOR	GPIO6_A6	NP	GPIO3_C6/SDMMC1_DET	GPIO1_A1/UART0_TX	NP
AA	NP	GPIO6_B2	GPIO6_A1	CLK32K_IN	GPIO6_A3	OTG_RKELVIN	GPIO1_A4/UART1_RX/SPI0_CSN0	GPIO3_D2/SDMMC1_INT	GPIO3_C3/SDMMC1_D2	GPIO3_C4/SDMMC1_D3	GPIO1_A2/UART0_CTSN	GPIO3_C5/SDMMC1_CLKO
AB	CPU_PWROFF	GPIO6_B1	GPIO6_A2	OTG_ID	OTG_VBUS	GPIO1_A6/UART1_CTSN/SPI0_RXD	GPIO1_A7/UART1_RTSN/SPI0_TXD	GPIO3_C0/SDMMC1_CMD	GPIO3_C2/SDMMC1_D1	VSS	XOUT24M	GPIO1_A0/UART0_RX
AC	CORE_PWROFF	GPIO6_B3	NP	GPIO6_A7	GPIO1_A5/UART1_TX/SPI0_CLK	NP	GPIO4_B7/SPI0_CSN1	GPIO3_C1/SDMMC1_D0	NP	GPIO1_A3/UART0_RTSN	XIN24M	NP
	1	2	3	4	5	6	7	8	9	10	11	12

	13	14	15	16	17	18	19	20	21	22	23
A	MCKE0	MBA0	NP	MCK_N	MA1	NP	MA7	MA11	NP	MDQS_B2	MDQ20
B	MCSN0	MBA1	MA0	MCK	MA4	MA6	MA8	MODT0	MDQ16	MDQS_2	MDQ21
C	MWEN	MBA2	MA3	VSS	MA5	MA9	MA13	MODT1	MDM2	MDQ17	NP
D	MCASN	MRASN	NP	MA14	MDQ19	MA10	MA12	VSS	MDQ22	MDQ23	MDM0
E	MCSN1	MA2	NP	MDQ18	MDQ0	MDQ3	NP	MDQ2	MDQ1	MDQS_0	MDQS_B0
F	MVREF	MVDD	NP	MVDD	MVDD	NP	MDQ4	MDQ7	MDQ5	MDQ6	NP
G	MVDD	MVDD	MPZQ	CVDD_1V1	NP	GPIO2_D5/I2C0_SCL	GPIO2_D4/I2C0_SDA	TRSTN	TMS/PLL_BYPASS	TDI/CPR_BYPASS	GPIO6_B4
H	VSS	VSS	VSS	VSS	VCCIO1	GPIO0_A6/HOST_DRV_VBUS	GPIO0_A2/HDMI_I2C_SDA	PWM2/GPIO0_D6	PWM1/GPIO0_A4	TDO	TCK/HSSCAN_SHIFT_CLOCK
J	VSS	VSS	VSS	VSS	CVDD_1V1	NP	NP	NP	PWM3/GPIO0_D7	GPIO0_A5/OTG_DRV_VBUS	NP

K	VSS	VSS	VSS	VSS	VCCIO0	GPIO3_D5/UART3_CTSN	GPIO3_D4/UART3_TX	GPIO3_B5/SDMMC0_D3	GPIO0_B4/I2S0_SDO0	GPIO2_D7/I2C1_SCL	GPIO3_A0/I2C2_SDA
L	VSS	VSS	VSS	VSS	CVDD_1V1	GPIO3_D6/UART3_RTSN	GPIO3_D3/UART3_RX	GPIO3_B6/SDMMC0_DET	GPIO0_A7/I2S0_SDI	GPIO1_B2/SPDIF_TX	GPIO2_D6/I2C1_SDA
M	VSS	VSS	VSS	VSS	VSS	NP	NP	NP	GPIO3_B2/SDMMC0_D0	GPIO0_B7/I2S0_SDO3	NP
N	VSS	VSS	VSS	VSS	FLASH_VCC	GPIO4_B0/FLASH_CSN1	GPIO3_B7/SDMMC0_WP	FLASH_RDN	GPIO3_D7/FLASH_DQS/EMMC_CLKO	GPIO1_B0/UART2_RX	GPIO0_B6/I2S0_SDO2
P	VSS	VSS	VSS	VSS	CVDD_1V1	FLASH_D0/EMMC_D0	GPIO0_D0/I2S2_CLK/SMCCSN0	GPIO0_D1/I2S2_SCLK/SMC_WEN	GPIO4_B2/FLASH_CSN3/EMMC_RSTNO	GPIO3_B1/SDMMC0_CMD	GPIO0_B5/I2S0_SDO1
R	VSS	VSS	VSS	VSS	SMC_VCC	NP	NP	NP	GPIO0_B3/I2S0_LRCK_TX	GPIO0_B2/I2S0_LRCK_RX	NP
T	AVSS_C/GPLL	VSS	VSS	VSS	CVDD_1V1	GPIO0_C6/TRACE_CLK/SMC_A2	GPIO4_C3/SMC_D3/TRACE_D3	FLASH_ALE	GPIO3_B4/SDMMC0_D2	GPIO0_B0/I2S0_CLK	GPIO0_B1/I2S0_SCLK
U	PVDD_1V1	USBVDD_1V1	USBVDD_2V5	AP0_VCC	NP	GPIO4_D4/SMC_D12/TRACE_D12	GPIO4_C5/SMC_D5/TRACE_D5	FLASH_RDY	GPIO4_B1/FLASH_CSN2/EMMC_CMD	GPIO3_B0/SDMMC0_CLKO	GPIO3_B3/SDMMC0_D1
V	PVCC_3V3	USBVDD_3V3	NP	AP1_VCC	GPIO4_C4/SMC_D4/TRACE_D4	NP	GPIO4_C6/SMC_D6/TRACE_D6	FLASH_D5/EMMC_D5	GPIO0_D4/I2S2_SDI/SMC_A0	GPIO3_A7/SDMMC0_PWREN	NP
W	HOST_RKELVIN	EFUSE	NP	GPIO4_C2/SMC_D2/TRACE_D2	GPIO4_C1/SMC_D1/TRACE_D1	GPIO4_C7/SMC_D7/TRACE_D7	NP	GPIO4_D2/SMC_D10/TRACE_D10	GPIO0_D3/I2S2_LRCK_TX/SMC_ADVN	FLASH_D3/EMMC_D3	GPIO3_A6/SDMMC0_RSTNO
Y	GPIO3_D0/SDMMC1_PWREN	GPIO0_C4/I2S1_SDI	NP	GPIO0_A1/HDMI_I2C_SCL	GPIO4_C0/SMC_D0/TRACE_D0	GPIO4_D0/SMC_D8/TRACE_D8	GPIO3_A1/I2C2_SCL	GPIO4_D6/SMC_D14/TRACE_D14	GPIO0_D2/I2S2_LRCK_RX/SMC_OEN	FLASH_D4/EMMC_D4	FLASH_CSN0
AA	GPIO3_C7/SDMMC1_WP	GPIO3_D1/SDMMC1_BACKEND	PWM0/GPIO0_A3	VSS	VSS	GPIO4_D1/SMC_D9/TRACE_D9	GPIO0_A0/HDMI_HPD	GPIO4_D7/SMC_D15/TRACE_D15	FLASH_D1/EMMC_D1	FLASH_D6/EMMC_D6	NP
AB	GPIO0_C1/I2S1_SCLK	GPIO0_C3/I2S1_LRCK_TX	GPIO0_C5/I2S1_SDO	OTG_DM	HOST_DM	GPIO4_D3/SMC_D11/TRACE_D11	GPIO1_B1/UART2_TX	GPIO0_C7/TRACE_CTL/SMC_A3	FLASH_D2/EMMC_D2	FLASH_D7/EMMC_D7	FLASH_WP/EMMC_PWREN
AC	GPIO0_C0/I2S1_CLK	GPIO0_C2/I2S1_LRCK_RX	NP	OTG_DP	HOST_DP	NP	GPIO4_D5/SMC_D13/TRACE_D13	GPIO0_D5/I2S2_SDO/SMC_A1	NP	FLASH_CLE	FLASH_WRN
	13	14	15	16	17	18	19	20	21	22	23

2.3 Pin Number Order

Table 2 RK3066 Pin Number Order Information

Ball #	Pin Name	Ball #	Pin Name
A1	HDMI_TX2	B1	HDMI_TX2N
A2	HDMI_TX1	B2	HDMI_TX1N
A3	NP	B3	HDMI_AVSS
A4	HDMI_TX0	B4	HDMI_TX0N
A5	HDMI_TXC	B5	HDMI_TXCN
A6	NP	B6	HDMI_AVSS
A7	MDQ27	B7	MDQ26
A8	MDQS_B3	B8	MDQS_3
A9	NP	B9	MDQ8
A10	MDQ10	B10	MDQ11
A11	MDQS_B1	B11	MDQS_1
A12	NP	B12	MDQ15
A13	MCKE0	B13	MCSN0
A14	MBA0	B14	MBA1
A15	NP	B15	MA0
A16	MCK_N	B16	MCK
A17	MA1	B17	MA4
A18	NP	B18	MA6
A19	MA7	B19	MA8
A20	MA11	B20	MODT0
A21	NP	B21	MDQ16
A22	MDQS_B2	B22	MDQS_2
A23	MDQ20	B23	MDQ21
C1	NP	D1	LCD0_D4
C2	LCD0_D2	D2	LCD0_D6
C3	LCD0_D1	D3	LCD0_D3
C4	LCD0_D0	D4	LCD0_DEN
C5	HDMI_AVSS	D5	LCD0_VSYNC
C6	HDMI_REXT	D6	LCD0_HSYNC
C7	MDQ24	D7	MDQ25
C8	MDQ31	D8	MDQ29
C9	MDM1	D9	NP
C10	MDQ9	D10	MDQ12
C11	MDQ14	D11	MCKE1
C12	MRESET	D12	NP
C13	MWEN	D13	MCASN
C14	MBA2	D14	MRASN
C15	MA3	D15	NP
C16	VSS	D16	MA14
C17	MA5	D17	MDQ19
C18	MA9	D18	MA10
C19	MA13	D19	MA12
C20	MODT1	D20	VSS
C21	MDM2	D21	MDQ22
C22	MDQ17	D22	MDQ23
C23	NP	D23	MDM0
E1	LCD0_D12	F1	NP
E2	LCD0_D10	F2	LCD0_D16
E3	LCD0_D9	F3	LCD0_D11
E4	LCD0_D7	F4	LCD0_D8
E5	NP	F5	LCD0_D5

E6	LCD0_DCLK	F6	NP
E7	MDM3	F7	HDMIVDD_1V1
E8	MDQ28	F8	HDMIAVDD_2V5
E9	NP	F9	NP
E10	MDQ30	F10	MVDD
E11	MDQ13	F11	MVDD
E12	NP	F12	NP
E13	MCSN1	F13	MVREF
E14	MA2	F14	MVDD
E15	NP	F15	NP
E16	MDQ18	F16	MVDD
E17	MDQ0	F17	MVDD
E18	MDQ3	F18	NP
E19	NP	F19	MDQ4
E20	MDQ2	F20	MDQ7
E21	MDQ1	F21	MDQ5
E22	MDQS_0	F22	MDQ6
E23	MDQS_B0	F23	NP
G1	LCD0_D19	H1	GPIO2_A2/LCD1_D2/SMC_A6
G2	LCD0_D18	H2	LCD0_D22
G3	LCD0_D17	H3	LCD0_D21
G4	LCD0_D14	H4	LCD0_D20
G5	LCD0_D13	H5	LCD0_D23
G6	LCD0_D15	H6	GPIO2_A0/LCD1_D0/SMC_A4
G7	NP	H7	CVDD_1V1
G8	HDMI_AVSS	H8	VSS
G9	HDMI_AVSS	H9	VSS
G10	MVDD	H10	VSS
G11	CVDD_1V1	H11	VSS
G12	VSS	H12	VSS
G13	MVDD	H13	VSS
G14	MVDD	H14	VSS
G15	MPZQ	H15	VSS
G16	CVDD_1V1	H16	VSS
G17	NP	H17	VCCIO1
G18	GPIO2_D5/I2C0_SCL	H18	GPIO0_A6/HOST_DRV_VBUS
G19	GPIO2_D4/I2C0_SDA	H19	GPIO0_A2/HDMI_I2C_SDA
G20	TRSTN	H20	PWM2/GPIO0_D6
G21	TMS/PLL_BYPASS	H21	PWM1/GPIO0_A4
G22	TDI/CPR_BYPASS	H22	TDO
G23	GPIO6_B4	H23	TCK/HSSCAN_SHIFT_CLOCK
J1	NP	K1	GPIO2_C4/LCD1_D20/SPI1_CSN0/TS_D1
J2	GPIO2_A1/LCD1_D1/SMC_A5	K2	GPIO2_C3/LCD1_D19/SPI1_CLK/TS_D0
J3	GPIO2_B5/LCD1_D13/SMC_A17/TS_VALID	K3	GPIO2_C2/LCD1_D18/SMC_BIS_N1/TS_D5
J4	NP	K4	GPIO2_C1/LCD1_D17/SMC_BIS_N0/TS_D6
J5	NP	K5	GPIO2_B7/LCD1_D15/SMC_A19/TS_D7
J6	NP	K6	GPIO2_B6/LCD1_D14/SMC_A18/TS_SYNC
J7	LCD0_VCC1	K7	LCD0_VCC0
J8	VSS	K8	VSS
J9	VSS	K9	VSS
J10	VSS	K10	VSS
J11	VSS	K11	VSS
J12	VSS	K12	VSS
J13	VSS	K13	VSS
J14	VSS	K14	VSS
J15	VSS	K15	VSS

J16	VSS	K16	VSS
J17	CVDD_1V1	K17	VCCIO0
J18	NP	K18	GPIO3_D5/UART3_CTSN
J19	NP	K19	GPIO3_D4/UART3_TX
J20	NP	K20	GPIO3_B5/SDMMC0_D3
J21	PWM3/GPIO0_D7	K21	GPIO0_B4/I2S0_SDO0
J22	GPIO0_A5/OTG_DRV_VBUS	K22	GPIO2_D7/I2C1_SCL
J23	NP	K23	GPIO3_A0/I2C2_SDA
L1	GPIO2_C5/LCD1_D21/SPI1_TXD/TS_D2	M1	NP
L2	GPIO2_C6/LCD1_D22/SPI1_RXD/TS_D3	M2	CIF0_D5
L3	GPIO2_C7/LCD1_D23/SPI1_CSN1/TS_D4	M3	CIF0_D4
L4	CIF0_D3	M4	NP
L5	GPIO2_C0/LCD1_D16/GPS_CLK/TS_CLKO	M5	NP
L6	CIF0_D2	M6	NP
L7	LCD1_VCC	M7	CIF0_VCC
L8	VSS	M8	VSS
L9	VSS	M9	VSS
L10	VSS	M10	VSS
L11	VSS	M11	VSS
L12	VSS	M12	VSS
L13	VSS	M13	VSS
L14	VSS	M14	VSS
L15	VSS	M15	VSS
L16	VSS	M16	VSS
L17	CVDD_1V1	M17	VSS
L18	GPIO3_D6/UART3_RTSN	M18	NP
L19	GPIO3_D3/UART3_RX	M19	NP
L20	GPIO3_B6/SDMMC0_DET	M20	NP
L21	GPIO0_A7/I2S0_SDI	M21	GPIO3_B2/SDMMC0_D0
L22	GPIO1_B2/SPDIF_TX	M22	GPIO0_B7/I2S0_SDO3
L23	GPIO2_D6/I2C1_SDA	M23	NP
N1	CIF0_D6	P1	CIF0_D9
N2	CIF0_D7	P2	CIF0_HREF
N3	CIF0_D8	P3	CIF0_CLKIN
N4	CIF0_VSYNC	P4	GPIO1_B5/CIF0_D1
N5	AVDD	P5	AVDD
N6	CIF1_VCC	P6	AVDD
N7	CVDD_1V1	P7	VSS
N8	VSS	P8	VSS
N9	VSS	P9	VSS
N10	VSS	P10	VSS
N11	VSS	P11	VSS
N12	VSS	P12	VSS
N13	VSS	P13	VSS
N14	VSS	P14	VSS
N15	VSS	P15	VSS
N16	VSS	P16	VSS
N17	FLASH_VCC	P17	CVDD_1V1
N18	GPIO4_B0/FLASH_CSN1	P18	FLASH_D0/EMMC_D0
N19	GPIO3_B7/SDMMC0_WP	P19	GPIO0_D0/I2S2_CLK/SMC_CSN0
N20	FLASH_RDN	P20	GPIO0_D1/I2S2_SCLK/SMC_WEN
N21	GPIO3_D7/FLASH_DQS/EMMC_CLKO	P21	GPIO4_B2/FLASH_CSN3/EMMC_RSTNO
N22	GPIO1_B0/UART2_RX	P22	GPIO3_B1/SDMMC0_CMD
N23	GPIO0_B6/I2S0_SDO2	P23	GPIO0_B5/I2S0_SDO1
R1	NP	T1	GPIO1_B6/CIF0_D10
R2	GPIO1_B3/CIF0_CLKO	T2	GPIO1_B7/CIF0_D11

R3	GPIO1_B4/CIF0_D0	T3	GPIO3_A2/I2C3_SDA
R4	NP	T4	GPIO1_C4/CIF1_D6/RMII_RX_ERR
R5	NP	T5	AVDD
R6	NP	T6	AVDD
R7	VSS	T7	VSS
R8	VSS	T8	VSS
R9	VSS	T9	VSS
R10	VSS	T10	VSS
R11	VSS	T11	AVSS_APLL
R12	VSS	T12	AVSS_DPLL
R13	VSS	T13	AVSS_C/GPLL
R14	VSS	T14	VSS
R15	VSS	T15	VSS
R16	VSS	T16	VSS
R17	SMC_VCC	T17	CVDD_1V1
R18	NP	T18	GPIO0_C6/TRACE_CLK/SMC_A2
R19	NP	T19	GPIO4_C3/SMC_D3/TRACE_D3
R20	NP	T20	FLASH_ALE
R21	GPIO0_B3/I2S0_LRCK_TX	T21	GPIO3_B4/SDMMC0_D2
R22	GPIO0_B2/I2S0_LRCK_RX	T22	GPIO0_B0/I2S0_CLK
R23	NP	T23	GPIO0_B1/I2S0_SCLK
U1	GPIO3_A3/I2C3_SCL	V1	NP
U2	GPIO1_C0/CIF1_D2/RMII_CLKO	V2	GPIO1_C2/CIF1_D4/RMII_TXD1
U3	GPIO1_C1/CIF1_D3/RMII_TX_EN	V3	GPIO1_C3/CIF1_D5/RMII_TXD0
U4	GPIO1_C5/CIF1_D7/RMII_CRS_DVALID	V4	GPIO1_C7/CIF1_D9/RMII_RXD0
U5	AVDD	V5	AVDD
U6	AVDD	V6	NP
U7	NP	V7	AVDD
U8	AVDD	V8	AVDD
U9	AVDD	V9	NP
U10	APLL_1V1	V10	AVDD_COM
U11	DPLL_1V1	V11	ADCVDD_2V5
U12	C/GPLL_1V1	V12	NP
U13	PVDD_1V1	V13	PVCC_3V3
U14	USBVDD_1V1	V14	USBVDD_3V3
U15	USBVDD_2V5	V15	NP
U16	AP0_VCC	V16	AP1_VCC
U17	NP	V17	GPIO4_C4/SMC_D4/TRACE_D4
U18	GPIO4_D4/SMC_D12/TRACE_D12	V18	NP
U19	GPIO4_C5/SMC_D5/TRACE_D5	V19	GPIO4_C6/SMC_D6/TRACE_D6
U20	FLASH_RDY	V20	FLASH_D5/EMMC_D5
U21	GPIO4_B1/FLASH_CSN2/EMMC_CMD	V21	GPIO0_D4/I2S2_SDI/SMC_A0
U22	GPIO3_B0/SDMMC0_CLKO	V22	GPIO3_A7/SDMMC0_PWREN
U23	GPIO3_B3/SDMMC0_D1	V23	NP
W1	GPIO1_C6/CIF1_D8/RMII_RXD1	Y1	GPIO1_D7/CIF1_CLKO
W2	GPIO1_D0/CIF1_VSYNC/MII_MD	Y2	GPIO1_D6/CIF1_D11
W3	GPIO1_D1/CIF1_HREF/MII_MDCLK	Y3	GPIO3_A5/I2C4_SCL
W4	GPIO1_D2/CIF1_CLKIN	Y4	GPIO3_A4/I2C4_SDA
W5	NP	Y5	GPIO6_A4
W6	ADC_IN0	Y6	GPIO6_A5
W7	ADC_IN2	Y7	NPOR
W8	ADC_IN1	Y8	GPIO6_A6
W9	NP	Y9	NP
W10	GPIO6_B0	Y10	GPIO3_C6/SDMMC1_DET
W11	GPIO6_A0	Y11	GPIO1_A1/UART0_TX
W12	NP	Y12	NP

W13	HOST_RKELVIN	Y13	GPIO3_D0/SDMMC1_PWREN
W14	EFUSE	Y14	GPIO0_C4/I2S1_SDI
W15	NP	Y15	NP
W16	GPIO4_C2/SMC_D2/TRACE_D2	Y16	GPIO0_A1/HDMI_I2C_SCL
W17	GPIO4_C1/SMC_D1/TRACE_D1	Y17	GPIO4_C0/SMC_D0/TRACE_D0
W18	GPIO4_C7/SMC_D7/TRACE_D7	Y18	GPIO4_D0/SMC_D8/TRACE_D8
W19	NP	Y19	GPIO3_A1/I2C2_SCL
W20	GPIO4_D2/SMC_D10/TRACE_D10	Y20	GPIO4_D6/SMC_D14/TRACE_D14
W21	GPIO0_D3/I2S2_LRCK_TX/SMC_ADVN	Y21	GPIO0_D2/I2S2_LRCK_RX/SMC_OEN
W22	FLASH_D3/EMMC_D3	Y22	FLASH_D4/EMMC_D4
W23	GPIO3_A6/SDMMC0_RSTNO	Y23	FLASH_CSN0
AA1	NP	AB1	CPU_PWROFF
AA2	GPIO6_B2	AB2	GPIO6_B1
AA3	GPIO6_A1	AB3	GPIO6_A2
AA4	CLK32K_IN	AB4	OTG_ID
AA5	GPIO6_A3	AB5	OTG_VBUS
AA6	OTG_RKELVIN	AB6	GPIO1_A6/UART1_CTSN/SPI0_RXD
AA7	GPIO1_A4/UART1_RX/SPI0_CSN0	AB7	GPIO1_A7/UART1_RTSN/SPI0_TXD
AA8	GPIO3_D2/SDMMC1_INT	AB8	GPIO3_C0/SDMMC1_CMD
AA9	GPIO3_C3/SDMMC1_D2	AB9	GPIO3_C2/SDMMC1_D1
AA10	GPIO3_C4/SDMMC1_D3	AB10	VSS
AA11	GPIO1_A2/UART0_CTSN	AB11	XOUT24M
AA12	GPIO3_C5/SDMMC1_CLKO	AB12	GPIO1_A0/UART0_RX
AA13	GPIO3_C7/SDMMC1_WP	AB13	GPIO0_C1/I2S1_SCLK
AA14	GPIO3_D1/SDMMC1_BACKEND	AB14	GPIO0_C3/I2S1_LRCK_TX
AA15	PWM0/GPIO0_A3	AB15	GPIO0_C5/I2S1_SDO
AA16	VSS	AB16	OTG_DM
AA17	VSS	AB17	HOST_DM
AA18	GPIO4_D1/SMC_D9/TRACE_D9	AB18	GPIO4_D3/SMC_D11/TRACE_D11
AA19	GPIO0_A0/HDMI_HPD	AB19	GPIO1_B1/UART2_TX
AA20	GPIO4_D7/SMC_D15/TRACE_D15	AB20	GPIO0_C7/TRACE_CTL/SMC_A3
AA21	FLASH_D1/EMMC_D1	AB21	FLASH_D2/EMMC_D2
AA22	FLASH_D6/EMMC_D6	AB22	FLASH_D7/EMMC_D7
AA23	NP	AB23	FLASH_WP/EMMC_PWREN
AC1	CORE_PWROFF	AC13	GPIO0_C0/I2S1_CLK
AC2	GPIO6_B3	AC14	GPIO0_C2/I2S1_LRCK_RX
AC3	NP	AC15	NP
AC4	GPIO6_A7	AC16	OTG_DP
AC5	GPIO1_A5/UART1_TX/SPI0_CLK	AC17	HOST_DP
AC6	NP	AC18	NP
AC7	GPIO4_B7/SPI0_CSN1	AC19	GPIO4_D5/SMC_D13/TRACE_D13
AC8	GPIO3_C1/SDMMC1_D0	AC20	GPIO0_D5/I2S2_SDO/SMC_A1
AC9	NP	AC21	NP
AC10	GPIO1_A3/UART0_RTSN	AC22	FLASH_CLE
AC11	XIN24M	AC23	FLASH_WRN
AC12	NP		

2.4 RK3066 power/ground IO descriptions

Table 3 RK3066 Power/Ground IO informations

Group	Ball #	Descriptions
GND	H8, H9, H10, H11, H12, H13, H14, H15,H16,J8,J9,J10,J11,J12,J13,J14,J15,J16,K8,K9,K10,K11,K12,K13,K14,K15,K16,L8,L9,L10,L11,L12,L13,L14,L15,L16,M8,M9,M10,M11,M12,M13,M14,M15,M16,N8,N9,N10,N11,N12,N13,N14,N15,N16,P8,P9,P10,P11,P12,P13,P14,P15,P16,R8,R9,R10,R11,R12,R13,R14,R15,R16,T8,T9,T10,P7,R7,T7,T14,T15,T16,G12,G16,M17,D20,AB10,AA16,AA17	Internal Core Ground and Digital IO Ground
AVDD	N5,P5,P6,T5,T6,U5,U6,V5,U8,U9,V7,V8	Internal CPU Power (@ cpu frequency <= 1GHz)
		Internal CPU Power (@ cpu frequency <= 1.3GHz)
CVDD	G11,G16,H7,J17,L17,N7,P17,T17	Internal Core Power
PVDD	U13	Internal RTC Domain Power
PVCC	V13	RTC Domain Digital GPIO Power
VDDIO0	K17	Digital GPIO Power
VDDIO1	H17	
LCD0_VCC0	K7	LCDC Digital IO Power
LCD0_VCC1	J7	
LCD1_VCC	L7	
CIF0_VCC	M7	Camera Digital IO Power
CIF1_VCC	N6	
SMC_VCC	R17	SMC Digital IO Power
FLASH_VCC	N17	Nand Flash Digital IO Power
AP0_VCC	U16	I2S/UART/I2C for Mobile phone Digital IO Power
AP1_VCC	V16	

MVDD	F10,F11,F14,F16,F17,G10,G13,G14	DDR3 Digital IO Power LPDDR2 Digital IO Power
AVSS_APLL	T11	ARM PLL Analog Ground
AVDD_APLL	U10	ARM PLL Analog Power
AVSS_DPLL	T12	DDR PLL Analog Ground
AVDD_DPLL	U11	DDR PLL Analog Power
AVSS_CGPLL	T13	CODEC/GENERAL PLL Analog Ground
AVDD_CGPLL	U12	CODEC/GENERAL PLL Analog Power
VDDA_SARADCVDDA_TSADC	V11	SAR-ADC Analog PowerTS-ADC Analog Power
OTG_DVDDHOST_DVDD	U14	USB OTG2.0/Host2.0 Digital Power
OTG_VDD25HOST_VDD25	U15	USB OTG2.0/Host2.0 Analog Power
OTG_VDD33HOST_VDD33	V14	USB OTG2.0/Host2.0 Analog Power
EFUSE_VDDQ	W14	eFuse IO Digital Power
HDMI_AVSS	B3,B6,C5,G8,G9	HDMI Analog Ground

2.5 RK3066 function IO descriptions

Table 4 RK3066 IO descriptions

Pin Name	Ball #	func0	func1	func2	func3	Pad bype①	Drive ②	pull up/ down	Reset State③	Power supply⑤
Left Side④										
LCDC0_DATA[7]	E4	LCDC0_DATA[7]				I/O	8	N/A	I	LCD0_VCC0 LCD0_VCC1
LCDC0_DATA[8]	F4	LCDC0_DATA[8]				I/O	8	N/A	I	
LCDC0_DATA[9]	E3	LCDC0_DATA[9]				I/O	8	N/A	I	
LCDC0_DATA[10]	E2	LCDC0_DATA[10]				I/O	8	N/A	I	
LCDC0_DATA[11]	F3	LCDC0_DATA[11]				I/O	8	N/A	I	
LCDC0_DATA[12]	E1	LCDC0_DATA[12]				I/O	8	N/A	I	
LCDC0_DATA[13]	G5	LCDC0_DATA[13]				I/O	8	N/A	I	
LCDC0_DATA[14]	G4	LCDC0_DATA[14]				I/O	8	N/A	I	
LCDC0_DATA[15]	G6	LCDC0_DATA[15]				I/O	8	N/A	I	
LCDC0_DATA[16]	F2	LCDC0_DATA[16]				I/O	8	N/A	I	
LCDC0_DATA[17]	G3	LCDC0_DATA[17]				I/O	8	N/A	I	
LCDC0_DATA[18]	G2	LCDC0_DATA[18]				I/O	8	N/A	I	
LCDC0_DATA[19]	G1	LCDC0_DATA[19]				I/O	8	N/A	I	
LCDC0_DATA[20]	H4	LCDC0_DATA[20]				I/O	8	N/A	I	
LCDC0_DATA[21]	H3	LCDC0_DATA[21]				I/O	8	N/A	I	
LCDC0_DATA[22]	H2	LCDC0_DATA[22]				I/O	8	N/A	I	
LCDC0_DATA[23]	H5	LCDC0_DATA[23]				I/O	8	N/A	I	
GPIO2_A[0]	H6	GPIO2_A[0]	lcdc1_data0	smc_addr4		I/O	8	down	I	LCD1_VCC
GPIO2_A[1]	J2	GPIO2_A[1]	lcdc1_data1	smc_addr5		I/O	8	down	I	
GPIO2_A[2]	H1	GPIO2_A[2]	lcdc1_data2	smc_addr6		I/O	8	down	I	
GPIO2_B[5]	J3	GPIO2_B[5]	lcdc1_data13	smc_addr17	hsadc_data8	I/O	8	down	I	
GPIO2_B[6]	K6	GPIO2_B[6]	lcdc1_data14	smc_addr18	ts_sync	I/O	8	down	I	
GPIO2_B[7]	K5	GPIO2_B[7]	lcdc1_data15	smc_addr19	hsadc_data7	I/O	8	down	I	

GPIO2_C[0]	L5	GPIO2_C[0]	lcdc1_data16	gps_clk	hsadc_clkout	I/O	8	down	I	
GPIO2_C[1]	K4	GPIO2_C[1]	lcdc1_data17	smc_bls_n0	hsadc_data6	I/O	8	down	I	
GPIO2_C[2]	K3	GPIO2_C[2]	lcdc1_data18	smc_bls_n1	hsadc_data5	I/O	8	down	I	
GPIO2_C[3]	K2	GPIO2_C[3]	lcdc1_data19	spi1_clk	hsadc_data0	I/O	8	down	I	
GPIO2_C[4]	K1	GPIO2_C[4]	lcdc1_data20	spi1_csn0	hsadc_data1	I/O	8	down	I	
GPIO2_C[5]	L1	GPIO2_C[5]	lcdc1_data21	spi1_txd	hsadc_data2	I/O	8	down	I	
GPIO2_C[6]	L2	GPIO2_C[6]	lcdc1_data22	spi1_rxd	hsadc_data3	I/O	8	down	I	
GPIO2_C[7]	L3	GPIO2_C[7]	lcdc1_data23	spi1_csn1	hsadc_data4	I/O	8	down	I	
CIF0_DATAIN[2]	L6	CIF0_DATAIN[2]				I	8	down	I	CIF0_VCC
CIF0_DATAIN[3]	L4	CIF0_DATAIN[3]				I	8	down	I	
CIF0_DATAIN[4]	M3	CIF0_DATAIN[4]				I	8	down	I	
CIF0_DATAIN[5]	M2	CIF0_DATAIN[5]				I	8	down	I	
CIF0_DATAIN[6]	N1	CIF0_DATAIN[6]				I	8	down	I	
CIF0_DATAIN[7]	N2	CIF0_DATAIN[7]				I	8	down	I	
CIF0_DATAIN[8]	N3	CIF0_DATAIN[8]				I	8	down	I	
CIF0_DATAIN[9]	P1	CIF0_DATAIN[9]				I	8	down	I	
CIF0_VSYNC	N4	CIF0_VSYNC				I	8	down	I	
CIF0_HREF	P2	CIF0_HREF				I	8	down	I	
CIF0_CLKIN	P3	CIF0_CLKIN				I	8	down	I	
GPIO1_B[3]	R2	GPIO1_B[3]	cif0_clkout			I/O	4	down	I	
GPIO1_B[4]	R3	GPIO1_B[4]	cif0_data0			I/O	8	down	I	
GPIO1_B[5]	P4	GPIO1_B[5]	cif0_data1			I/O	8	down	I	
GPIO1_B[6]	T1	GPIO1_B[6]	cif0_data10			I/O	8	down	I	
GPIO1_B[7]	T2	GPIO1_B[7]	cif0_data11			I/O	8	down	I	
GPIO3_A[2]	T3	GPIO3_A[2]	i2c3_sda			I/O	8	up	I	
GPIO3_A[3]	U1	GPIO3_A[3]	i2c3_scl			I/O	8	up	I	
GPIO1_C[0]	U2	GPIO1_C[0]	cif1_data2	rmii_clkout	rmii_clkin	I/O	4	down	I	CIF1_VCC
GPIO1_C[1]	U3	GPIO1_C[1]	cif1_data3	rmii_tx_en		I/O	4	down	I	
GPIO1_C[2]	V2	GPIO1_C[2]	cif1_data4	rmii_txd1		I/O	4	down	I	

GPIO1_C[3]	V3	GPIO1_C[3]	cif1_data5	rmii_txd0		I/O	4	down	I	
GPIO1_C[4]	T4	GPIO1_C[4]	cif1_data6	rmii_rx_err		I/O	8	down	I	
GPIO1_C[5]	U4	GPIO1_C[5]	cif1_data7	rmii_crs_dvalid		I/O	8	down	I	
GPIO1_C[6]	W1	GPIO1_C[6]	cif1_data8	rmii_rxd1		I/O	8	down	I	
GPIO1_C[7]	V4	GPIO1_C[7]	cif1_data9	rmii_rxd0		I/O	8	down	I	
GPIO1_D[0]	W2	GPIO1_D[0]	cif1_vsync	mii_md		I/O	8	down	I	
GPIO1_D[1]	W3	GPIO1_D[1]	cif1_href	mii_mdclk		I/O	8	down	I	
GPIO1_D[2]	W4	GPIO1_D[2]	cif1_clkin			I/O	8	down	I	
GPIO1_D[7]	Y1	GPIO1_D[7]	cif1_clkout			I/O	4	down	I	
GPIO1_D[6]	Y2	GPIO1_D[6]	cif1_data11			I/O	8	down	I	
GPIO3_A[4]	Y4	GPIO3_A[4]	i2c4_sda			I/O	8	up	I	
GPIO3_A[5]	Y3	GPIO3_A[5]	i2c4_scl			I/O	8	up	I	
Bottom Side										
ARMP_power_feedback	V10	1.1V				P	N/A	N/A	N/A	
VDDA_SARADC	V11	2.5V				AP	N/A	N/A	N/A	SARADC Domain
SARADC_AIN[2]	W7	SARADC_AIN[2]				A	N/A	N/A	N/A	
SARADC_AIN[1]	W8	SARADC_AIN[1]				A	N/A	N/A	N/A	
SARADC_AIN[0]	W6	SARADC_AIN[0]				A	N/A	N/A	N/A	
AVSS_CGPLL	T13	Analog Ground				AG	N/A	N/A	N/A	PLL Domain
AVDD_CGPLL	U12	1.1V				AP	N/A	N/A	N/A	
AVSS_APLL	T11	Analog Ground				AG	N/A	N/A	N/A	
AVDD_APLL	U10	1.1V				AP	N/A	N/A	N/A	
AVDD_DPLL	U11	1.1V				AP	N/A	N/A	N/A	
AVSS_DPLL	T12	Analog Ground				AG	N/A	N/A	N/A	
CPU_PWROFF	AB1	CPU_PWROFF				O	8	down	O	PVCC
CORE_PWROFF	AC1	CORE_PWROFF				O	8	down	O	
GPIO6_B[0]	W10	GPIO6_B[0]				I/O	8	down	I	
GPIO6_B[1]	AB2	GPIO6_B[1]				I/O	8	down	I	

GPIO6_B[2]	AA2	GPIO6_B[2]				I/O	8	down	I	
GPIO6_B[3]	AC2	GPIO6_B[3]				I/O	8	down	I	
GPIO6_A[0]	W11	GPIO6_A[0]				I/O	8	up	I	
GPIO6_A[1]	AA3	GPIO6_A[1]				I/O	8	up	I	
GPIO6_A[2]	AB3	GPIO6_A[2]				I/O	8	up	I	
GPIO6_A[3]	AA5	GPIO6_A[3]				I/O	8	up	I	
GPIO6_A[4]	Y5	GPIO6_A[4]				I/O	8	up	I	
GPIO6_A[5]	Y6	GPIO6_A[5]				I/O	8	up	I	
CLK32K	AA4	CLK32K				I	N/A	down	I	
XIN24M	AC11	XIN24M				I	N/A	N/A	I	
XOUT24M	AB11	XOUT24M				O	N/A	N/A	O	
GPIO6_A[6]	Y8	GPIO6_A[6]				I/O	8	up	I	
GPIO6_A[7]	AC4	GPIO6_A[7]				I/O	8	up	I	
NPOR	Y7	NPOR				I	8	N/A	I	
OTG_DVDD	U14	OTG_DVDD				DP	N/A	N/A	N/A	USB Domain
OTG_ID	AB4	OTG_ID				A	N/A	N/A	N/A	
OTG_VBUS	AB5	OTG_VBUS				A	N/A	N/A	N/A	
OTG_VDD33	V14	OTG_VDD33				AP	N/A	N/A	N/A	
OTG_DP	AC16	OTG_DP				A	N/A	N/A	N/A	
OTG_DM	AB16	OTG_DM				A	N/A	N/A	N/A	
OTG_RKELVIN	AA6	OTG_RKELVIN				A	N/A	N/A	N/A	
OTG_VDD25	U15	OTG_VDD25				AP	N/A	N/A	N/A	
HOST_DP	AC17	HOST_DP				A	N/A	N/A	N/A	
HOST_DM	AB17	HOST_DM				A	N/A	N/A	N/A	
HOST_RKELVIN	W13	HOST_RKELVIN				A	N/A	N/A	N/A	
EFUSE_VDDQ	W14	EFUSE_VDDQ				AP	N/A	N/A	N/A	EFUSE Domain
GPIO1_A[4]	AA7	GPIO1_A[4]	uart1_sin	spi0_csn0		I/O	8	up	I	AP1_VCC
GPIO1_A[5]	AC5	GPIO1_A[5]	uart1_sout	spi0_clk		I/O	8	down	I	

GPIO1_A[6]	AB6	GPIO1_A[6]	uart1_cts_n	spi0_rxd		I/O	8	up	I	
GPIO1_A[7]	AB7	GPIO1_A[7]	uart1_rts_n	spi0_txd		I/O	8	up	I	
GPIO4_B[7]	AC7	GPIO4_B[7]	spi0_csn1			I/O	8	up	I	
GPIO3_D[2]	AA8	GPIO3_D[2]	sdmmc1_int_n			I/O	8	up	I	AP0_VCC
GPIO3_C[0]	AB8	GPIO3_C[0]	sdmmc1_cmd			I/O	4	up	I	
GPIO3_C[1]	AC8	GPIO3_C[1]	sdmmc1_data0			I/O	4	up	I	
GPIO3_C[2]	AB9	GPIO3_C[2]	sdmmc1_data1			I/O	4	up	I	
GPIO3_C[3]	AA9	GPIO3_C[3]	sdmmc1_data2			I/O	4	up	I	
GPIO3_C[4]	AA10	GPIO3_C[4]	sdmmc1_data3			I/O	4	up	I	
GPIO3_C[5]	AA12	GPIO3_C[5]	sdmmc1_clkout			I/O	4	down	I	
GPIO3_C[6]	Y10	GPIO3_C[6]	sdmmc1_detect_n			I/O	8	up	I	
GPIO3_C[7]	AA13	GPIO3_C[7]	sdmmc1_write_prt			I/O	8	down	I	
GPIO3_D[0]	Y13	GPIO3_D[0]	sdmmc1_pwr_en			I/O	8	down	I	
GPIO3_D[1]	AA14	GPIO3_D[1]	sdmmc1_backend_pwr			I/O	8	down	I	
GPIO0_C[4]	Y14	GPIO0_C[4]	i2s1_sdi			I/O	8	down	I	
Right Side										
GPIO0_C[0]	AC13	GPIO0_C[0]	i2s1_clk			I/O	4	down	I	AP0_VCC
GPIO0_C[1]	AB13	GPIO0_C[1]	i2s1_sclk			I/O	4	down	I	
GPIO0_C[2]	AC14	GPIO0_C[2]	i2s1_lrck_rx			I/O	4	down	I	
GPIO0_C[3]	AB14	GPIO0_C[3]	i2s1_lrck_tx			I/O	4	down	I	
GPIO0_C[5]	AB15	GPIO0_C[5]	i2s1_sdo			I/O	4	down	I	
GPIO1_A[0]	AB12	GPIO1_A[0]	uart0_sin			I/O	8	up	I	
GPIO1_A[1]	Y11	GPIO1_A[1]	uart0_sout			I/O	8	down	I	
GPIO1_A[2]	AA11	GPIO1_A[2]	uart0_cts_n			I/O	8	up	I	
GPIO1_A[3]	AC10	GPIO1_A[3]	uart0_rts_n			I/O	8	up	I	
GPIO4_C[0]	Y17	GPIO4_C[0]	smc_data0	trace_data0		I/O	4	up	I	SMC_VCC
GPIO4_C[1]	W17	GPIO4_C[1]	smc_data1	trace_data1		I/O	4	up	I	
GPIO4_C[2]	W16	GPIO4_C[2]	smc_data2	trace_data2		I/O	4	up	I	
GPIO4_C[3]	T19	GPIO4_C[3]	smc_data3	trace_data3		I/O	4	up	I	

GPIO4_C[4]	V17	GPIO4_C[4]	smc_data4	trace_data4		I/O	4	up	I	
GPIO4_C[5]	U19	GPIO4_C[5]	smc_data5	trace_data5		I/O	4	up	I	
GPIO4_C[6]	V19	GPIO4_C[6]	smc_data6	trace_data6		I/O	4	down	I	
GPIO4_C[7]	W18	GPIO4_C[7]	smc_data7	trace_data7		I/O	4	down	I	
GPIO4_D[0]	Y18	GPIO4_D[0]	smc_data8	trace_data8		I/O	4	down	I	
GPIO4_D[1]	AA18	GPIO4_D[1]	smc_data9	trace_data9		I/O	4	down	I	
GPIO4_D[2]	W20	GPIO4_D[2]	smc_data10	trace_data10		I/O	4	down	I	
GPIO4_D[3]	AB18	GPIO4_D[3]	smc_data11	trace_data11		I/O	4	down	I	
GPIO4_D[4]	U18	GPIO4_D[4]	smc_data12	trace_data12		I/O	4	down	I	
GPIO4_D[5]	AC19	GPIO4_D[5]	smc_data13	trace_data13		I/O	4	down	I	
GPIO4_D[6]	Y20	GPIO4_D[6]	smc_data14	trace_data14		I/O	4	down	I	
GPIO4_D[7]	AA20	GPIO4_D[7]	smc_data15	trace_data15		I/O	4	down	I	
GPIO0_C[7]	AB20	GPIO0_C[7]	trace_ctl	smc_addr3		I/O	4	down	I	
GPIO0_C[6]	T18	GPIO0_C[6]	trace_clk	smc_addr2		I/O	4	down	I	
GPIO0_D[5]	AC20	GPIO0_D[5]	i2s2_sdo	smc_addr1		I/O	4	down	I	
GPIO0_D[4]	V21	GPIO0_D[4]	i2s2_sdi	smc_addr0		I/O	4	down	I	
GPIO0_D[3]	W21	GPIO0_D[3]	i2s2_lrck_tx	smc_adv_n		I/O	4	up	I	
GPIO0_D[2]	Y21	GPIO0_D[2]	i2s2_lrck_rx	smc_oe_n		I/O	4	up	I	
GPIO0_D[0]	P19	GPIO0_D[0]	i2s2_clk	smc_csn0		I/O	4	up	I	
GPIO0_D[1]	P20	GPIO0_D[1]	i2s2_sclk	smc_we_n		I/O	4	up	I	
FLASH_DATA[0]	P18	FLASH_DATA[0]	emmc_data0			I/O	8	down	I	FLASH_VCC
FLASH_DATA[1]	AA21	FLASH_DATA[1]	emmc_data1			I/O	8	down	I	
FLASH_DATA[2]	AB21	FLASH_DATA[2]	emmc_data2			I/O	8	down	I	
FLASH_DATA[3]	W22	FLASH_DATA[3]	emmc_data3			I/O	8	down	I	
FLASH_DATA[4]	Y22	FLASH_DATA[4]	emmc_data4			I/O	8	down	I	
FLASH_DATA[5]	V20	FLASH_DATA[5]	emmc_data5			I/O	8	down	I	
FLASH_DATA[6]	AA22	FLASH_DATA[6]	emmc_data6			I/O	8	down	I	
FLASH_DATA[7]	AB22	FLASH_DATA[7]	emmc_data7			I/O	8	down	I	
FLASH_RDY	U20	FLASH_RDY				I/O	8	up	I	

FLASH_ALE	T20	FLASH_ALE				O	4	down	O	
FLASH_CLE	AC22	FLASH_CLE				O	4	down	O	
FLASH_RDN	N20	FLASH_RDN				O	8	up	O	
FLASH_WRN	AC23	FLASH_WRN				O	8	up	O	
FLASH_WP	AB23	FLASH_WP	emmc_pwr_en			O	4	down	O	
FLASH_CSN0	Y23	FLASH_CSN0				O	4	up	O	
GPIO4_B[0]	N18	GPIO4_B[0]	flash_csn1			I/O	4	up	I	
GPIO4_B[1]	U21	GPIO4_B[1]	flash_csn2	emmc_cmd		I/O	4	up	I	
GPIO4_B[2]	P21	GPIO4_B[2]	flash_csn3	emmc_rstn_out		I/O	4	up	I	
GPIO3_D[7]	N21	GPIO3_D[7]	flash_dqs	emmc_clkout		I/O	8	up	I	
GPIO3_B[6]	L20	GPIO3_B[6]	sdmmc0_detect_n			I/O	8	up	I	VCCIO0 VCCIO1
GPIO3_B[7]	N19	GPIO3_B[7]	sdmmc0_write_prt			I/O	8	down	I	
GPIO3_A[6]	W23	GPIO3_A[6]	sdmmc0_rstn_out			I/O	8	up	I	
GPIO3_A[7]	V22	GPIO3_A[7]	sdmmc0_pwr_en			I/O	8	down	I	
GPIO3_B[0]	U22	GPIO3_B[0]	sdmmc0_clkout			I/O	4	down	I	
GPIO3_B[1]	P22	GPIO3_B[1]	sdmmc0_cmd			I/O	4	up	I	
GPIO3_B[2]	M21	GPIO3_B[2]	sdmmc0_data0			I/O	4	up	I	
GPIO3_B[3]	U23	GPIO3_B[3]	sdmmc0_data1			I/O	4	up	I	
GPIO3_B[4]	T21	GPIO3_B[4]	sdmmc0_data2			I/O	4	up	I	
GPIO3_B[5]	K20	GPIO3_B[5]	sdmmc0_data3			I/O	4	up	I	
GPIO0_A[7]	L21	GPIO0_A[7]	i2s0_sdi			I/O	8	down	I	
GPIO0_B[0]	T22	GPIO0_B[0]	i2s0_clk			I/O	4	down	I	
GPIO0_B[1]	T23	GPIO0_B[1]	i2s0_sclk			I/O	4	down	I	
GPIO0_B[2]	R22	GPIO0_B[2]	i2s0_lrck_rx			I/O	4	down	I	
GPIO0_B[3]	R21	GPIO0_B[3]	i2s0_lrck_tx			I/O	4	down	I	
GPIO0_B[4]	K21	GPIO0_B[4]	i2s0_sdo0			I/O	4	down	I	
GPIO0_B[5]	P23	GPIO0_B[5]	i2s0_sdo1			I/O	4	down	I	
GPIO0_B[6]	N23	GPIO0_B[6]	i2s0_sdo2			I/O	4	up	I	
GPIO0_B[7]	M22	GPIO0_B[7]	i2s0_sdo3			I/O	4	up	I	

GPIO1_B[2]	L22	GPIO1_B[2]	spdif_tx			I/O	4	down	I	
GPIO1_B[0]	N22	GPIO1_B[0]	uart2_sin			I/O	8	up	I	
GPIO1_B[1]	AB19	GPIO1_B[1]	uart2_sout			I/O	8	down	I	
GPIO2_D[6]	L23	GPIO2_D[6]	i2c1_sda			I/O	8	up	I	
GPIO2_D[7]	K22	GPIO2_D[7]	i2c1_scl			I/O	8	up	I	
GPIO3_A[0]	K23	GPIO3_A[0]	i2c2_sda			I/O	8	up	I	
GPIO3_A[1]	Y19	GPIO3_A[1]	i2c2_scl			I/O	8	up	I	
GPIO3_D[3]	L19	GPIO3_D[3]	uart3_sin			I/O	8	up	I	
GPIO3_D[4]	K19	GPIO3_D[4]	uart3_sout			I/O	8	down	I	
GPIO3_D[5]	K18	GPIO3_D[5]	uart3_cts_n			I/O	8	up	I	
GPIO3_D[6]	L18	GPIO3_D[6]	uart3_rts_n			I/O	8	up	I	
GPIO0_A[0]	AA19	GPIO0_A[0]	hdmi_hot_plug_in			I/O	8	down	I	
GPIO0_A[1]	Y16	GPIO0_A[1]	hdmi_i2c_scl			I/O	8	up	I	
GPIO0_A[2]	H19	GPIO0_A[2]	hdmi_i2c_sda			I/O	8	up	I	
GPIO0_A[3]	AA15	GPIO0_A[3]	pwm0			I/O	8	down	I	
GPIO0_A[4]	H21	GPIO0_A[4]	pwm1			I/O	8	down	I	
GPIO0_A[5]	J22	GPIO0_A[5]	otg_drv_vbus			I/O	8	down	I	
GPIO0_A[6]	H18	GPIO0_A[6]	host_drv_vbus			I/O	8	down	I	
GPIO0_D[6]	H20	GPIO0_D[6]	pwm2			I/O	8	down	I	
GPIO0_D[7]	J21	GPIO0_D[7]	pwm3			I/O	8	down	I	
TDO	H22	TDO				O	8	N/A	O	
TCK	H23	TCK				I	8	up	I	
TRST_N	G20	TRST_N				I	8	down	I	
TDI	G22	TDI				I	8	up	I	
TMS	G21	TMS				I/O	8	up	I	
GPIO2_D[4]	G19	GPIO2_D[4]	i2c0_sda			I/O	8	up	I	
GPIO2_D[5]	G18	GPIO2_D[5]	i2c0_scl			I/O	8	up	I	
GPIO6_B[4]	G23	GPIO6_B[4]				I/O	8	up	I	
Top Side										

DDR_DQ[7]	F20	DDR_DQ[7]				I/O	N/A	N/A	I	
DDR_DQ[6]	F22	DDR_DQ[6]				I/O	N/A	N/A	I	
DDR_DQ[5]	F21	DDR_DQ[5]				I/O	N/A	N/A	I	
DDR_DQ[4]	F19	DDR_DQ[4]				I/O	N/A	N/A	I	
DDR_DQS[0]	E22	DDR_DQS[0]				I/O	N/A	N/A	I	
DDR_DQS_B[0]	E23	DDR_DQS_B[0]				I/O	N/A	N/A	I	
DDR_DQ[3]	E18	DDR_DQ[3]				I/O	N/A	N/A	I	
DDR_DQ[2]	E20	DDR_DQ[2]				I/O	N/A	N/A	I	
DDR_DQ[1]	E21	DDR_DQ[1]				I/O	N/A	N/A	I	
DDR_DQ[0]	E17	DDR_DQ[0]				I/O	N/A	N/A	I	
DDR_DM[0]	D23	DDR_DM[0]				I/O	N/A	N/A	I	
DDR_VREF	F13	DDR_VREF				P	N/A	N/A	N/A	
DDR_DQ[23]	D22	DDR_DQ[23]				I/O	N/A	N/A	I	
DDR_DQ[22]	D21	DDR_DQ[22]				I/O	N/A	N/A	I	
DDR_DQ[21]	B23	DDR_DQ[21]				I/O	N/A	N/A	I	MVDD
DDR_DQ[20]	A23	DDR_DQ[20]				I/O	N/A	N/A	I	
DDR_DQS[2]	B22	DDR_DQS[2]				I/O	N/A	N/A	I	
DDR_DQS_B[2]	A22	DDR_DQS_B[2]				I/O	N/A	N/A	I	
DDR_DQ[19]	D17	DDR_DQ[19]				I/O	N/A	N/A	I	
DDR_DQ[18]	E16	DDR_DQ[18]				I/O	N/A	N/A	I	
DDR_DQ[17]	C22	DDR_DQ[17]				I/O	N/A	N/A	I	
DDR_DQ[16]	B21	DDR_DQ[16]				I/O	N/A	N/A	I	
DDR_DM[2]	C21	DDR_DM[2]				I/O	N/A	N/A	I	
DDR_PZQ	G15	DDR_PZQ				I/O	N/A	N/A	I	
DDR_ODT[1]	C20	DDR_ODT[1]				O	N/A	N/A	O	
DDR_ODT[0]	B20	DDR_ODT[0]				O	N/A	N/A	O	
DDR_ADDR[14]	D16	DDR_ADDR[14]				O	N/A	N/A	O	
DDR_ADDR[13]	C19	DDR_ADDR[13]				O	N/A	N/A	O	
DDR_ADDR[12]	D19	DDR_ADDR[12]				O	N/A	N/A	O	

DDR_ADDR[11]	A20	DDR_ADDR[11]				O	N/A	N/A	O	
DDR_ADDR[10]	D18	DDR_ADDR[10]				O	N/A	N/A	O	
DDR_ADDR[9]	C18	DDR_ADDR[9]				O	N/A	N/A	O	
DDR_ADDR[8]	B19	DDR_ADDR[8]				O	N/A	N/A	O	
DDR_ADDR[7]	A19	DDR_ADDR[7]				O	N/A	N/A	O	
DDR_ADDR[6]	B18	DDR_ADDR[6]				O	N/A	N/A	O	
DDR_ADDR[5]	C17	DDR_ADDR[5]				O	N/A	N/A	O	
DDR_CK	B16	DDR_CK				O	N/A	N/A	O	
DDR_CK_N	A16	DDR_CK_N				O	N/A	N/A	O	
DDR_ADDR[4]	B17	DDR_ADDR[4]				O	N/A	N/A	O	
DDR_ADDR[3]	C15	DDR_ADDR[3]				O	N/A	N/A	O	
DDR_ADDR[2]	E14	DDR_ADDR[2]				O	N/A	N/A	O	
DDR_ADDR[1]	A17	DDR_ADDR[1]				O	N/A	N/A	O	
DDR_ADDR[0]	B15	DDR_ADDR[0]				O	N/A	N/A	O	
DDR_BA[2]	C14	DDR_BA[2]				O	N/A	N/A	O	
DDR_BA[1]	B14	DDR_BA[1]				O	N/A	N/A	O	
DDR_BA[0]	A14	DDR_BA[0]				O	N/A	N/A	O	
DDR_RASN	D14	DDR_RASN				O	N/A	N/A	O	
DDR_CASN	D13	DDR_CASN				O	N/A	N/A	O	
DDR_WEN	C13	DDR_WEN				O	N/A	N/A	O	
DDR_CSN[1]	E13	DDR_CSN[1]				O	N/A	N/A	O	
DDR_CSN[0]	B13	DDR_CSN[0]				O	N/A	N/A	O	
DDR_CKE1	D11	DDR_CKE1				O	N/A	N/A	O	
DDR_CKE0	A13	DDR_CKE0				O	N/A	N/A	O	
DDR_RESET	C12	DDR_RESET				O	N/A	N/A	O	
DDR_DQ[15]	B12	DDR_DQ[15]				I/O	N/A	N/A	I	
DDR_DQ[14]	C11	DDR_DQ[14]				I/O	N/A	N/A	I	
DDR_DQ[13]	E11	DDR_DQ[13]				I/O	N/A	N/A	I	
DDR_DQ[12]	D10	DDR_DQ[12]				I/O	N/A	N/A	I	

DDR_DQS[1]	B11	DDR_DQS[1]				I/O	N/A	N/A	I	
DDR_DQS_B[1]	A11	DDR_DQS_B[1]				I/O	N/A	N/A	I	
DDR_DQ[11]	B10	DDR_DQ[11]				I/O	N/A	N/A	I	
DDR_DQ[10]	A10	DDR_DQ[10]				I/O	N/A	N/A	I	
DDR_DQ[9]	C10	DDR_DQ[9]				I/O	N/A	N/A	I	
DDR_DQ[8]	B9	DDR_DQ[8]				I/O	N/A	N/A	I	
DDR_DM[1]	C9	DDR_DM[1]				I/O	N/A	N/A	I	
DDR_DQ[31]	C8	DDR_DQ[31]				I/O	N/A	N/A	I	
DDR_DQ[30]	E10	DDR_DQ[30]				I/O	N/A	N/A	I	
DDR_DQ[29]	D8	DDR_DQ[29]				I/O	N/A	N/A	I	
DDR_DQ[28]	E8	DDR_DQ[28]				I/O	N/A	N/A	I	
DDR_DQS[3]	B8	DDR_DQS[3]				I/O	N/A	N/A	I	
DDR_DQS_B[3]	A8	DDR_DQS_B[3]				I/O	N/A	N/A	I	
DDR_DQ[27]	A7	DDR_DQ[27]				I/O	N/A	N/A	I	
DDR_DQ[26]	B7	DDR_DQ[26]				I/O	N/A	N/A	I	
DDR_DQ[25]	D7	DDR_DQ[25]				I/O	N/A	N/A	I	
DDR_DQ[24]	C7	DDR_DQ[24]				I/O	N/A	N/A	I	
DDR_DM[3]	E7	DDR_DM[3]				I/O	N/A	N/A	I	
HDMI_VDDLA	F7	1.1V				AP	N/A	N/A	N/A	
HDMI_PVDD	F8	2.5V				AP	N/A	N/A	N/A	
HDMI_REXT	C6	HDMI_REXT				A	N/A	N/A	N/A	
HDMI_TXC_N	B5	HDMI_TXC_N				A	N/A	N/A	N/A	
HDMI_TXC	A5	HDMI_TXC				A	N/A	N/A	N/A	
HDMI_AVDD25	F8	2.5V				AP	N/A	N/A	N/A	HDMI Domain
HDMI_TX0_N	B4	HDMI_TX0_N				A	N/A	N/A	N/A	
HDMI_TX0	A4	HDMI_TX0				A	N/A	N/A	N/A	
HDMI_TX1_N	B2	HDMI_TX1_N				A	N/A	N/A	N/A	
HDMI_TX1	A2	HDMI_TX1				A	N/A	N/A	N/A	
HDMI_TX2_N	B1	HDMI_TX2_N				A	N/A	N/A	N/A	

HDMI_TX2	A1	HDMI_TX2				A	N/A	N/A	N/A	
LCDC0_HSYNC	D6	LCDC0_HSYNC				I/O	4	N/A	I	
LCDC0_DCLK	E6	LCDC0_DCLK				I/O	12	N/A	I	
LCDC0_VSYNC	D5	LCDC0_VSYNC				I/O	4	N/A	I	
LCDC0_DEN	D4	LCDC0_DEN				I/O	4	N/A	I	
LCDC0_DATA[0]	C4	LCDC0_DATA[0]				I/O	8	N/A	I	
LCDC0_DATA[1]	C3	LCDC0_DATA[1]				I/O	8	N/A	I	LCD0_VCC0
LCDC0_DATA[2]	C2	LCDC0_DATA[2]				I/O	8	N/A	I	
LCDC0_DATA[3]	D3	LCDC0_DATA[3]				I/O	8	N/A	I	
LCDC0_DATA[4]	D1	LCDC0_DATA[4]				I/O	8	N/A	I	
LCDC0_DATA[5]	F5	LCDC0_DATA[5]				I/O	8	N/A	I	
LCDC0_DATA[6]	D2	LCDC0_DATA[6]				I/O	8	N/A	I	

Notes : ①: *Pad types : I = input , O = output , I/O = input/output (bidirectional) ,*
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: *Output Drive Unit is mA , only Digital IO have drive value*

③: *Reset state : I = input without any pull resistor , O = output without any pull resistor ,*

④: *It is die location. For examples, "Left side" means that all the related IOs are always in left side of die*

⑤: *Power supply means that all the related IOs is in these IO power domain. If multiple powers is included, they are connected together in one IO power ring*

CHAPTER 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 5 RK3066 absolute maximum ratings

Paramerters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	ARMP, COREP_EFUSE, COREP_LCDC0,COREP_LCDC1, COREP_CIF0,COREP_CIF1, COREP_CIF1_ARM, COREP_PMU,COREP_SMC, COREP_AP0,COREP_AP1, COREP_FLASH,COREP_GPIO, OTG_DVDD, HOST_DVDD, VDDCORE_BL0~VDDCORE_BL3, VDDCORE_CMD	1.21	V
DC supply voltage for Digital GPIO (except for SAR-ADC, TS-ADC, PLL, USB, DDR IO)	IOP_GPIO, IOP_LCD0, IOP_LCD1, IOP_CIF0,IOP_CIF1, IOP_ARM,IOP_PMU, IOP_SMC, IOP_FLASH, IOP_AP0, IOP_AP1, IOP_EFUSE	3.6	V
DC supply voltage for DDR IO	VDDIO_BL0~VDDIO_BL3,VDDIO_CMD	1.65	V
DC supply voltage for Analog part of SAR-ADC	VDDA_SARADC	2.75	V
DC supply voltage for Analog part of TS-ADC	VDDA_TSADC	2.75	V
DC supply voltage for Analog part of PLL	AVDD_APLL,AVDD_DPLL, AVDD_CPLL,AVDD_GPLL	1.21	V
DC supply voltage for Analog part of USB OTG/Host2.0	OTG_VDD25,HOST_VDD25 OTG_VDD33,HOST_VDD33	2.75 3.63	V
DC supply voltage for Analog part of HDMI	HDMI_VDDLA HDMI_PVDD,HDMI_AVDD25	1.21 2.75	V
DC supply voltage for Analog part of EFUSE	EFUSE_VDDQ	2.75	V
Analog Input voltage for SAR-ADC		2.75	V
Analog Input voltage for TS-ADC		2.75	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Analog input voltage for RKELVIN/ID of USB OTG/Host2.0		2.75	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIO		3.6	V
Storage Temperature		150	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

Table 6 RK3066 recommended operating conditions

Parameters	Symbol①	Min	Typ	Max	Units
Internal digital logic Power （except USB OTG)	ARMP, COREP_EFUSE, COREP_LCDC0,COREP_LCDC1, COREP_CIF0,COREP_CIF1, COREP_CIF1_ARM, COREP_PMU,COREP_SMC, COREP_AP0,COREP_AP1, COREP_FLASH,COREP_GPIO, VDDCORE_BL0~VDDCORE_BL3, VDDCORE_CMD	0.99	1.10	1.21	V
Digital GPIO Power(3.3V)	IOP_GPIO, IOP_SMC, IOP_EFUSE	3	3.3	3.6	V
Digital GPIO Power(3.3V/1.8V)	IOP_LCD0, IOP_LCD1, IOP_CIF0,IOP_CIF1, IOP_ARM,IOP_PMU, IOP_FLASH, IOP_AP0, IOP_AP1	3 1.62	3.3 1.8	3.6 1.98	V
DDR IO (DDR3 mode) Power	VDDIO_BL0~VDDIO_BL3, VDDIO_CMD	1.425	1.5	1.575	V
DDR IO (LPDDR2 mode) Power	VDDIO_BL0~VDDIO_BL3, VDDIO_CMD	1.14	1.2	1.30	V
DDR reference supply (VREF) Input	DDR_ISO_VREF[0], DDR_CMD_VREF[1], DDR_VREF[2], DDR_VREF[3]	0.49*VDDIO_BL$_i$ (i=0~3)	0.5*VDDIO_BL$_i$(i=0~3)	0.51*VDDIO_BL$_i$(i=0~3)	V
DDR External termination voltage		DDR_VREF[i] - 40mV (i=2~3)	DDR_VREF[i] (i=2~3)	DDR_VREF[i] + 40mV (i=2~3)	V
PLL Analog Power	AVDD_APLL, AVDD_DPLL, AVDD_CPLL, AVDD_GPLL,	0.99	1.1	1.21	V
SAR-ADC Analog Power	VDDA_SARADC	2.25	2.5	2.75	V
TS-ADC Analog Power	VDDA_TSADC	2.25	2.5	2.75	V
USB OTG/Host2.0 Digital Power	OTG_DVDD, HOST_DVDD	1.023	1.1	1.21	V
USB OTG/Host2.0 Analog Power(2.5V)	OTG_VDD25,HOST_VDD25	2.325	2.5	2.75	V
USB OTG/Host2.0 Analog Power(3.3V)	OTG_VDD33,HOST_VDD33	3.069	3.3	3.63	V
USB OTG/Host2.0 external resistor	REXT	42.768	43.2	43.632	Ohm
PLL input clock frequency		N/A	24	N/A	MHz

Operating Temperature		-40	25	85	℃

Notes : ①, Symbol name is same as the pin name in the io descriptions

3.3 DC Characteristics

Table 7 RK3066 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	V_{il}	-0.3	0	0.8	V
	Input High Voltage	V_{ih}	2	3.3	3.6	V
	Output Low Voltage	V_{ol}	N/A	0	0.4	V
	Output High Voltage	V_{oh}	2.4	3.3	N/A	V
	Threshold Point	V_t	1.34	1.46	1.6	V
	Threshold Point with Pullup Resistor Enabled	V_{tpu}	1.2	1.31	1.45	V
	Threshold Point with Pulldown Resistor Enabled	V_{tpd}	1.71	1.84	1.97	V
	Pullup Resistor	R_{pu}	41	60	91	Kohm
	Pulldown Resistor	R_{pd}	43	63	103	Kohm
Digital GPIO @1.8V	Input Low Voltage	V_{il}	-0.3	0	0.63	V
	Input High Voltage	V_{ih}	1.17	1.8	3.6	V
	Output Low Voltage	V_{ol}	N/A	0	0.45	V
	Output High Voltage	V_{oh}	1.35	1.8	N/A	V
	Threshold Point	V_t	0.77	0.84	0.92	V
	Threshold Point with Pullup Resistor Enabled	V_{tpu}	0.77	0.84	0.91	V
	Threshold Point with Pulldown Resistor Enabled	V_{tpd}	0.77	0.85	0.92	V
	Pullup Resistor	R_{pu}	79	129	218	Kohm
	Pulldown Resistor	R_{pd}	73	127	233	Kohm
DDR IO @DDR3 mode	Input High Voltage	V_{ih_ddr}	DDR_VREF[*i*] + 0.1 (i=2~3)	1.8	VDDIO_BL$_i$ (i=0~3)	V
	Input Low Voltage	V_{il_ddr}	-0.3	0	DDR_VREF[*i*] - 0.1 (i=2~3)	V
	Output High Voltage	V_{oh_ddr}	0.8 * VDDIO_BL$_i$ (i=0~3)	1.8	N/A	V
	Output Low Voltage	V_{ol_ddr}	N/A	0	0.2 * VDDIO_BL$_i$ (i=0~3)	V
	Input termination resistance(ODT) to VDDIO_BLi/2 (i=0~3)	R_{tt}	100 54 36	120 60 40	140 66 44	Ohm
DDR IO @LPDDR2 mode	Input High Voltage	V_{ih_ddr}	DDR_VREF[*i*]+ 0.13	1.2	VDDIO_BL$_i$ (i=0~3)	V

			(i=2~3)			
	Input Low Voltage	V_{il_ddr}	-0.3	0	DDR_VREF[*i*]- 0.13 (i=2~3)	V
	Output High Voltage	V_{oh_ddr}	0.9 * VDDIO_BL$_i$ (i=0~3)	1.2	N/A	V
	Output Low Voltage	V_{ol_ddr}	N/A	0	0.1 * VDDIO_BL$_i$ (i=0~3)	V

3.4 Electrical Characteristics for General IO

Table 8 RK3066 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	I_i	Vin = 3.3V or 0V	-10	N/A	10	uA
	Tri-state output leakage current	I_{oz}	Vout = 3.3V or 0V	-10	N/A	10	uA
	High level input current	I_{ih}	Vin = 3.3V, pulldown disabled	TBD	N/A	TBD	uA
			Vin = 3.3V, pulldown enabled	32	52	77	uA
	Low level input current	I_{il}	Vin = 0V, pullup disabled	TBD	N/A	TBD	uA
			Vin = 0V, pullup enabled	36	55	80	uA
Digital GPIO @1.8V	Input leakage current	I_i	Vin = 1.8V or 0V	-10	N/A	10	uA
	Tri-state output leakage current	I_{oz}	Vout = 1.8V or 0V	-10	N/A	10	uA
	High level input current	I_{ih}	Vin = 1.8V, pulldown disabled	TBD	N/A	TBD	uA
			Vin = 1.8V, pulldown enabled	7.7	14	25	uA
	Low level input current	I_{il}	Vin = 0V, pullup disabled	TBD	N/A	TBD	uA
			Vin = 0V, pullup enabled	8.3	14	23	uA

3.5 Electrical Characteristics for PLL

Table 9 RK3066 Electrical Characteristics for PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input clock frequency	F_{in}	$F_{in} = F_{ref} * NR$① @1.1V	0.183	24	1500	MHz
Comparison frequency	F_{ref}	$F_{ref} = F_{in} / NR$ @1.1V	0.183	N/A	1500	MHz
VCO operating range	F_{VCO}	$F_{VCO} = F_{ref} * NF$① @1.1V	300	N/A	1500	MHz
Output clock frequency	F_{out}	$F_{out} = F_{VCO} / NO$① @1.1V	18.75	N/A	1500	MHz
Lock time	T_{lt}	(NR * 500) / F_{in} @1.1V	N/A	N/A	N/A	N/A
Power consumption	N/A	F_{out} = 750MHz, NO = 1 @1.1V	N/A	3	N/A	mA

Notes : ①: *NR is the input divider value;*
NF is the feedback divider value;
NO is the output divider value

3.6 Electrical Characteristics for SAR-ADC

Table 10 RK3066 Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution	N		N/A	10	N/A	bits
Analog Supply Voltage	VDDIO		2.25	2.5	2.75	V
Digital Supply Voltage	VDDCore		1.0	1.1	1.2	V
Conversion speed	F_s	The duty cycle should be between 40%~60%	N/A	N/A	1	MSPS
Analog Supply Current	IAVDD		N/A	200	N/A	uA
Digital Supply Current	IDVDD		N/A	50	N/A	uA
Number of Channels	NCH AVDD		N/A	8	N/A	N/A
Differential Non Linearity	DNL		N/A	±1	N/A	LSB
Integral Non Linearity	INL		N/A	±2	N/A	LSB
Gain Error	E_{gain}		-8	N/A	8	LSB
Offset Error	E_{offset}		-8	N/A	8	mV
Power Down Current	ISHDN	From AVDD	N/A	0.5	N/A	uA
		From DVDD	N/A	0.5	N/A	uA
Power up time			N/A	7	N/A	$1/F_s$

3.7 Electrical Characteristics for TS-ADC

Table 11 RK3066 Electrical Characteristics for TS-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog Supply Voltage	AVDD		2.25	2.5	2.75	V
Digital Supply Voltage	DVDD		1.0	1.1	1.2	V
TSADC Accuracy			N/A	N/A	±5	C
Quiescent Current	IQ	From AVDD	N/A	180	N/A	uA
		From DVDD	N/A	40	N/A	uA
Power Down Current	ISHDN	From AVDD	N/A	1	N/A	uA
		From DVDD	N/A	5	N/A	uA
Number of Channels (Differential)		7 external, 1 internal	N/A	8	N/A	N/A
Clock Frequency	Fclk		N/A	N/A	50.0	KHz
Power up time			N/A	N/A	7	TCLK
Latency			N/A	N/A	1	TCLK

3.8 Electrical Characteristics for USB OTG/Host2.0 Interface

Table 12 RK3066 Electrical Characteristics for USB OTG/Host2.0 Interface

Parameters		Test condition	Min	Typ	Max	Units
HS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD	75℃ , OTG_VDD25 = HOST_VDD25 = 2.5V, OTG_VDD33 = HOST_VDD33 = 3.3V, OTG_DVDD = HOST_DVDD = 1.1V ,	N/A	5.35	N/A	mA
	Current From OTG_VDD33		N/A	2.50	N/A	mA
	Current From OTG_VDD25		N/A	21.2	N/A	mA

HS transmit, minimum transition density (all 1's data in DP/DM)	Current From OTG_DVDD	15-cm USB cable attached to DP/DM	N/A	4.07	N/A	mA
	Current From OTG_VDD33		N/A	2.25	N/A	mA
	Current From OTG_VDD25		N/A	17	N/A	mA
HS idle mode	Current From OTG_DVDD		N/A	5.4	N/A	mA
	Current From OTG_VDD33		N/A	2.22	N/A	mA
	Current From OTG_VDD25		N/A	6.23	N/A	mA
FS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD		N/A	3.25	N/A	mA
	Current From OTG_VDD33		N/A	16.5	N/A	mA
	Current From OTG_VDD25		N/A	6.47	N/A	mA
LS transmit, maximum transition density (all 0's data in DP/DM)	Current From OTG_DVDD		N/A	3.62	N/A	mA
	Current From OTG_VDD33		N/A	16.9	N/A	mA
	Current From OTG_VDD25		N/A	6.39	N/A	mA
Suspend mode	Current From OTG_DVDD		N/A	61.2	N/A	uA
	Current From OTG_VDD33		N/A	0.1	N/A	uA
	Current From OTG_VDD25		N/A	17.0	N/A	uA
Sleep mode	Current From OTG_DVDD		N/A	0.2	N/A	mA
	Current From OTG_VDD33		N/A	0.1	N/A	uA
	Current From OTG_VDD25		N/A	0.348	N/A	mA

3.9 Electrical Characteristics for HDMI

Table 13 RK3066 Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
2.5V Supply Voltage	VDDH	2.5±10%	2.25	2.5	2.75	V
1.1V Supply Voltage	VDDL	1.1±10%	0.99	1.0	1.21	V
REXT Resistance Error	DREXT	470ohms	-1	0	1	%
D2-0[9:0] Setup Time	TSU	To TMDS_CK	700	N/A	N/A	ps
D2-0[9:0] Hold Time	THLD	To TMDS_CK	700	N/A	N/A	ps
MSENS detect voltage for monitor connection	VCNCT	(VTXC+VTXC_N) / 2	2	N/A	N/A	V
MSENS detect voltage for monitor disconnection	VDISC	(VTXC+VTXC_N) / 2	N/A	N/A	0.4	V
MSENS response time	TMSENS		3	N/A	15	us
OSC minimum oscillation frequency when f(IDCK)=0Hz	FMINDDC	IDCK=L	20	30	40	MHz
Supply Current (2.5V)	IDDH		N/A	N/A	TBD	mA
Supply Current (1.1V)	IDDL		N/A	N/A	TBD	mA
Activation Time From Sleep	TACT		N/A	N/A	1	ms

3.10 Electrical Characteristics for DDR IO

Table 14 RK3066 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	VDDIO_DDR standby current, ODT OFF		@ 1.5V , 125℃	N/A	0.02	14.47	uA
	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	N/A	0.02	5.06	uA
DDR IO	Input leakage current		@ 1.2V , 125℃	N/A	0.01	4.51	uA

@LPDDR2 mode	VDD quiescent current		@ 1.1V , 125℃	N/A	0.02	4.21	uA
	VDDIO_DDR quiescent current		@ 1.2V , 125℃	N/A	0.02	12.31	uA

3.11 Electrical Characteristics for eFuse

Table 15 RK3066 Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Active mode	read current for COREP_EFUSE(1.1V)	I_{load_vdd}	STROBE high	2.537	4.049	5.695	mA
	read current for COREP_EFUSE(1.1V)	I_{active_vdd}	normal read 10MHz	1.498	2.368	3.308	mA
standby mode	standby current for COREP_EFUSE(1.1V)	$I_{standby\_vdd}$		0.057	0.255	0.492	uA