Rockchip RK61X Datasheet

Revision 1.2
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Revision History

Date	Revision	Description
2015-12-1	1.3	Update
2014-6-11	1.2	Update
2013-07-12	1.1	1.Update RGB output PIN name 2.Update codec content
2013-05-27	1.0	First revision

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Chapter 1 Introduction

1.1 Overview

RK61X is a partner chip for Rockchip mobile application processor. It can minimize the external components in Rockchip's Table and TV BOX solution; reduce the total cost and PCB size.

RK61X includes two RGB display input interface with double data rate. With the internal MUX function, it can output 1080P HDMI signal to TV and output RGB/LVDS/MIPI signal to TFT panel. In this case, RK61X can support dual panel (TV and TFT) display.

RK61X includes a audio codec, which with two I2S/PCM interface, two differential microphone input and audio processing function.

RK61X provides a complete set of display interface to support very flexible applications as follows:

- 2 RGB display input interface with double data rate
- 1 LVDS display output interface with double channels
- 1 MIPI display output interface with 4 data lanes
- 1 HDMI display output interface
- 1 RGB display input interface shared with LVDS
- 1 RGB display input interface shared with RGB display input interface
- Audio interface: one 4ch I2S/PCM interface, one 1ch I2S/PCM interface and one SPDIF rx interface
- I2Cconfigured interface

This document will provide guideline on how to use RK61X correctly and efficiently. The chapter 1 will introduce the features, block diagram, signal descriptions and system usage of RK61X, the chapter 2 to chapter 15 will describe the full function of each module in detail.

RK61X contains two versions:RK616 and RK618,the difference like follow：For RK616 ,it contains the chapters2,3,4,5,,8,9,10,12,13. For RK618,it contains the all chapters.

Table 1-1 The difference of RK616 and RK618

	RK616	RK618
PACKAGE	144-L	216-L
HDMI	support	support
SINGLE LVDS	support	support
DOUBLE LVDS	don't support	support
MIPI	don't support	support
ACODEC Normal	support	support
VIF/SCALER	support	support
ACODEC capless output	don't support	support

1.2 Features

1.2.1 Display interface

- Two 24BIT RGB input interface with dual data rate
- supports MIPI,LVDS and RGB interface to TFT LCD
- With scaler function, LVDS/MIPI/RGB and HDMI can output at the same time

1.2.2 HDMI

- Very low power operation, less than 60mW in PHY during 1080P HD display
- HDMI 1.4/1.3/1.2/1.1, HDCP 1.2 and DVI 1.0 standard compliant transmitter
- Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
- Support 3D function defined in HDMI 1.4 spec
- TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
- Supports all DTV resolutions including 480i/576i/480p/576p/720p/1080i/1080p
- Digital video interface supports a pixel size of 24bits color depth in RGB
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-192kHz Fs) using IEC60958 and IEC 61937
- Multiphase 4MHz fixed bandwidth PLL with low jitter
- DDC Bus I2C master interface at 3.3V
- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
- Support HDMI LipSync if needed as addon feature
- Lower power operation with optimal power management feature
- Embedded ESD, scan support logic.
- The EDID and CEC function are also supported by HDMI Transmitter Controller
- Optional Monitor Detection supported through Hot Plug

1.2.3 LVDS

- 35MHz~150MHz clock support
- 28:4 data channel compression at data rates up to 945 Mbps per channel
- Support VGA,SVGA,XGA and single pixel SXGA
- Comply with the Standard TIA/EIA-644-A LVDS stand
- Support 8bit format-1, format-2, format-3 display mode, Support 6bit display mode.
- Display mode can be select by input MUX
- Low power mode

1.2.4 MIPI D-PHY

- Mixed-signal D-PHY mixed-signal hard-macro- LS Transmitter and LS/HS Receiver solution
- Designed to MIPI® v1.0 Specifications
- Integrated PHY Protocol Interface (PPI) supports interface to CSI, DSI and UniPro™ MIPI® protocols
- 1.0GHz maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 4Gbps transfer rate
- HS, LP and ULPS modes supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- Low-Power dissipation: HS less than 3mA/Lane
- Tx/Rx Buffers with tunable On-Die-Termination and advanced equalization.
- Embedded ESD, boundary scan support logic.

1.2.5 MIPI Controller

- Support video and command modes
- PPI interface to the D-PHY
- Configurable from 1 to 4 data lanes output
- Supports up to 1Gb/s per data lane
- Bi-directional communication and escape mode support
- Programmable display resolutions, up to 2048x1080
- Multiple peripheral support capability with configurable virtual channels
- Video mode pixel formats: RGB565, RGB666 packed and loosely, RGB888
- Supports transmission of all generic commands

- ECC and checksum capabilities
- Supports ultra-low power mode
- Fault recovery schemes

1.2.6 Scaler

- Support max line pixel input upto 2560
- Support scaling down and scale up function
- Max output resolution 2048x1536

1.2.7 Audio Codec

- Two I2S/PCM interface
- Pure logic process, no need for Mixed signal process.
- Very low power, can be made <6.5mA in 3.3V for playback.
- 18 to 24 bit high order Sigma-Delta modulation for DAC with >93 dB SNR.
- 16 to 18 bit high order Sigma-Delta modulation for ADC with >90 dB SNR.
- Digital interpolation and decimation filter integrated.
- Line-in, microphone and speaker out interface.
- On-chip analog post filter and digital filters.
- Single–ended or differential microphone input.
- Automatic gain control for smooth audio recording.
- Sampling rate of 8k/12k/16k/24k/32k/48k/44.1k/96k Hz
- Support 16ohm to 32ohm headphone and speaker phone output.
- 3.3V analog +/-10% power supply for analog and 1.2/1.1/1.0V for digital core.
- Mono, Stereo supported.

1.2.8 Chip controll

Chapter 1 I2C slave interface
Chapter 2 External clock input for Chip working, this clock can share with MCLK (12M)
Chapter 3 Interrupt output for HDMI in and other function
Chapter 4 Two PLL , one for dual datarate input logic; the other for scaler

1.3 Block Diagram

The following diagram shows the basic block diagram for RK61X

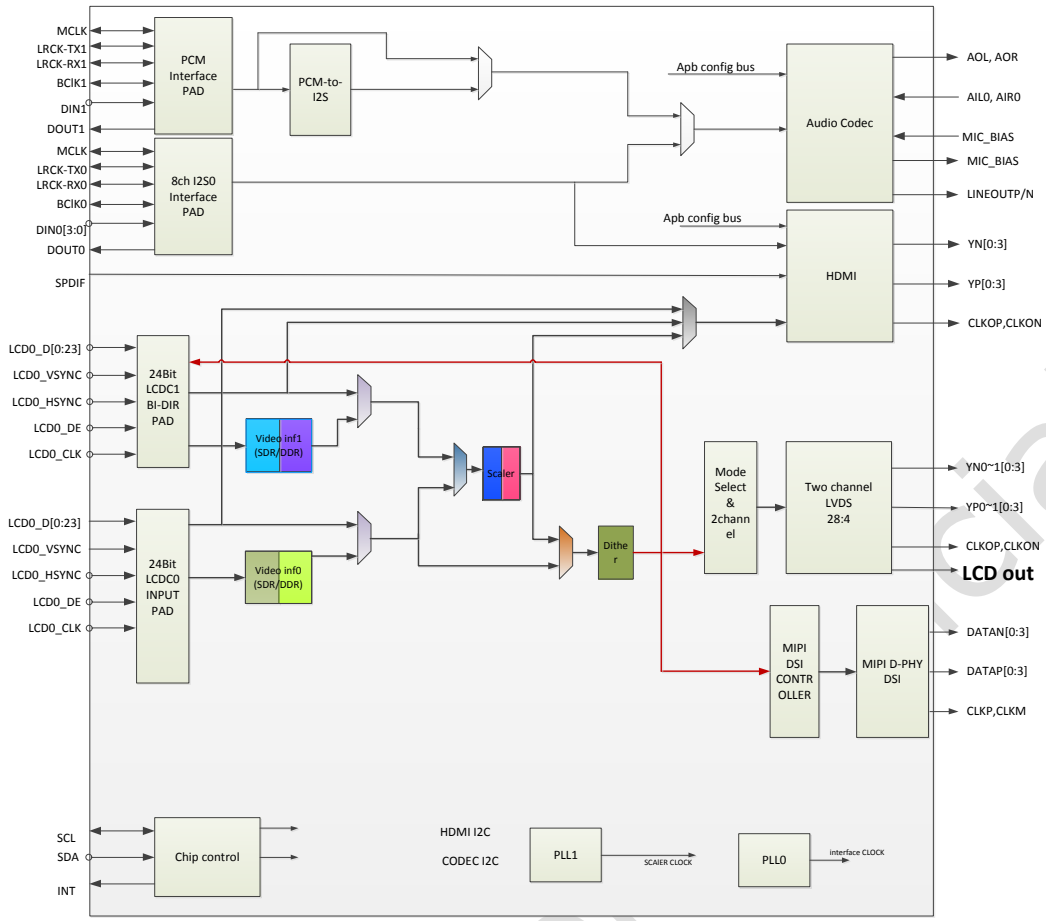

Fig. 1-1 RK61X Block Diagram

1.4 Pin Description

In this chapter, the pin description is all power/ground descriptions in Table 1-1, include analog power/ground.

1.4.1 RK61X power/ground IO descriptions

Table 1-2 RK616 Power/Ground IO information

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	C3,C5,B7,C6,D5,F6,F7,G7,J11, L10,E8,F9,C10,B12	0	0	0	Internal Core Ground and Digital IO Ground
VCC	G5,J6	3	3.3	3.6	Digital IO Power
VDD	F5,F8,H7,D10	1.08	1.2	1.32	Internal Core Power

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
LVDS_VCC	A11,A12,B11, E10,F10	2.25	2.5	2.75	LVDS Analog power
PLL1VDD_1V2	J10	1.08	1.2	1.32	PLL1 1.2 power
PLL2VDD_1V2	K10	1.08	1.2	1.32	PLL2 1.2 power
PLL1VDD_3V3	K10	3	3.3	3.6	PLL1 3.3 power
PLLVSS	K11	0	0	0	PLL analog ground
AVCC	C4,C7 A7,B8,B9	3	3.3	3.6	HDMI 3.3 analog power CODEC Analog power
HDMIVDD	D6	1.08	1.2	1.32	HDMI 1.2 analog power
CODEC_AVSS	C8,D7	0	0	0	CODEC Analog ground

Table 1-3 RK618 Power/Ground IO information

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	C3,C8,C11,C14,F6,F7,F9 F11,G7,G8,G9,G10,H7,H8,H9 H10,J2,J6,J7,J8,J9,J10,K6,K7 K8,K9,K10,K11,L6,L9,L10,L11 P9,P12,R3	N/A	N/A	N/A	Internal Core Ground and Digital IO Ground
VCC	F8,G6,L7	N/A	3.3	N/A	Digital IO Power
VDD	H6,F10,L8	N/A	1.2	N/A	Internal Core Power
LVDS_VCC	P6,P8,P11	N/A	2.5	N/A	LVDS Analog power
PLL1VDD_1V2	L4	N/A	1.2	N/A	PLL1 1.2 power
PLL2VDD_1V2	L4	N/A	1.2	N/A	PLL2 1.2 power
PLLVDD_3V3	L1,M4	N/A	3.3	N/A	PLL1 3.3 power MIPI PLL analog power
PLLVSS	K2	N/A	N/A	N/A	PLL analog ground
AVCC	R16,H16,K16,D16,E16	N/A	3.3	N/A	HDMI/CODEC/MIPI 3.3V Analog power

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
HDMIVDD	K15	N/A	1.2	N/A	HDMI 1.2 analog power
AVSS	D15,E15,F16,H15,J13	N/A	N/A	N/A	Analog ground
HDMI_AVSS	L14,M14,P14,R15	N/A	N/A	N/A	HDMI Analog ground
MIPIAVDD_1V2	L3	N/A	1.2	N/A	MIPI analog power
MIPI_AVSS	L2,M3,P3,T3	N/A	N/A	N/A	MIPI analog ground

1.4.2 RK61X function IO descriptions

Table 1-4 RK61X IO descriptions

Port name	BALL# (144-L) RK616	BALL# (216-L) RK618	Pad dir	Reset value	Pull up/down	Power Supply	Pin Description
IO_LCDC1_DATA[8]	H8	E1	I/O	input	pull down	LCDC	LCD interface 1 data 8
IO_LCDC1_DATA[7]	G8	F5	I/O	input	pull down	LCDC	LCD interface 1 data 7
IO_LCDC1_DATA[6]	M9	F4	I/O	input	pull down	LCDC	LCD interface 1 data 6
IO_LCDC1_DATA[5]	L9	F3	I/O	input	pull down	LCDC	LCD interface 1 data 5
IO_LCDC1_DATA[4]	K9	F2	I/O	input	pull down	LCDC	LCD interface 1 data 4
IO_LCDC1_DATA[3]	J9	F1	I/O	input	pull down	LCDC	LCD interface 1 data 3
IO_LCDC1_DATA[2]	H9	G1	I/O	input	pull down	LCDC	LCD interface 1 data 2
IO_LCDC1_DATA[1]	G9	G2	I/O	input	pull down	LCDC	LCD interface 1 data 1
IO_LCDC1_DATA[0]	M10	H5	I/O	input	pull down	LCDC	LCD interface 1 data 0
IO_LCDC1_DEN	M11	H4	I/O	input	pull down	LCDC	lcdc1 data enable signal
IO_LCDC1_DCLKP	L11	H1	I/O	input	pull down	LCDC	lcdc1 clock out
IO_LCDC1_DCLKN	---	H2	I/O	input	pull down	LCDC	lcdc1 clock out(Negative)
IO_LCDC1_HSYNCN	M12	J1	I/O	input	pull down	LCDC	lcdc0 horizontal sync signal
IO_LCDC1_VSYNCN	L12	K1	I/O	input	pull down	LCDC	lcdc0 vertical sync signal
IO_I2S1SDO	H12	H3	O		pull down	LCDC	I2S1 SDO
IO_I2S1BCLK	J12	J5	I/O		pull down	LCDC	I2S1 SCLK
IO_I2S1SLRCKRX	K12	J4	I/O		pull down	LCDC	I2S1 LRCK for ADC
IO_I2S1SLRCKTX	H11	J3	I/O		pull down	LCDC	I2S1 LRCK for DAC
IO_I2S1SDI	G10	L5	I		pull down	LCDC	I2S1 SDI

Port name	BALL# (144-L) RK616	BALL# (216-L) RK618	Pad dir	Reset value	Pull up/down	Power Supply	Pin Description
IO_MIPIPHY_DATAN0	---	M1	A			MIPIPHY	MIPI data lane0 serial data output(Negative)
IO_MIPIPHY_DATAP0	---	M2	A			MIPIPHY	MIPI data lane0 serial data output
IO_MIPIPHY_DATAN1	---	N1	A			MIPIPHY	MIPI data lane1 serial data output(Negative)
IO_MIPIPHY_DATAP1	---	N2	A			MIPIPHY	MIPI data lane1 serial data output
IO_MIPIPHY_CLKN	---	P1	A			MIPIPHY	MIPI clock lane serial data output(Negative)
IO_MIPIPHY_CLKP	---	P2	A			MIPIPHY	MIPI clock lane serial data output
IO_MIPIPHY_DATAP2	---	R2	A			MIPIPHY	MIPI data lane2 serial data output
IO_MIPIPHY_DATAN2	---	R1	A			MIPIPHY	MIPI data lane2 serial data output(Negative)
IO_MIPIPHY_DATAP3	---	T2	A			MIPIPHY	MIPI data lane3 serial data output
IO_MIPIPHY_DATAN3	---	T1	A			MIPIPHY	MIPI data lane3 serial data output(Negative)
IO_LCDC_DEN	---	R4	O	0	pull down	RGB	lcdc data enable signal(LVDS used as RGB Output)
IO_LCDC_DCLK	---	T4	O	0	pull down	RGB	lcdc clock out
IO_LCDC_HSYNCN	---	N5	O	0	pull down	RGB	lcdc horizontal sync signal
IO_LCDC_VSYNCN	---	M6	O	0	pull down	RGB	lcdc0 vertical sync signal
IO_LCDC_DATA23	---	P5	O	0	pull down	RGB	LCD interface data 23
IO_LCDC_DATA22	---	N6	O	0	pull down	RGB	LCD interface data 22
IO_LCDC_DATA21	---	N8	O	0	pull down	RGB	LCD interface data 21
IO_LCDC_DATA20	---	M8	O	0	pull down	RGB	LCD interface data 20
IO_LVDS_PADN_8/LCDC_DATA17	---	T5	A			LVDS/ RGB	Transmit serial data out (Negative), n=1~8/LCD interface data 17
IO_LVDS_PADP_8/LCDC_DATA16	---	R5	A			LVDS/ RGB	Transmit serial data out, n=1~8/LCD interface data 16
IO_LVDS_CLKN2/LCDC_DATA19	---	T6	A			LVDS/ RGB	Output clock (Negative)/LCD interface data 19
IO_LVDS_CLKP2/LCDC_DATA18	---	R6	A			LVDS/ RGB	Output clock/LCD interface data 18
IO_LVDS_PADN_7/LCDC_DATA15	---	T7	A			LVDS/ RGB	Transmit serial data out (Negative), n=1~8 /LCD interface data 15
IO_LVDS_PADP_7/LCDC_DATA14	---	R7	A			LVDS/ RGB	Transmit serial data out, n=1~8/ LCD interface data 14
IO_LVDS_PADN_6/LCDC_DATA13	---	T8	A			LVDS/ RGB	Transmit serial data out (Negative), n=1~8/LCD interface data 13
IO_LVDS_PADP_6/LCDC_DATA12	---	R8	A			LVDS/ RGB	Transmit serial data out, n=1~8/LCD interface data 12
IO_LVDS_PADN_5/LCDC_DATA11	---	T9	A			LVDS/ RGB	Transmit serial data out (Negative), n=1~8/LCD interface data 11
IO_LVDS_PADP_5/LCDC_DATA10	---	R9	A			LVDS/ RGB	Transmit serial data out, n=1~8/LCD interface data 10
IO_LVDS_XRES	E9	T15	A			LVDS	LVDS current biasing generation,Connect 12Kohm resistor to ground
IO_LVDS_PADN_4/LCDC_DATA7	C11	T10	A			LVDS/ RGB	Transmit serial data out, n=1~8/LCD interface data 7
IO_LVDS_PADP_4/LCDC_DATA6	C12	R10	A			LVDS/ RGB	Transmit serial data out (Negative), n=1~8/LCD interface data 6
IO_LVDS_CLKN1/LCDC	E11	T11	A			LVDS/	Output clock (Negative)/LCD

Port name	BALL# (144-L) RK616	BALL# (216-L) RK618	Pad dir	Reset value	Pull up/down	Power Supply	Pin Description
_DATA9						RGB	interface data 9
IO_LVDS_CLKP1/LCDC _DATA8	E12	R11	A			LVDS/ RGB	Output clock/LCD interface data 8
IO_LVDS_PADN_3/LCD C_DATA5	D11	T12	A			LVDS/ RGB	Transmit serial data out (Negative), n=1~8/LCD interface data 5
IO_LVDS_PADP_3/LCD C_DATA4	D12	R12	A			LVDS/ RGB	Transmit serial data out, n=1~8/LCD interface data 4
IO_LVDS_PADN_2/LCD C_DATA3	F11	T13	A			LVDS/ RGB	Transmit serial data out (Negative), n=1~8/LCD interface data 3
IO_LVDS_PADP_2/LCD C_DATA2	F12	R13	A			LVDS/ RGB	Transmit serial data out, n=1~8/LCD interface data 2
IO_LVDS_PADN_1/LCD C_DATA1	G11	T14	A			LVDS/ RGB	Transmit serial data out (Negative), n=1~8/LCD interface data 1
IO_LVDS_PADP_1/LCD C_DATA0	G12	R14	A			LVDS/ RGB	Transmit serial data out, n=1~8/LCD interface data 0
IO_HDMI_EXTR	A2	T16	A			HDMI	Connect 1.9Kohm resistor to ground to generate reference current.
IO_HDMI_TX3N	A6	P15	A			HDMI	TMDS negative clock line
IO_HDMI_TX3P	B6	P16	A			HDMI	TMDS positive clock line.
IO_HDMI_TX0N	A5	N15	A			HDMI	TMDS channel 0 negative data line.
IO_HDMI_TX0P	B5	N16	A			HDMI	TMDS channel 0 positive data line.
IO_HDMI_TX1N	A4	M15	A			HDMI	TMDS channel 1 negative data line.
IO_HDMI_TX1P	B4	M16	A			HDMI	TMDS channel 1 positive data line.
IO_HDMI_TX2N	A3	L15	A			HDMI	TMDS channel 2 negative data line.
IO_HDMI_TX2P	B3	L16	A			HDMI	TMDS channel 2 positive data line.
IO_ACODEC_IN3L	B10	L13	A			ACODEC	Left line input
IO_ACODEC_IN3R	A10	M13	A			ACODEC	Right line input
IO_ACODEC_MIC1N	C9	J11	A			ACODEC	Negative input for left microphone
IO_ACODEC_MIC1P	---	J12	A			ACODEC	Positive input for left microphone
IO_ACODEC_MICBIAS1	D9	M11	A			ACODEC	Microphone bias ouput1
IO_ACODEC_MICBIAS2	---	L12	A			ACODEC	Microphone bias ouput2
IO_ACODEC_MIC2P	---	H13	A			ACODEC	Positive input for right microphone
IO_ACODEC_MIC2N	---	H12	A			ACODEC	Negative input for right microphone
IO_ACODEC_IN1N	---	F12	A			ACODEC	Negative line input
IO_ACODEC_IN1P	---	F13	A			ACODEC	Positive line input
IO_ACODEC_VCM	D8	J16	A			ACODEC	Common mode reference voltage decoupling pin
IO_ACODEC_LINE1	---	F14	A			ACODEC	Line output 1
IO_ACODEC_LINE2	---	H14	A			ACODEC	Line output 2
IO_ACODEC_SPKL	A8	J14	A			ACODEC	Left speaker output
IO_ACODEC_SPKR	A9	J15	A			ACODEC	Right speaker output
AOM1	---	F15	A			ACODEC	Common mode analog output
NC	---	G15	A			ACODEC	Don`t connected,lleft floating
AOM2	---	G16	A			ACODEC	Common mode analog output
IO_HDMI_CEC	E7	E13	I/0		pull up	LCDC	HDMI CEC control line.
IO_HDMI_HDP	E6	C16	I/0		pull up	LCDC	HDMI HPD Hot plug detect

Port name	BALL# (144-L) RK616	BALL# (216-L) RK618	Pad dir	Reset value	Pull up/down	Power Supply	Pin Description
IO_HDMI_I2CSDA	D4	N12	I/0		pull up	LCDC	DDC channel SDA in. For tri - state gate use
IO_HDMI_I2CSCL	E5	N11	I/0		pull up	LCDC	DDC channel SCL in. For tri - state gate use
IO_I2C_SDA	E2	M9	I/0		pull up	LCDC	I2C SDA
IO_I2C_SCL	D1	N9	I		pull up	LCDC	I2C SCL
IO_CLKIN	D2	C15	I		pull down	LCDC	RK61X clock input
IO_I2S0SDO	B2	E14	O		pull down	LCDC	I2S0 sdo
IO_I2S0BCLK	A1	B16	I/O		pull down	LCDC	I2S0 SCLK
IO_I2S0SLRCKRX	B1	B15	I/O		pull down	LCDC	I2S0 LRCK for ADC
IO_I2S0SLRCKTX	C2	A16	I/O		pull down	LCDC	I2S0 LRCK for DAC
IO_I2S0SDI[0]	C1	D12	I		pull down	LCDC	I2S0 sdi[0]
IO_I2S0SDI[1]	D3	E11	I		pull down	LCDC	I2S0 sdi[1]
IO_I2S0SDI[2]	E4	B14	I		pull down	LCDC	I2S0 sdi[2]
IO_I2S0SDI[3]	E3	A15	I		pull down	LCDC	I2S0 sdi[3]
IO_SPDIF	F4	H11	I		pull down	LCDC	SPDIF input
IO_TEST	F3	G11	I		pull down	LCDC	test input
IO_NPOR	F2	A14	I		pull up	LCDC	power on reset
IO_INT	E1	D11	I		pull down	LCDC	RK61X interrupt output
IO_LCDC0_VSYNCN	K5	B13	I		pull down	LCDC	lcdc0 vertical sync signal
IO_LCDC0_HSYNCN	L5	C12	I		pull down	LCDC	lcdc0 horizontal sync signal
IO_LCDC0_DEN	L4	A13	I		pull down	LCDC	lcdc0 data enable signal
IO_LCDC0_DCLKP	M5	A12	I		pull down	LCDC	lcdc0 clock out
IO_LCDC0_DCLKN	---	B12	I		pull down	LCDC	lcdc0 clock out(Negative)
IO_LCDC0_DATA[23]	F1	C9	I		pull down	LCDC	LCD interface 0 data 23
IO_LCDC0_DATA[22]	G1	B11	I		pull down	LCDC	LCD interface 0 data 22
IO_LCDC0_DATA[21]	G2	E9	I		pull down	LCDC	LCD interface 0 data 21
IO_LCDC0_DATA[20]	G3	A11	I		pull down	LCDC	LCD interface 0 data 20
IO_LCDC0_DATA[19]	G4	D9	I		pull down	LCDC	LCD interface 0 data 19
IO_LCDC0_DATA[18]	H1	B10	I		pull down	LCDC	LCD interface 0 data 18
IO_LCDC0_DATA[17]	H2	A10	I		pull down	LCDC	LCD interface 0 data 17
IO_LCDC0_DATA[16]	H3	B9	I		pull down	LCDC	LCD interface 0 data 16
IO_LCDC0_DATA[15]	H4	A9	I		pull down	LCDC	LCD interface 0 data 15
IO_LCDC0_DATA[14]	J1	A8	I		pull down	LCDC	LCD interface 0 data 14
IO_LCDC0_DATA[13]	J2	E8	I		pull down	LCDC	LCD interface 0 data 13
IO_LCDC0_DATA[12]	J3	B8	I		pull down	LCDC	LCD interface 0 data 12
IO_LCDC0_DATA[11]	J4	D8	I		pull down	LCDC	LCD interface 0 data 11
IO_LCDC0_DATA[10]	K1	A7	I		pull down	LCDC	LCD interface 0 data 10
IO_LCDC0_DATA[9]	K2	A6	I		pull down	LCDC	LCD interface 0 data 9
IO_LCDC0_DATA[8]	K3	B7	I		pull down	LCDC	LCD interface 0 data 8
IO_LCDC0_DATA[7]	K4	A5	I		pull down	LCDC	LCD interface 0 data 7
IO_LCDC0_DATA[6]	L1	B6	I		pull down	LCDC	LCD interface 0 data 6
IO_LCDC0_DATA[5]	L2	C6	I		pull down	LCDC	LCD interface 0 data 5
IO_LCDC0_DATA[4]	M1	A4	I		pull down	LCDC	LCD interface 0 data 4
IO_LCDC0_DATA[3]	M2	E6	I		pull down	LCDC	LCD interface 0 data 3
IO_LCDC0_DATA[2]	L3	B5	I		pull down	LCDC	LCD interface 0 data 2
IO_LCDC0_DATA[1]	M3	D6	I		pull down	LCDC	LCD interface 0 data 1
IO_LCDC0_DATA[0]	M4	D5	I		pull down	LCDC	LCD interface 0 data 0
IO_LCDC1_DATA[23]	J5	A3	I/O	input	pull down	LCDC	LCD interface 1 data 23
IO_LCDC1_DATA[22]	H5	A2	I/O	input	pull down	LCDC	LCD interface 1 data 22
IO_LCDC1_DATA[21]	M6	B4	I/O	input	pull down	LCDC	LCD interface 1 data 21
IO_LCDC1_DATA[20]	L6	A1	I/O	input	pull down	LCDC	LCD interface 1 data 20
IO_LCDC1_DATA[19]	K6	C5	I/O	input	pull down	LCDC	LCD interface 1 data 19
IO_LCDC1_DATA[18]	H6	B3	I/O	input	pull down	LCDC	LCD interface 1 data 18

Port name	BALL# (144-L) RK616	BALL# (216-L) RK618	Pad dir	Reset value	Pull up/down	Power Supply	Pin Description
IO_LCDC1_DATA[17]	G6	B2	I/O	input	pull down	LCDC	LCD interface 1 data 17
IO_LCDC1_DATA[16]	M7	B1	I/O	input	pull down	LCDC	LCD interface 1 data 16
IO_LCDC1_DATA[15]	L7	C1	I/O	input	pull down	LCDC	LCD interface 1 data 15
IO_LCDC1_DATA[14]	K7	C2	I/O	input	pull down	LCDC	LCD interface 1 data 14
IO_LCDC1_DATA[13]	J7	D1	I/O	input	pull down	LCDC	LCD interface 1 data 13
IO_LCDC1_DATA[12]	M8	E4	I/O	input	pull down	LCDC	LCD interface 1 data 12
IO_LCDC1_DATA[11]	L8	D2	I/O	input	pull down	LCDC	LCD interface 1 data 11
IO_LCDC1_DATA[10]	K8	E3	I/O	input	pull down	LCDC	LCD interface 1 data 10
IO_LCDC1_DATA[9]	J8	E2	I/O	input	pull down	LCDC	LCD interface 1 data 9

Notes :

①: Pad types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: Output Drive strength is configurable, it's the suggested value in this table. Unit is mA , only Digital IO have drive value

③:Reset state: I = input without any pull resistor O = output

④:It is die location. For examples, "Left side" means that all the related IOs are always in left side of die

⑤:Power supply means that all the related IOs are in this IO power domain. If multiple powers are included, they are connected together in one IO power ring

⑥ The pull up/pull down is configurable.

1.5 Package information

1.5.1 RK616 Dimension

RK616 package is TFBGA (HF) 10x10 0.8P 144L_2L Substrate
(body: 10mm x 10mm ; ball size : 0.4mm ; ball pitch : 0.8mm)

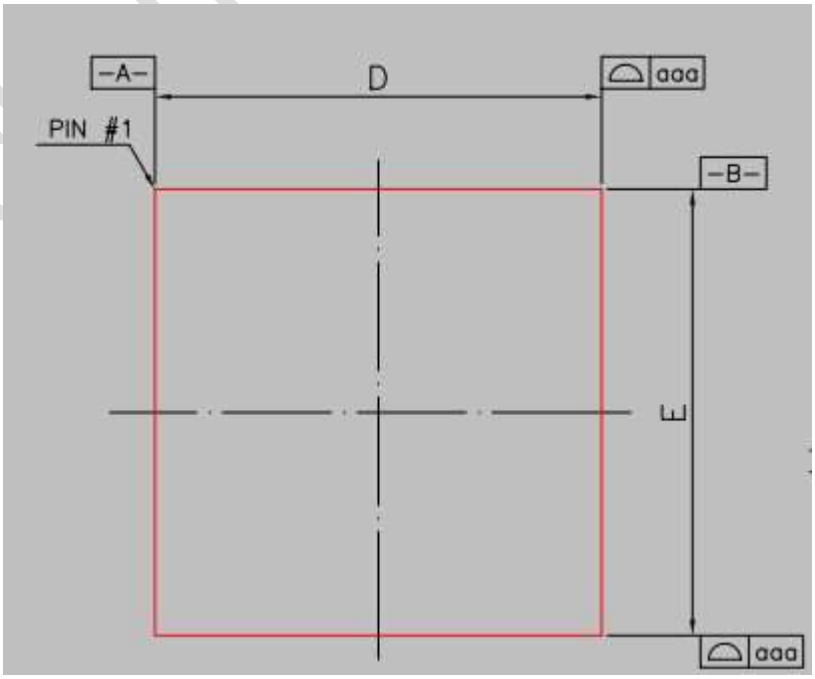

Fig. 1-2 RK616 TFBGA(HF) Package Top View

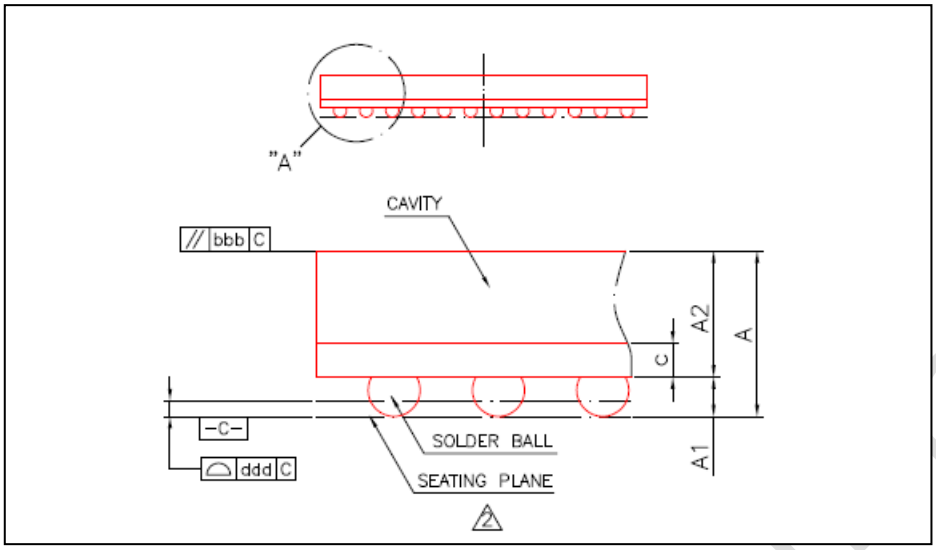

Fig. 1-3 RK616 TFBGA(HF) Package Side View

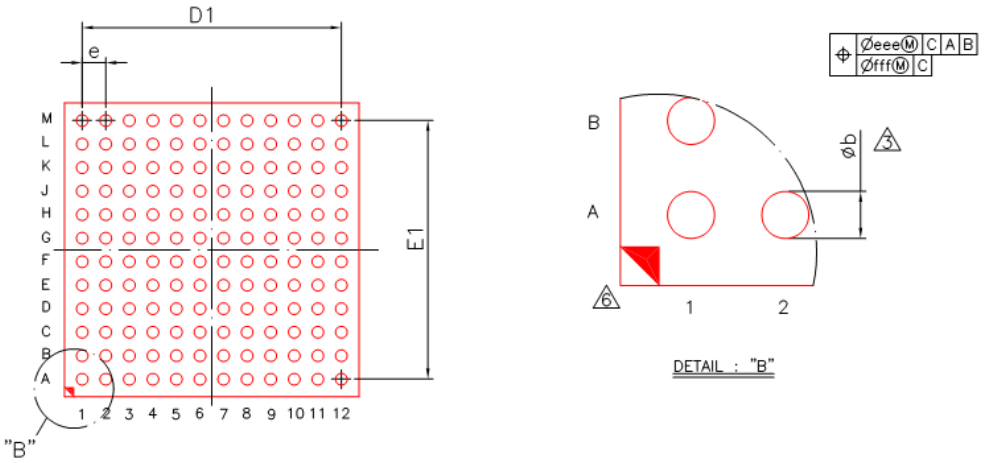

Fig. 1-4 RK616 TFBGA(HF) Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	---	8.80	---	---	0.346	---
E1	---	8.80	---	---	0.346	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.12			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	12/12			12/12		

Fig. 1-5 RK616 TFBGA(HF) Package Dimension

1.5.2 RK618 Dimension

RK618 package is TFBGA (HF) 11x11 0.65P 216L_2L Substrate
(body: 11mm x 11mm ; ball size : 0.3mm ; ball pitch : 0.65mm)

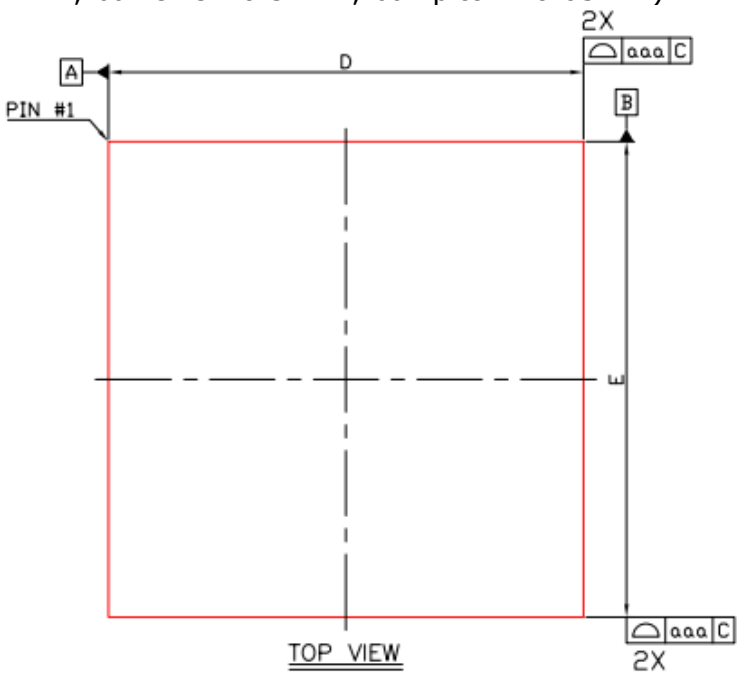

Fig. 1-6 RK618 TFBGA(HF) Package Top View

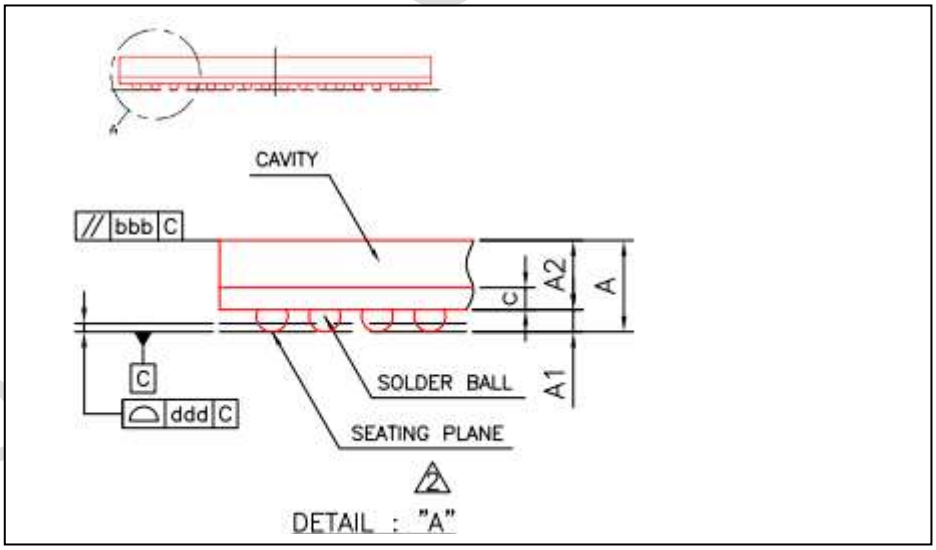

Fig. 1-7 RK618 TFBGA(HF) Package Side View

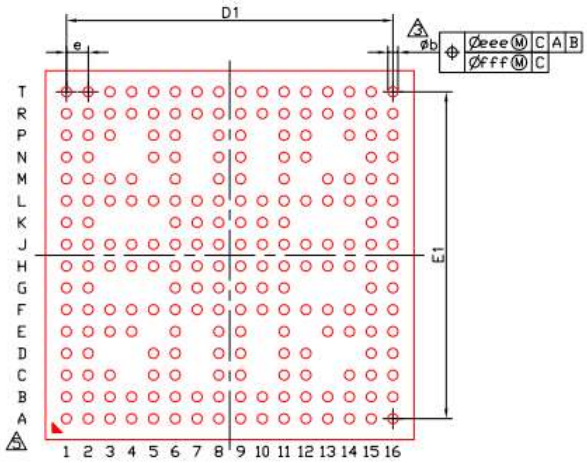

Fig. 1-8 RK618 TFBGA(HF) Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	10.90	11.00	11.10	0.429	0.433	0.437
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	----	9.75	----	----	0.384	----
E1	----	9.75	----	----	0.384	----
e	----	0.65	----	----	0.026	----
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	16 /16			16 /16		

Fig. 1-9 RK618 TFBGA(HF) Package Dimension

1.5.3 RK616 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	
A	I2S0_SCLK	HDMI_EXTR	HDMI_TX2N	HDMI_TX1N	HDMI_TX0N	HDMI_TXCN	CODEC_AVCC	AOL	AOR	IN3R	LVDS_VCC	LVDS_VCC	A
B	I2S0_LRCK_RX	I2S0_SDO	HDMI_TX2P	HDMI_TX1P	HDMI_TX0P	HDMI_TXCP	VSS	CODEC_AVCC	CODEC_AVCC	IN3L	LVDS_VCC	VSS	B
C	I2S0_SDI_D0	I2S0_LRCK_TX	VSS	HDMIVCC_3V3	VSS	VSS	HDMIVCC_3V3	CODEC_AVSS	MIC1N	VSS	LCD_D9/LVDS0_D3N	LCD_D8/LVDS0_D3P	C
D	I2C_SCL	I2S0_CLK	I2S0_SDI_D1	HDMI_SDA	VSS	HDMIVDD_1V2	CODEC_AVSS	VCM	MICBIAS1	VDD	LCD_D5/LVDS0_D2N	LCD_D4/LVDS0_D2P	D
E	INT	I2C_SDA	I2S0_SDI_D3	I2S0_SDI_D2	HDMI_SCL	HDMI_HPD	HDMI_CEC	VSS	LVDS_EXTR	LVDS_VCC	LCD_D7/LVDS0_CLKN	LCD_D6/LVDS0_CLKP	E
F	LCD0_D23	NPOR	TEST	SPDIF	VDD	VSS	VSS	VDD	VSS	LVDS_VCC	LCD_D3/LVDS0_D1N	LCD_D2/LVDS0_D1P	F
G	LCD0_D22	LCD0_D21	LCD0_D20	LCD0_D19	VCC	LCD1_D17	VSS	LCD1_D7	LCD1_D1	I2S1_SDI	LCD_D1/LVDS0_D0N	LCD_D0/LVDS0_D0P	G
H	LCD0_D18	LCD0_D17	LCD0_D16	LCD0_D15	LCD1_D22	LCD1_D18	VDD	LCD1_D6	LCD1_D2	PLL1VDD_3V3	I2S1_LRCK_TX	I2S1_SDO	H
J	LCD0_D14	LCD0_D13	LCD0_D12	LCD0_D11	LCD1_D23	VCC	LCD1_D13	LCD1_D9	LCD1_D3	PLL1VDD_1V2	VSS	I2S1_SCLK	J
K	LCD0_D10	LCD0_D9	LCD0_D8	LCD0_D7	LCD0_VSYNC	LCD1_D19	LCD1_D14	LCD1_D10	LCD1_D4	PLL2VDD_1V2	PLLVSS	I2S1_LRCK_RX	K
L	LCD0_D6	LCD0_D5	LCD0_D2	LCD0_DEN	LCD0_HSYNC	LCD1_D20	LCD1_D15	LCD1_D11	LCD1_D5	VSS	LCD1_DCLK	LCD1_VSYNC	L
M	LCD0_D4	LCD0_D3	LCD0_D1	LCD0_D0	LCD0_DCLK	LCD1_D21	LCD1_D16	LCD1_D12	LCD1_D8	LCD1_D0	LCD1_DEN	LCD1_HSYNC	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Fig. 1-10 RK616 Ball Mapping Diagram

1.5.4 RK618 Ball Map

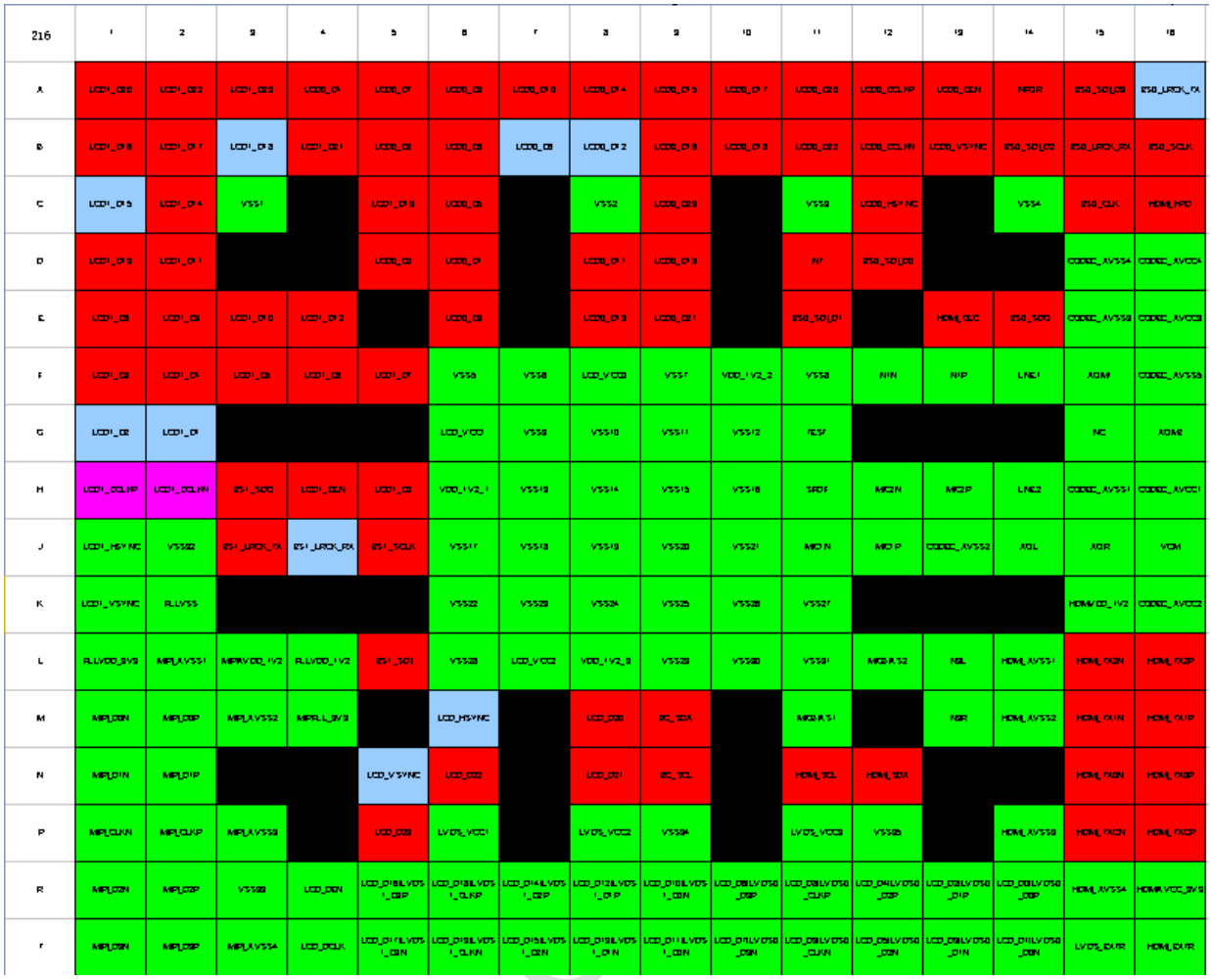

Fig. 1-11 RK618 Ball Mapping Diagram

1.6 Electrical Specification

1.6.1 Electrical Characteristics for General IO

Table 1-5 RK61X Electrical DC Characteristics for Digital General IO

Parameters		Symbol	Min	Typ	Max
Digital GPIO @3.3V	Pre-driver supply voltage	VDD	1.08V	1.2V	1.32V
	I/O supply voltage	VCC	2.97V	3.3V	3.63V
	Input High Voltage	VIH	2.0V	N/A	VCC+
	Input Low Voltage	VIL	-0.3V	N/A	0.8V
	Threshold point	VT	1.21V	1.42V	1.64V
	Schmitt trig Low to High threshold point	VT+	1.36V	1.60V	1.86V
	Schmitt trig. High to Low threshold point	VT-	0.93V	1.09V	1.30V
	Junction Temperature	TJ	0℃	25℃	125℃
	Input Leakage Current	IL			±1uA
	Tri-State output leakage current	IOZ			±1uA

Parameters		Symbol	Min	Typ	Max
	Pull-up Resistor	RPU	33K	41K	62K
	Pull-down Resistor	RPD	33K	42K	68K
	Output low voltage @IOL=2,4…24mA	VOL			0.4V
	Output high voltage @ IOH=2,4…24mA	VOH	2.4V		
	Low level output current @VOL=0.4V	IOL	8.0mA	12.4mA	15.6mA
	High level output current @VOH=2.4V	IOH	9.2mA	19.6mA	30.8mA

Table 1-6 RK61X Electrical AC Characteristics for Digital General IO

Type		Condition
Digital GPIO @3.3V	Typical case	VCC=3.3V, VDD=1.2V temperature=25℃ Process = Typical-Typical
	Best case	VCC=3.63V, VDD=1.32V temperature=0℃ Process = Fast-Fast
	Worst case	VCC=2.97V, VDD=1.08V temperature=125℃ Process =Slow-Slow
	Worst case (low temperature)	VCC=2.97V, VDD=1.08V temperature=-40℃ Process =Slow-Slow
	Best case (Low temperature)	VCC=3.63V, VDD=1.32V temperature=-40℃ Process = Fast-Fast

1.7 Hardware Guideline

1.7.1 HDMI PCB Layout Guide

This section describes the strategy of PCB layout for customer integration with HDMI Transmitter on their PCB system. It mainly introduces how to connect the TMDS channel, DDC channel, CEC channel and HPD signal of Innoslicon HDMI Transmitter to the HDMI port type A.

Designers should include decoupling and bypass capacitors at each power pin in the layout. Place these components as closely as possible to the power pins.

The differential lines should be routed as directly as possible from chip to connector. Each differential pair should be routed together, minimizing the number of vias through which the signal lines are routed. The distance separating the two traces of the differential pair should be kept to a minimum. Layout all the differential pairs (+/-)with controlled impedance of 100 ohm differential. It is important that the differential lines be referenced to a solid plane.
1,TMDS CHANNEL

As the PCB scheme shown below
Connect TX3N to CK- on the HDMI PORT.
Connect TX3P to CK+ on the HDMI PORT.
Connect TX0N to TM0- on the HDMI PORT.
Connect TX0P to TM0+ on the HDMI PORT.
Connect TX1N to TM1- on the HDMI PORT.

Connect TX1P to TM1+ on the HDMI PORT.
Connect TX2N to TM2- on the HDMI PORT.
Connect TX2P to TM2+ on the HDMI PORT.

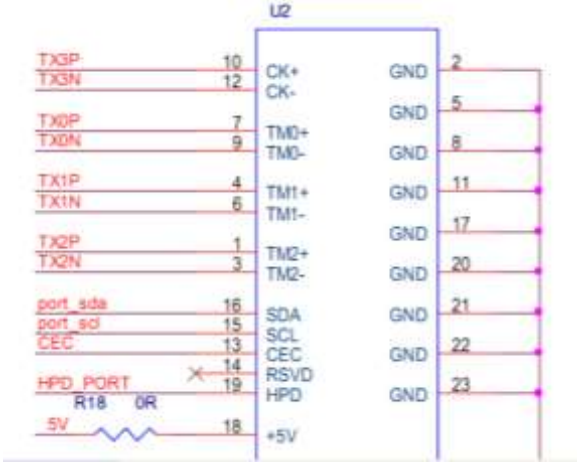

Fig. 1-12 PCB Scheme for TMDS Channel

2, DDC CHANNEL

The DDC channel used the industrial standard I2C bus. As shown the PCB Scheme below, the DDC_sda and DDC_scl on HDMI TX side need series a 33R resistor to the HDMI port. The port_sda and port_scl on the HDMI port side must be pulled up through a 2K resistor to 5V DC power.

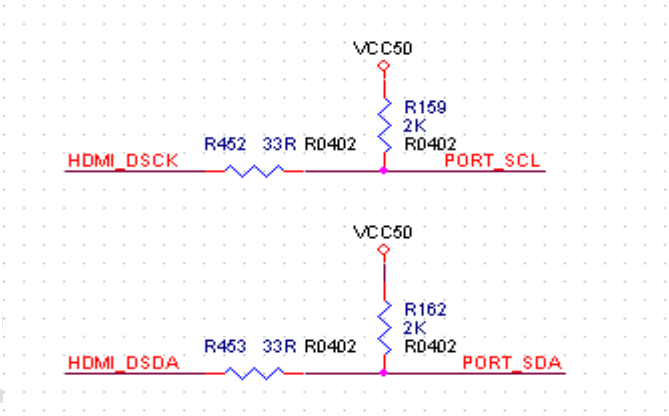

Fig. 1-13 PCB Scheme for DDC Channel

3,CEC CHANNEL
The signal CEC_sda on the HDMI Transmitter must be pulled up through a 10K resistor to 3.3V DC power, then directly connect to CEC pad on the HDMI port.

4,HPD
As shown the PCB scheme below, it gives the reference circuit for customer connecting HPD signal of the HDMI Transmitter to the HPD_PORT pad on the HDMI port.

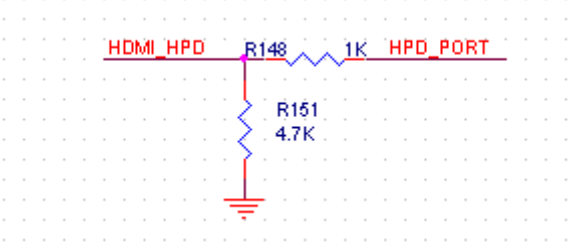

Fig. 1-14 PCB Scheme for hpd

5,ESD

If ESD suppression devices or common mode chokes are used, place them near the HDMI connector.

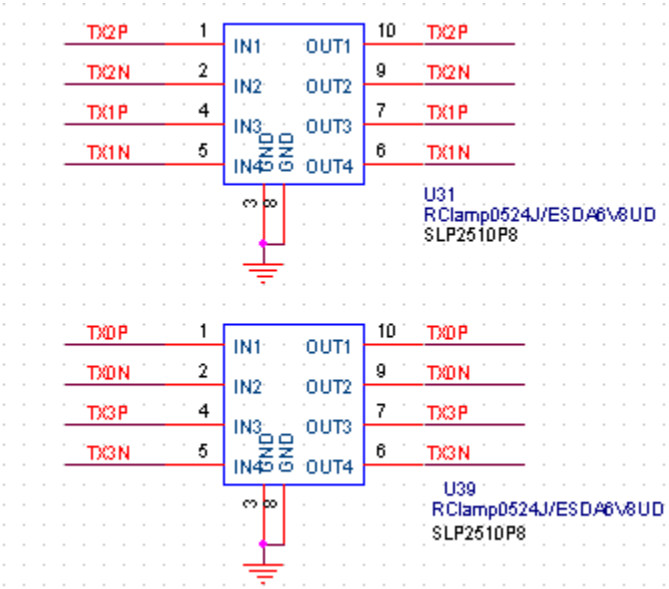

Fig. 1-15 PCB Scheme for ESD

1.7.2 CODEC PCB Layout Guide

This chapter describes the strategy of PCB layout for customer integration with Codec in their PCB system. It mainly introduces how to connect the Codec signals.

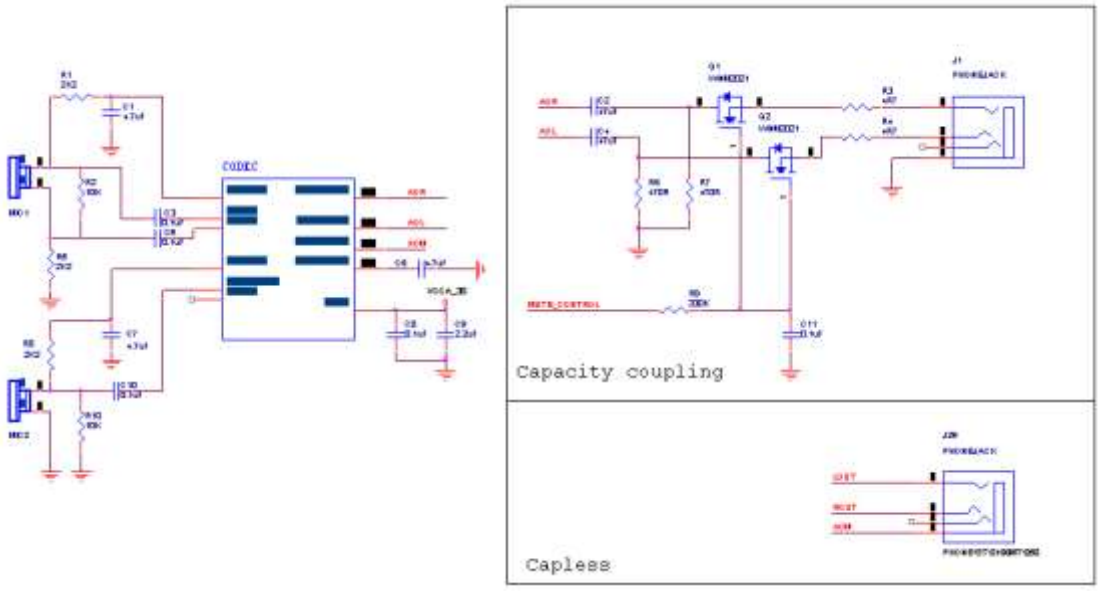

Fig. 1-16 PCB Scheme for CODEC

Look at above diagram the MIC1N and MIC1P are each connected with a MIC through a 0.1uf CAP.

The C3 are formed a filter for the MIC, and the C10 have same function.

The MICBIAS is used for bias the MIC through a resistor. The resistor value should be changed according the MIC.

The AVDD should be supplied by 3V. The CAP connected with AVDD should be placed as close as possible

The VCM is connected with GND through a 4.7uF CAP. The CAP should be placed as close as possible.

The audio output have two modes.One is capacity mode,the other is capless mode.In capacity

mode,need a 47uF or above capacitor , and there must be add a mute control circuit, shown as above diagram.And in capless mode,it need not add any components.

Chapter 2 I2C

2.1 Overview

The I2C module controls all registers in RK61X。

Features

External clock input for Chip working, this clock is 12MHz

Support I2C bus to APB bus convert

2.2 Block Diagram

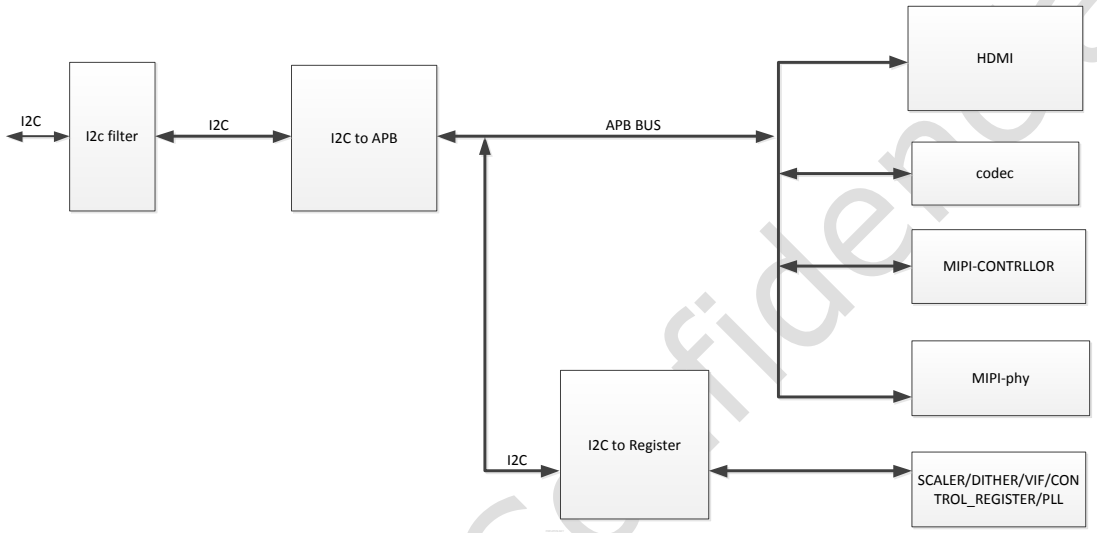

Fig. 2-1 I2C Block Diagram

I2C glitch filer module is used to filter glitch on I2C_SDA/I2C_SCL line.

I2C to APB block is used to control all blocks of RK61X.For scaler/ dither/vif/pll,they are I2C interface,we configure them directly through I2C bus.For HDMI/CODEC/MIPI-CONTROLLER/MIPI-PHY,they are APB interface, we configure them through I2C to APB module.

2.3 Function Description

2.3.1 I2C Write/Read operation

1. I2C Writing

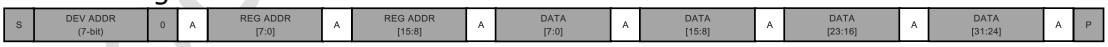

Fig. 2-2 I2C Writing Operation

2. I2C Reading

Fig. 2-3 I2C Reading Operation

For RK61X i2c slave, it expand the 7-bit addressing mode.

For I2C writing operation, please see Fig.22-2. I2C master works in tx only mode. First transmit DEVICE ADDR, then begin to transmit 2byte REGISTER ADDR, low 8-bit first transmit. And then transmit 4byte data, low 8-bit first transmit, the most 8-bit last transmit, then finish transaction. I2C slave receive each byte must return one ACK to I2C master.

For I2C reading operation, please see Fig.22-3. I2C master works in mix mode. First transmit 2byte REGISTER ADDR, write them into I2C module. Then restart(Sr), then transmit 1byte

DEVICE ADDR, and then read data from I2C slave, first receive low 8-bit, last receive the most 8-bit.

3. Register Address Assignment
The RK61X has only one device address, it is 0x50, all module use this device address.

2.4 I2C Timing Diagram

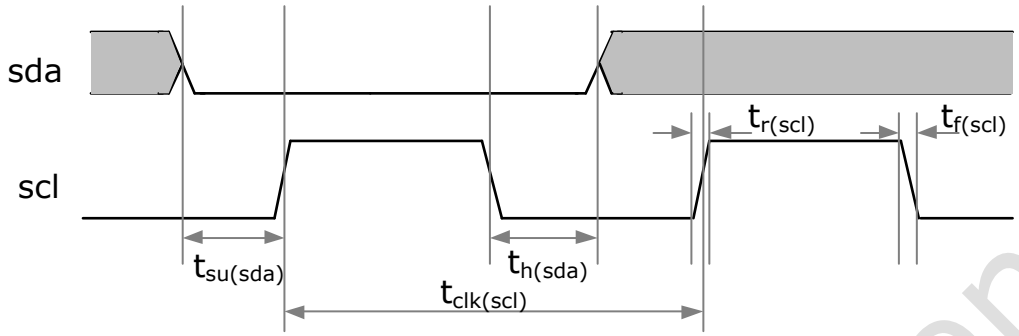

Fig. 2-4 I2C timing diagram

Table 2-1 I2C timing parameters

*timing condition: VCCIO=3.3V,

Parameter		Min.	Typ.	Max.	Unit
100KHz mode					
$t_{clk(scl)}$	SCL clock period	-	10	-	us
$t_{r(scl)}$	rise time for SCL	-	6.5	-	ns
$t_{f(scl)}$	fall time for SCL	-	6.0	-	ns
$t_{h(sda)}$	SDA hold time to falling edge of SCL	-	2.5	-	us
$t_{su(sda)}$	SDA setup time to rising edge of SCL	-	2.5	-	us
400KHz mode					
$t_{clk(scl)}$	SCL clock frequency	-	2.5	-	us
$t_{r(scl)}$	rise time for SCL	-	6.5	-	ns
$t_{f(scl)}$	fall time for SCL	-	6.0	-	ns
$t_{h(sda)}$	SDA hold time to falling edge of SCL	-	0.6	-	us
$t_{su(sda)}$	SDA setup time to rising edge of SCL	-	0.6	-	us

Chapter 3 MIPI D-PHY

3.1 Overview

The MIPI D-PHY integrates a MIPI® V1.0 compatible PHY that supports up to 1GHz high speed data receiver, plus a MIPI® low-power low speed transceiver that supports data transfer in the bi-directional mode. It supports the full specifications described in V1.0 of the D-PHY spec. The D-PHY is built in with a standard digital interface to talk to MIPI Host controller. The architecture supports connection of multiple data lanes in parallel – up to 4 data lanes can be connected to increase the total through-put, customizable to user determined configurations.The MIPI D-PHY supports the electrical portion of MIPI D-PHY V1.0 standard, covering all transmission modes (ULP/LP/HS).

The MIPI D-PHY supports the following features:

- Mixed-signal D-PHY mixed-signal hard-macro- LS Transmitter and LS/HS Receiver solution
- Designed to MIPI® v1.0 Specifications
- Integrated PHY Protocol Interface (PPI) supports interface to CSI, DSI and UniPro™ MIPI® protocols
- 1.0GHz maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 4Gbps transfer rate
- HS, LP and ULPS modes supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- Low-Power dissipation: HS less than 3mA/Lane
- Tx/Rx Buffers with tunable On-Die-Termination and advanced equalization.
- Embedded ESD, boundary scan support logic.

3.2 ELECTRICAL SPECIFICATIONS

3.2.1 DC SPECIFICATIONS

Table 3-1 HS Transmitter DC specifications

Parameter	Description	Min	Nom	Max	Unit	Note
V_{CMTX}	HS TX static Common-mode voltage	150	200	250	mV	1
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV	2
|VOD|	HS transmit differential voltage	140	200	270	mV	1
|ΔVOD|	V_{OD} mismatch when output is Differential-1 or Differential-0			10	mV	2
V_{OHHS}	HS output high voltage			360	mV	1
Z_{OS}	Single ended output impedance	40	50	62.5	ohm	
ΔZ_{OS}	Single ended output impedance mismatch			10	%	

1. Value when driving into load impedance anywhere in the ZID range.

2. It is recommended the implementer minimize ΔVOD and ΔVCMTX(1,0) in order to minimize radiation and optimize signal integrity.

Table 3-2 HS Transmitter DC specifications

Parameter	Description	Min	Nom	Max	Unit	Note
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input hysteresis	25			mV	

Table 3-3 LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Unit	Note
V_{OH}	The venin output high level	1.1	1.2	1.3	V	
V_{OL}	The venin output low level	-50		50	mV	
Z_{OLP}	Output impedance of LP transmitter	110			Ω	1

1. Though no maximum value for ZOLP is specified, the LP transmitter output impedance shall ensure theTRLP/TFLP specification is met.

3.2.2 AC specifications

Table 3-4 HS receiver AC specifications

Parameter	**Description**	**Min**	**Nom**	**Max**	**Unit**	**Note**
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450 MHz			100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz – 450MHz	-50		50	mV	1,4
C_{CM}	Common-mode termination			60	pF	3

1. Excluding 'static' ground shift of 50mV
2. ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.
4. Voltage difference compared to the DC average common-mode potential.

Table 3-5 LP receiver AC specifications

Parameter	**Description**	**Min**	**Nom**	**Max**	**Unit**	**Note**
e_{SPIKE}	Input pulse rejection			300	V.ps	1，2,3
T_{MIN-RX}	Minimum pulse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	

Parameter	Description	Min	Nom	Max	Unit	Note
f_{INT}	Interference frequency	450			MHz	

1. Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

Table 3-6 LP Transmitter AC specifications

Parameter	Description		Min	Nom	Max	Unit	Note
T_{RLP}/T_{FLP}	15%-85% rise time and fall time				25	ns	1
T_{REOT}	30%-85% rise time and fall time				35	ns	1,5,6
$T_{LP-PULSE-TX}$	Pulse width of exclusive-OR clock the LP	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4
		All other pulses	20				4
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock		90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF				500	mV/ns	1,3,7,8
	Slew rate @ C_{LOAD} = 5pF				300	mV/ns	1,3,7,8
	Slew rate @ C_{LOAD} = 20pF				250	mV/ns	1,3,7,8
	Slew rate @ C_{LOAD} = 70pF				150	mV/ns	1,3,7,8
	Slew rate @ C_{LOAD} = 0 to 70pF(Falling Edge Only)		30			mV/ns	1,2,3
	Slew rate @ C_{LOAD} = 0 to 70pF(Rising Edge Only)		30			mV/ns	1,3,9
	Slew rate @ C_{LOAD} = 0 to 70pF(Rising Edge Only)		30-0.075 * ($V_{O,INST}$ – 700)			mV/ns	1,10,11
C_{LOAD}	Load capacitance		0		70	pF	1

1. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

2. When the output voltage is between 400 mV and 930 mV.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in section 8.2.2.
5. The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
6. With an additional load capacitance CCM between 0 and 60pF on the termination center tap at RX side of the Lane
7. This value represents a corner point in a piecewise linear curve.
8. When the output voltage is in the range specified by VPIN(absmax).
9. When the output voltage is between 400 mV and 700 mV.
10. Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
11. When the output voltage is between 700 mV and 930 mV.

Chapter 4 LVDS

4.1 Overview

LVDS transmitter converts a CMOS signal into a low-voltage differential signal. Using a differential signal reduces the system's susceptibility to noise and EMI emissions. In addition, using a differential signal can deliver high speeds. This results in a very cost-effective solution to some of the greatest bandwidth bottlenecks in many transmission applications.

LVDS offers designers flexibility around their power supply solution, working equally well at 3.3V and lower. As a result, designers can reuse their LVDS solution even as systems move to lower voltages.

The LVDS transmitter in RK61X supports both single channel and dual channel.

4.1.1 Features

- 150MHz clock support
- Support single pixel and dual pixel interface
- 28:4 data sub_channel compression at data reate up to 1050Mbps per channel
- Support VGA,SVGA,XGA,SXGA and SXGA+
- PLL requires no external components
- LVTTL Combo I/O,support LVDS/TTL data output
- LVDS mode supply voltage: 1.2V/2.5V;LVTTL mode supply voltage:1.2V/3.3V
- Comply with the Standard TIA/EIA-644-A LVDS standard

4.2 Function description

4.2.1 lvds channel covert

lvds_channel_convert converts 24-bit RGB signal to two group 24-bit RGB signals.

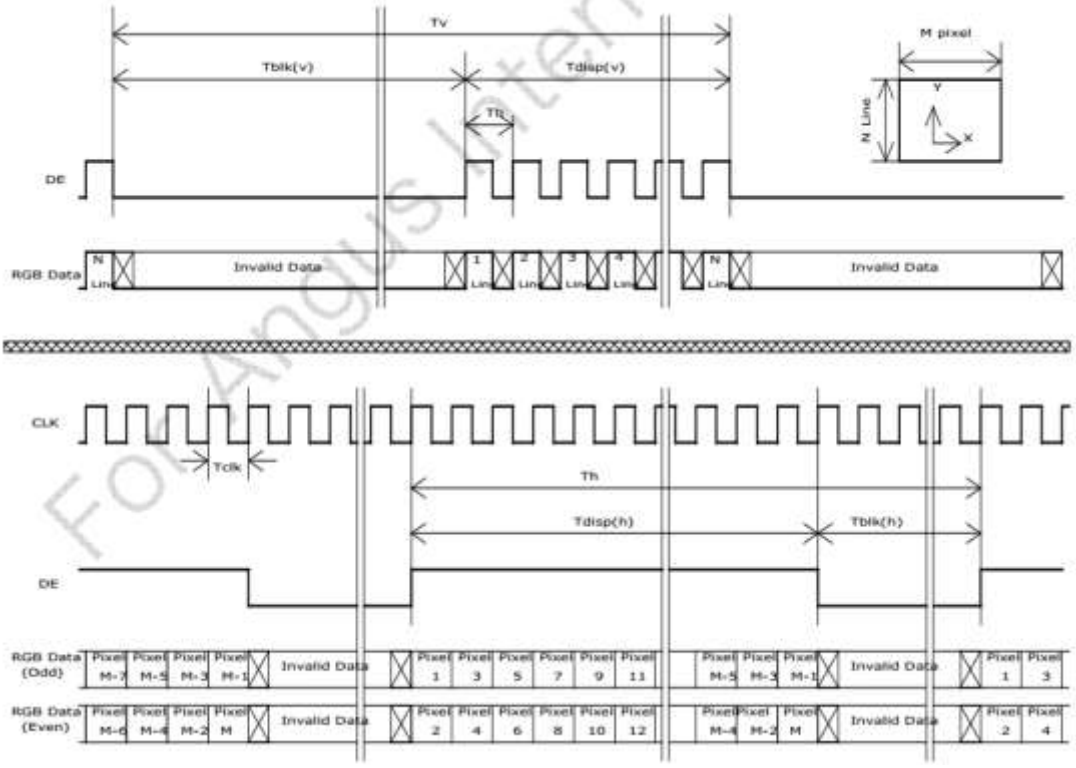

Fig. 4-1 lvds_channel_convert Timing

4.2.2 Truth table of LVDS Transmitter

Table 4-1 Truth Table of LVDS Transmitter

MODE	INPUT								OUTPUT	
	PDN_CBG	PD_PLL	PDN_1	OEN_1	PDN_2	OEN_2	Dn_m	Tq (1-20)	PADP/N_n &CLKP/N1 (n=1-4)	PADP/N_n &CLKP/N2 (n=5-8)
Dual LVDS Output	1	0	1	0	1	0	X	X	Refer to Figure 2	Refer to Figure 2
Single LVDS Output (CH1)	1	0	1	0	0	0	X	X	Refer to Figure 2	Z
LVTTL Output (CH1&2)	0	1	0	1	0	1	X	X	Tq (q=1~10)	Tq (q=11~20)
LVTTL Output (CH1)	0	1	0	1	0	0	X	X	Tq (q=1~10)	Z
Output Disable	x	0	0	0	0	0	X	X	Z	Z
Power Down	0	1	0	0	0	0	X	X	Z	Z

In default or after reset, LVDS Transmitter is in Power Down.

4.2.3 DC and AC Specification

This section provides DC and AC information of LVDS Transmitter. It includes the absolute maximum rating conditions for 2.5V(LVDS output mode) I/O application in Table22-2 and 3.3V(LVTTL output mode) I/O application in Table22-3 ,absolute maximum rating condition can either caused device reliability problem or damage the device sufficiently to cause immediate failure. Transmitter DC electrical specifications are showed in Table22-4. AC specifications are characterized in three operating condition. Those are worst-case, typical-case and best-case conditions and the detail of each condition are listed in the Table22-5 and Table22-6 and AC electrical specifications of transmitter are showed in Table22-7.

Please be kindly reminded that the LVDS output mode could only work under 2.5V I/O application, and LVTTL output mode works under 3.3V I/O application.

Table 4-2 Absolute Maximum Rating for 2.5V LVDS Output Application

Symbol	Parameter	Conditions	Minimum	Normal	Maximum
VDDDLVD	LVDS post-driver analog power		2.25V	2.5V	2.75V
VDDPLVD	LVDS level shifter power		2.25V	2.5V	2.75V
VDDPLL	PLL power		2.25V	2.5V	2.75V
VDD	LVDS & Serializer pre-driver power	±10%	1.08V	1.2V	1.32V
V_O	Pad output voltage (PADP_n, PADN_n)		0V	VDDDLVD	2.75V
V_{IC}	Core input voltage (Dn_m, OEN_n, PDN_n)		0V	VDD	1.32V
T_{OPT}	Operating temperature		0°C	25°C	125°C

Table 4-3 Absolute Maximum Rating for 3.3V LVTTL Output Application

Symbol	Parameter	Conditions	Minimum	Normal	Maximum
VDDDLVD	LVDS post-driver analog power		2.97V	3.3V	3.63V
VDDPLVD	LVDS level shifter power		2.97V	3.3V	3.63V
VDDPLL	PLL power		2.97V	3.3V	3.63V
VDD	LVDS & Serializer pre-driver power	±10%	1.08V	1.2V	1.32V
V_O	Pad output voltage (PADP_n, PADN_n)		0V	VDDDLVD	3.63V
V_{IC}	Core input voltage (Dn_m, OEN_n, PDN_n)		0V	VDD	1.32V
T_{OPT}	Operating temperature		0°C	25°C	125°C

Table 4-4 LVDS Transmitter DC Electrical Specifications

Symbol	Parameter	Conditions	Minimum	Maximum
V_{oh}	Output voltage high, V_{oa} or V_{ob}	Rload = 100Ω±1%		1475mV
V_{ol}	Output voltage low, V_{oa} or V_{ob}	Rload = 100Ω±1%	925mV	
$\lvert V_{od} \rvert$	Output differential voltage	Rload = 100Ω±1%	250mV	450mV
V_{os}	Output offset voltage	Rload = 100Ω±1%	1125mV	1375mV
$\lvert \Delta V_{od} \rvert$	Change in $\lvert V_{od} \rvert$ between '0' and '1'	Rload = 100Ω±1%		50mV/150mV#
ΔV_{os}	Change in V_{os} between '0' and '1'	Rload = 100Ω±1%		50mV
I_{sa}, I_{sb}	Output current	Transmitter shorted to ground		24mA
I_{sab}	Output current	Transmitter shorted to ground		12mA

Table 4-5 LVDS Transmitter AC Characterization Condition for 2.5V I/O Application

Type	Condition
Typical case	VDDDLVD=2.5V, VDDPLVD=2.5V, VDDPLL=2.5V, VDD=1.2V, temperature=25℃ Process = Typical-Typical
Best case	VDDDLVD=2.75V, VDDPLVD=2.75V, VDDPLL=2.75V, VDD=1.32V temperature=0℃ Process = Fast-Fast
Best case (High temperature)	VDDDLVD=2.75V, VDDPLVD=2.75V, VDDPLL=2.75V, VDD=1.32V temperature=125℃ Process = Fast-Fast
Best case (Low temperature)	VDDDLVD=2.75V, VDDPLVD=2.75V, VDDPLL=2.75V, VDD=1.32V temperature=-40℃ Process = Fast-Fast
Worst case (High temperature)	VDDDLVD=2.25V, VDDPLVD=2.25V, VDDPLL=2.25V, VDD=1.08V temperature=125℃ Process =Slow-Slow
Worst Case (Low temperature)	VDDDLVD=2.25V, VDDPLVD=2.25V, VDDPLL=2.25V, VDD=1.08V temperature=-40℃ Process =Slow-Slow

Table 4-6 LVDS Transmitter AC Characterization Condition for 3.3V I/O Application

Type	Condition
Typical case	VDDDLVD=3.3V, VDDPLVD=3.3V, VDDPLL=3.3V, VDD=1.2V, temperature=25℃ Process = Typical-Typical
Best case	VDDDLVD=3.63V, VDDPLVD=3.63V, VDDPLL=3.63V, VDD=1.32V temperature=0℃ Process = Fast-Fast
Best case (High temperature)	VDDDLVD=3.63V, VDDPLVD=3.63V, VDDPLL=3.63V, VDD=1.32V temperature=125℃ Process = Fast-Fast
Best case (Low temperature)	VDDDLVD=3.63V, VDDPLVD=3.63V, VDDPLL=3.63V, VDD=1.32V temperature=-40℃ Process = Fast-Fast
Worst case (High temperature)	VDDDLVD=2.97V, VDDPLVD=2.97V, VDDPLL=2.97V, VDD=1.08V temperature=125℃ Process =Slow-Slow
Worst Case (Low temperature)	VDDDLVD=2.97V, VDDPLVD=2.97V, VDDPLL=2.97V, VDD=1.08V temperature=-40℃ Process =Slow-Slow

LVDS Transmitter's timing is characterized with transmission line and measured at the receiver side. The test circuit and the three-state enable time's measure point are shows in the Figure22-3 and Figure22-4.

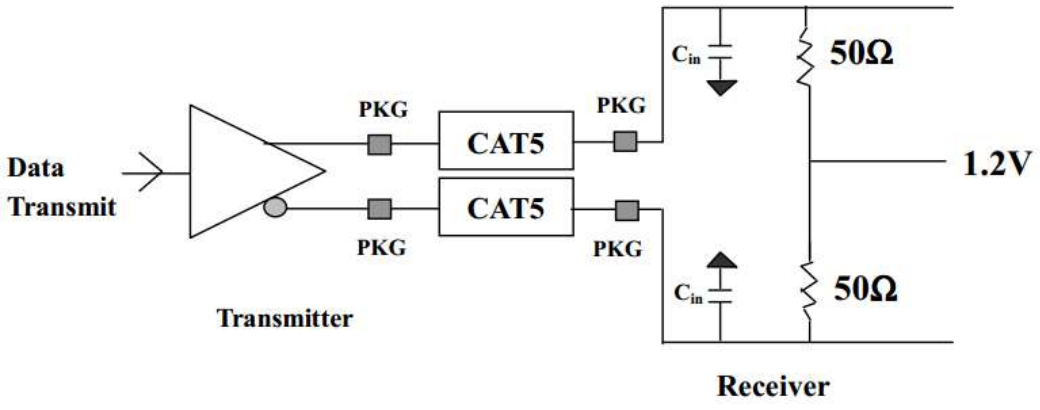

Fig. 4-2 Test Circuit of Three-state Enable Time

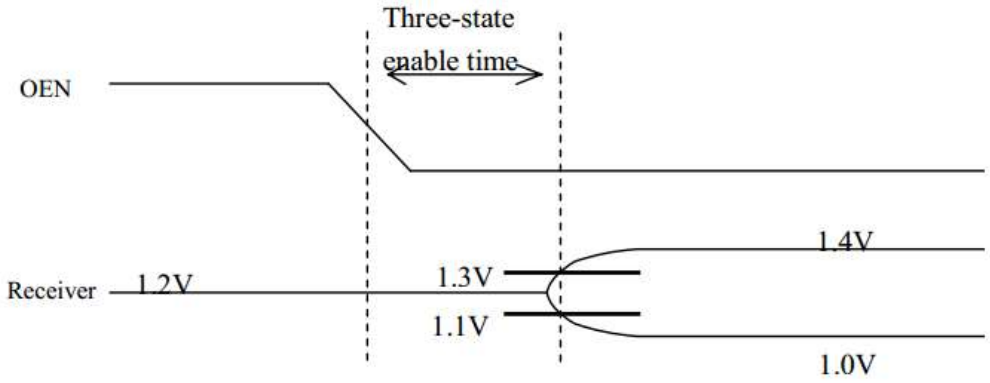

Fig. 4-3 Three-state Enable Time Measure Point

Table 4-7 LVDS Transmitter AC Electrical Specifications

Symbol	Parameter	Conditions	Min	Typ	Max
Clock	Clock signal duty cycle	135MHz		57%	
t_{fall}	V_{od} fall time, 20~80%	R_{load}= 100Ω±1%	260ps		0.3*Tui#
t_{rise}	V_{od} rise time, 20~80%	R_{load}= 100Ω±1%	260ps		0.3*Tui
T_{skew1}	$\lvert t_{phla} - t_{plhb} \rvert$ or $\lvert t_{phlb} - t_{plha} \rvert$, differential skew	R_{load}= 100Ω±1%			50ps
t_{TS}#	Data setup to CK_REF (135MHz)		2.1ns		
t_{TH}#	Data hold from CK_REF (135MHz)		1.9ns		
t_{TS}#	Data setup to CK_REF (85MHz)		2.7ns		
t_{TH}#	Data hold from CK_REF (85MHz)		2.5ns		
t_{TS}#	Data setup to CK_REF (20MHz)		8.2ns		
t_{TH}#	Data hold from CK_REF (20MHz)		8ns		

4.3 Interface description

4.3.1 LVDS Transmitter Output

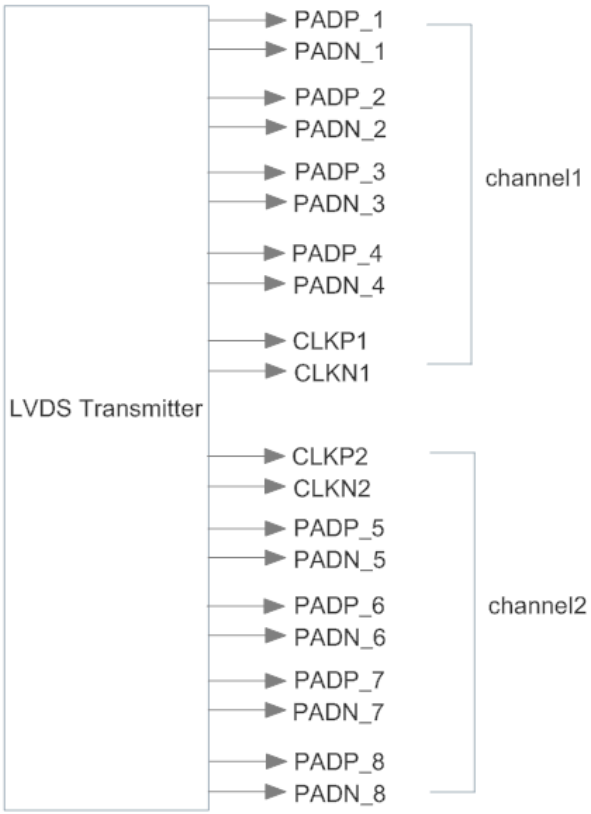

Fig. 4-4 LVDS Transmitter Interface

When single channel mode, use channel1, channel2 output Z.
When dual channel mode, use channel1 and channel2.

Chapter 5 HDMI

5.1 Overview

HDMI TX is consisted of HDMI Transmitter Controller and HDMI Transmitter PHY which is fully compliant with HDMI 1.4a specification, supporting 3D Display and up to 4Kx2K highest HD display grade.

The HDMI TX provide functionality to transmit digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. HDMI TX can carry high quality multi-channel audio data and can carry all standard and high-definition consumer electronics video formats. Content protection technology is available. HDMI TX offers a simple implementation for system on chip (SOC) for consumer electronics like DVD player/recorder and camcorder.

The HDMI TX is optimized for high speed (up to 3.4Gbps per TMDS link) High-Definition applications with robust timing and small silicon area in many process. HDMI TX contains controller and transmitter PHY circuit with programmable pre-emphasis, slew rate, output voltage swing and resistor values to drive transmit data with optimal signal quality and distance over the standard HDMI cable to a standard HDMI display device. The HDMI TX PHY contains all HDMI components including all I/O Library, high performance wide range PLL, the data symbol conversion/synchronization unit. The high performance drive and capture circuit is capable of working in the range of 250Mbps, 1.65Gbps, all the way up to 3.4Gbps in HDMI 1.4 standard per a TMDS pair.

The HDMI TX controller supports up to 300 MHz digital core design in many process, high definition multimedia interface (HDMI) v 1.4a compliant transmitter. It supports all mandatory and optional 3D video formats defined in the HDMI specification 1.4a. HDTV formats up to 1080p with up to 48 bit deep color. With the inclusion of HDCP, the HDMI TX allows the secure transmission of protected content as specified by the HDCP v.1.2 protocol. The HDMI TX helps reduce system design complexity and cost by incorporating such add on features as an I2C master for EDID reading, 5V tolerance on the I2C and hot plug detect pins, and CEC for high-level control functions between all of the various audiovisual products in a user's environment.

5.1.1 Features

- Very low power operation, less than 60mW in PHY during 1080P HD display
- HDMI 1.4/1.3/1.2/1.1, HDCP 1.2 and DVI 1.0 standard compliant transmitter
- Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
- Support 3D function defined in HDMI 1.4 spec
- TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
- Supports all DTV resolutions including 480i/576i/480p/576p/720p/1080i/1080p
- Digital video interface supports a pixel size of 24, 30, 36, 48bits color depth in RGB
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-192kHz Fs) using IEC60958 and IEC 61937
- Multiphase 4MHz fixed bandwidth PLL with low jitter
- DDC Bus I2C master interface at 3.3V
- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data

- Support HDMI LipSync if needed as addon feature
- Lower power operation with optimal power management feature
- Embedded ESD, scan support logic.
- The EDID and CEC function are also supported by HDMI Transmitter Controller
- Optional Monitor Detection supported through Hot Plug
- Optional HDMI controller solution available

5.2 Electrical Specification

HDMI Transmitter contains tunable source termination and pre-emphasis to enable high speed operation. The Transmitter meets the AC specifications below across all operating conditions specified. Rise and fall times are defined as the signal transition time between 20% and 80% of the nominal swing voltage (Vswing) of the device under test. The Transmitter intra-pair skew is the maximum allowable time difference (on both low-to-high and high-to-low transitions) as measured at TP1, between the true and complement signals of a given differential pair. This time difference is measured at the midpoint on the single-ended signal swing of the true and complement signals. The Transmitter inter-pair skew is the maximum allowable time difference (on both low-to-high and high-to-low transitions) as measured at TP1.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{REF}	Reference Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	$mV_{p.p}$
T_A	Ambient Temperature (with power applied)	0	25	70	℃

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}[1.2]	Supply Voltage 3.3V	-0.3		4.0	V
V_1[1.2]	Input Voltage	-0.3		V_{CC}+0.3	V
V_0[1.2]	Output Voltage	-0.3		V_{CC}+0.3	V
V_J[1.2]	Junction Temperature (with power applied)			125	℃

Transmitter DC Characteristics at TP1

Item	Value
Single-ended high level output voltage, V_H	AV_{cc}-10mV< V_H < AV_{cc}+10mV when sink <= 165Mhz
	AV_{cc}-200mV< V_H < AV_{cc}+10mV when sink >165Mhz
Single-ended low level output voltage, V_L	(AV_{cc} – 600mV) < V_L < (AV_{cc} – 400mV) when sink < =165Mhz
	(AV_{cc} – 700mV) < V_L < (AV_{cc} – 400mV) when sink > 165Mhz
Single-ended output swing voltage, V_{swing}	400mV < V_{swing} < 600mV

Item	Value
Single-ended standby (off) output voltage, V_{OFF}	AV_{cc}+-10mV
Single-ended standby (off) output current, I_{OFF}	$\lvert I_{OFF} \rvert$ < 10uA

Transmitter AC Characteristics at TP1

Item	Value
Rise time/fall time (20%-80%)	75psec < Rise time/fall time < 0.4 T_{bit}
Overshoot, max	15% of full differential amplitude (V_{swing}*2)
Undershoot, max	25% of full differential amplitude e (V_{swing}*2)
Intra-Pair Skew at Transmitter Connector, max	0.15 T_{bit}
Inter-Pair Skew at Transmitter Connector, max	0.20 T_{pixel}
TMDS Differential Clock Jitter, max	0.25 T_{bit}
Clock duty cycle	40% to 60%

Programmable Output Resistance and Output Equalization Level

Item	Value
Output Equalization level	10% to 60%
Termination Resistance	50ohm and 75 ohms selectable with fine steps
Output Swing Ranges	4 different levels

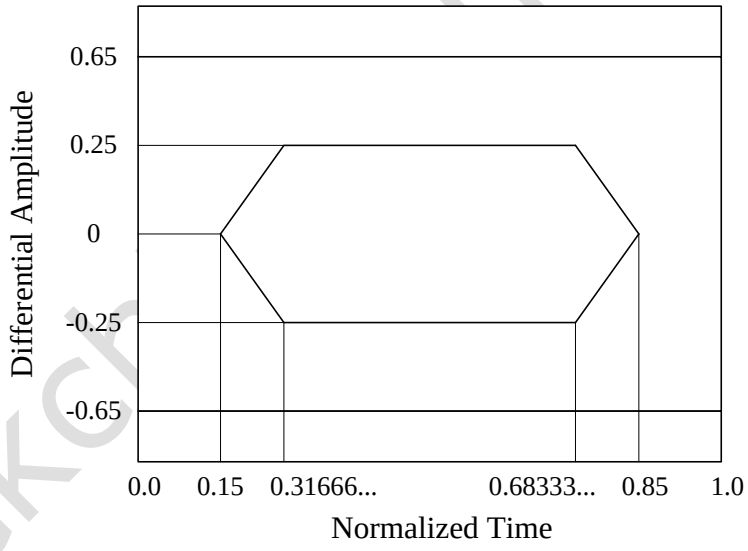

Fig. 5-1 The Eye Diagram of Differential TMDS Signals

The transmitter PHY will meet the above are the normalized eye diagram mask requirements at TP1 points for any data or clock TMDS output.

5.2.1 Control Signal – DDC

DDC (Display Data Channel) control signals follow the I2C Bus specifications. More details to be filled out from I2C specs.

Item	Value
High Voltage Level (Vih)	2.4V < Vih < 5.3V
Low Voltage Level (Vil)	0V < Vil < 0.4V
SCL clock frequency	100KHz (max)
Rise time	< 1000ns

Item	Value
Fall time	< 300ns
Capacitive load on bus line	400pF

5.2.2 Control Signal – HPD

HPD (Hot Plug Detect) signal is used by the source to read the sink's E-DID. The sink needs to meet the following requirements for reliable detection.

For Sink

Item	Value
High Voltage Level (Vih)	2.4V < Vih < 5.3V
Low Voltage Level (Vil)	0V < Vil < 0.4V

For Source

Item	Value
High Voltage Level (Voh)	2.0V < Voh < 5.3V
Low Voltage Level (Vol)	0V < Vol < 0.8V

Chapter 6 Audio Codec

6.1 Overview

The ADC with 16 to 24bit resolution, DAC with 16 to 18bit resolution and power amplifier are integrated in the Audio Codec.

Key Features

1 Pure logic process, no need for Mixed signal process.
2 Very low power, can be made <6.5mA in 3.3V for playback.
3 18 to 24 bit high order Sigma-Delta modulation for DAC with >93 dB SNR.
4 16 to 18 bit high order Sigma-Delta modulation for ADC with >90 dB SNR.
5 Digital interpolation and decimation filter integrated.
6 Line-in, microphone and speaker out interface.
7 On-chip analog post filter and digital filters.
8 Single–ended or differential microphone input.
9 Automatic gain control for smooth audio recording.
10 Sampling rate of 8k/12k/16k/24k/32k/48k/44.1k/96k Hz
11 Support 16ohm to 32ohm headphone and speaker phone output.
12 3.3V analog +/-10% power supply for analog and 1.2/1.1/1.0V for digital core.
13 Mono, Stereo supported.

6.2 Electrical Specification

TEST Conditions
AVDD=3.3V, T_A=27℃, 1 KHz sine input, fs = 6.144 MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Preamp Inputs						
Full-scale Input Signal Level	V_{INFS}	$GAIN_B$ =0dB $GAIN_P$ =0dB		1.1		Vrms
Input resistance	R_{MICIN}	$GAIN_B$ =0dB		14.5		KΩ
		$GAIN_B$ =20dB		79.75		KΩ
Input Gain Boost						
Programmable GAIN	$GAIN_B$		0		20	dB
Programmable GAIN Step Size			-	20	-	dB
Gain of PGA_L(PGA_R)						
Boost Gain	$GAIN_P$		-18		28.5	dB
Boost Gain Step Size				1.5		dB
Analogue to Digital Converter（ADC）						
Signal to Noise Ratio	SNR	$GAIN_P$=0dB $GAIN_B$ =0dB		90		dB
Channel Separation				70		dB
Digital to Analogue Converter(DAC) ,without load						
DAC output GAIN	$GAIN_D$		-39		6	dB
DAC output GAIN Step Size				1.5		dB
Signal to Noise Ratio	SNR	$GAIN_D$=0dB		93		dB
Total Harmonic Distortion	THD	$GAIN_D$=0dB Without Load		-80		dB
Total Harmonic	THD	$GAIN_D$=0dB		-70		dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Distortion		With 32Ω load				

6.3 I2S Timing Diagram

Master mode

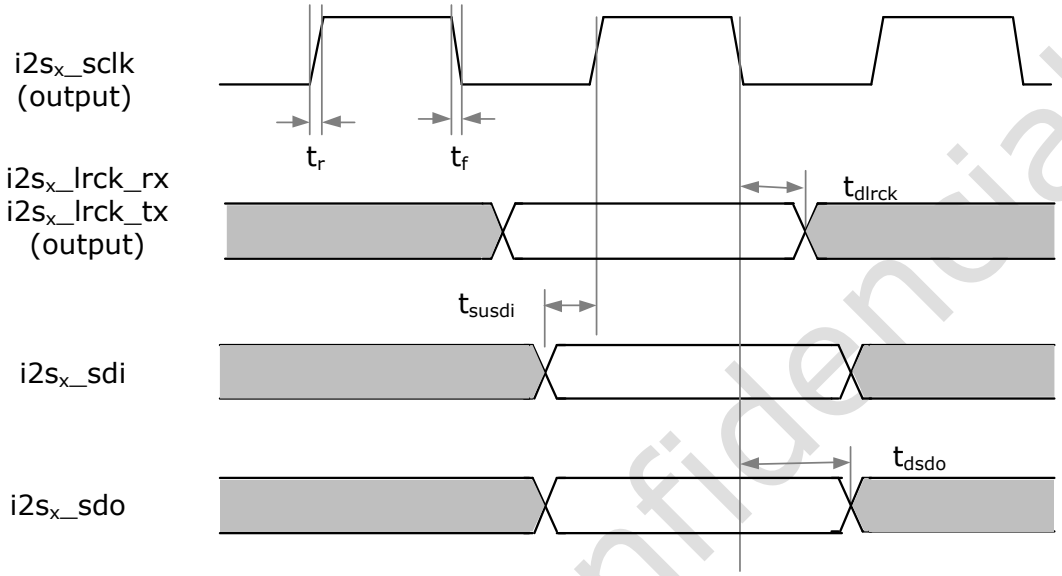

Fig. 6-1 Master mode timing diagram

Table 6-1 Meaning of the parameter in Fig. 9-1

*timing condition: VCCIO=3.3V, C_{LOAD}≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t_r	i2sx_sclk(output) rising time	-	-	39.84	ns
t_f	i2sx_sclk(output) falling time	-	-	39.84	ns
t_{dlrck}	i2sx_lrck_rx/i2sx_lrck_tx propagation delay from i2sx_sclk falling edge	3.96			ns
t_{susdi}	i2sx_sdo setup time to i2sx_sclk rising edge	4.86			ns
t_{dsdo}	i2sx_sdi propagation delay from i2sx_sclk falling edge	3.91		1.2	ns

Slave mode

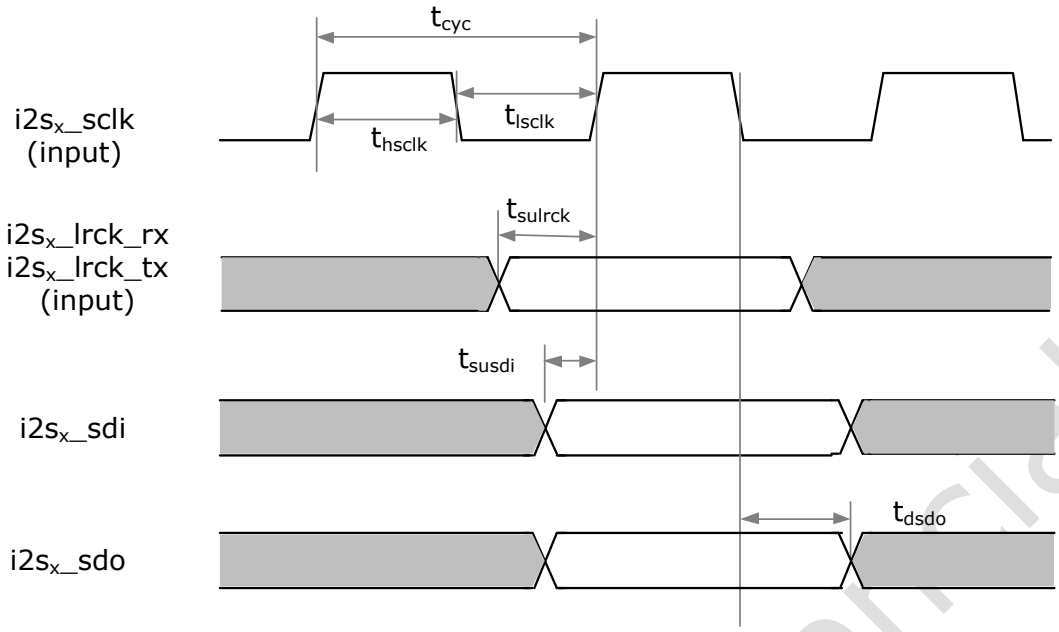

Fig. 6-2 Slave mode timing diagram

Table 6-2 Meaning of the parameter in Fig. 9-2

*****timing condition: VCCIO=3.3V, $C_{LOAD} \leqslant 8pF$, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t_{cyc}	$i2s_x$_sclk cycle time	-	-	20	ns
t_{hsclk}	$i2s_x$_sclk pulse width high	-	-	10	ns
t_{lsclk}	i2sx_sclk pulse width low	-	-	10	ns
t_{sulrck}	$i2s_x$_lrck_rx/$i2s_x$_lrck_tx setup time to i2sx_sclk rising edge	3.94	-	-	ns
t_{susdi}	$i2s_x$_sdo setup time to $i2s_x$_sclk rising edge	2.06	-	-	ns
t_{dsdo}	$i2s_x$_sdi propagation delay from $i2s_x$_sclk falling edge	5.2	-	11.0	ns