

Rockchip

RK912

Datasheet

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Revision History

Date	Revision	Description
2018-07-12	1.2	● Correct some information
2017-12-09	1.1	● Add power up sequence information
2017-11-19	1.0	● Initial Release

Table of Content

Table of Content	3
Figure Index	4
Table Index 5	
Chapter 1 Introduction	7
1.1 Overview.....	7
1.2 Features.....	7
1.3 Block Diagram	8
Chapter 2 Package information	9
2.1 Dimension	9
2.2 Ball Pin Number Order	10
2.3 Power/ground IO descriptions	11
2.4 Power Sequence.....	11
2.5 Function IO description	11
2.6 IO pin name descriptions.....	13
Chapter 3 Electrical Specification	15
3.1 Absolute Maximum Ratings.....	15
3.2 Recommended Operating Conditions.....	15
3.3 DC Characteristics	15
Chapter 4 Power Consumption	17
Chapter 5 RF Characteristic.....	18

Figure Index

Fig. 1-1 Block Diagram	8
Fig. 2-1 Package Top and SideView	9
Fig. 2-2 Package Bottom View	9
Fig. 2-3 Package Dimension	10
Fig. 2-4 Power Up Sequence with GPIO 3.3V mode	11
Fig. 2-5 Power Up Sequence with GPIO 1.8V mode	11

Table Index

Table 2-1 Ball Pin Number Order Information	10
Table 2-2 Power/Ground IO information	11
Table 2-3 Function IO description	11
Table 2-4 RK912 IO Function Description List.....	13
Table 3-1 RK912 Absolute Maximum Ratings	15
Table 3-2 RK912 Recommended Operating Condition	15
Table 3-3 RK912 DC Characteristics.....	15
Table 4-1 RK912 Power Consumption Data	17
Table 5-1 RK912 RF Characteristic Data	18

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Chapter 1 Introduction

1.1 Overview

RK912 is a low power WLAN connectivity chip for portable media device, which supports IEEE 802.11b/g/n.

RK912 provides a compact ultra-small form factor solution with minimal external components to drive the costs for mass volumes and allows for flexibility in size, form, and function. Taking advanced design techniques and process technology to deliver the lowest active and idle power, RK912 extends the system battery life while maintaining consistent connectivity and still provides a rich set of features.

RK912 is a very highly integrated design with internal PA, TR switch, Balun, LNA for low BOM cost. The chip is embedded with low power and low cost processor to talk with host device. With the internal processor, RK912 firmware can be flexibly developed for meeting different customer production application requirement.

RK912 provides the automatic hardware calibration solution to tune the RF characteristic to achieve best RF performance, which can avoid RF performance penalty causing by the hardware board differentiation.

1.2 Features

1.2.1 Wireless Interface

- Integrated TR switch, BALUN, LNA, Power Amplifier and matching network in a single chip for 802.11 b/g/n compatible WLAN chip
- Complete 802.11n solution for 2.4GHz band and 20MHz bandwidth
- Standards Supported
 - IEEE 802.11b/g/n compatible WLAN
 - IEEE 802.11e QoS Enhancement(WMM)
 - 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- MAC
 - HW/SW partition optimized to minimize power consumption
 - Frame aggregation for increased MAC efficiency(A-MSDU,A-MPDU)
 - Low latency immediate High-Throughput Block Acknowledgement(HT-BA)
 - Power saving mechanism
 - Channel management and co-existence
- PHY Feature
 - SISO
 - IEEE 802.11n OFDM
 - One Transmit and one Receive path(1T1R)
 - 20Mhz bandwidth transmission
 - Transmit power up to 16dBm
 - Meets or exceeds standard specified sensitivity requirements including ACI/AACI
 - Dynamic power management based on packet signal quality
 - Optimized listen mode power consumption
 - DSSS with DBPSK and DQPSK,CCK modulation with long and short preamble
 - OFDM with BPSK, QPSK, 16QAM and 64QAM modulation. Convolutional Coding

Rate: 1/2, 2/3, 3/4 and 5/6

- Maximum data rate 11Mbps in 802.11b, 54Mbps in 802.11g and 65Mbps in 802.11n
- Switch diversity for DSSS/CCK
- Fast receiver Automatic Gain Control(AGC)

- Support STA, AP and P2P operation modes

1.2.2 SDIO interface

- Compliant with SDIO Specification Version 3.00
- Support 4bit data bus width
- Support 2 Functions
- Support DMA operation for high speed data transfer
- Support Dual-Buffer mode to optimize throughput

1.2.3 Others

- Embedded power regulator for BOM cost save and high power utilization efficiency
- Embedded RTC OSC for low power mode working
- With large enough buffer to reach high TX and RX data throughput, which make sure better user experience
- Package Type: QFN40(body: 5mmx5mm)

1.3 Block Diagram

The following diagram shows the basic block diagram.

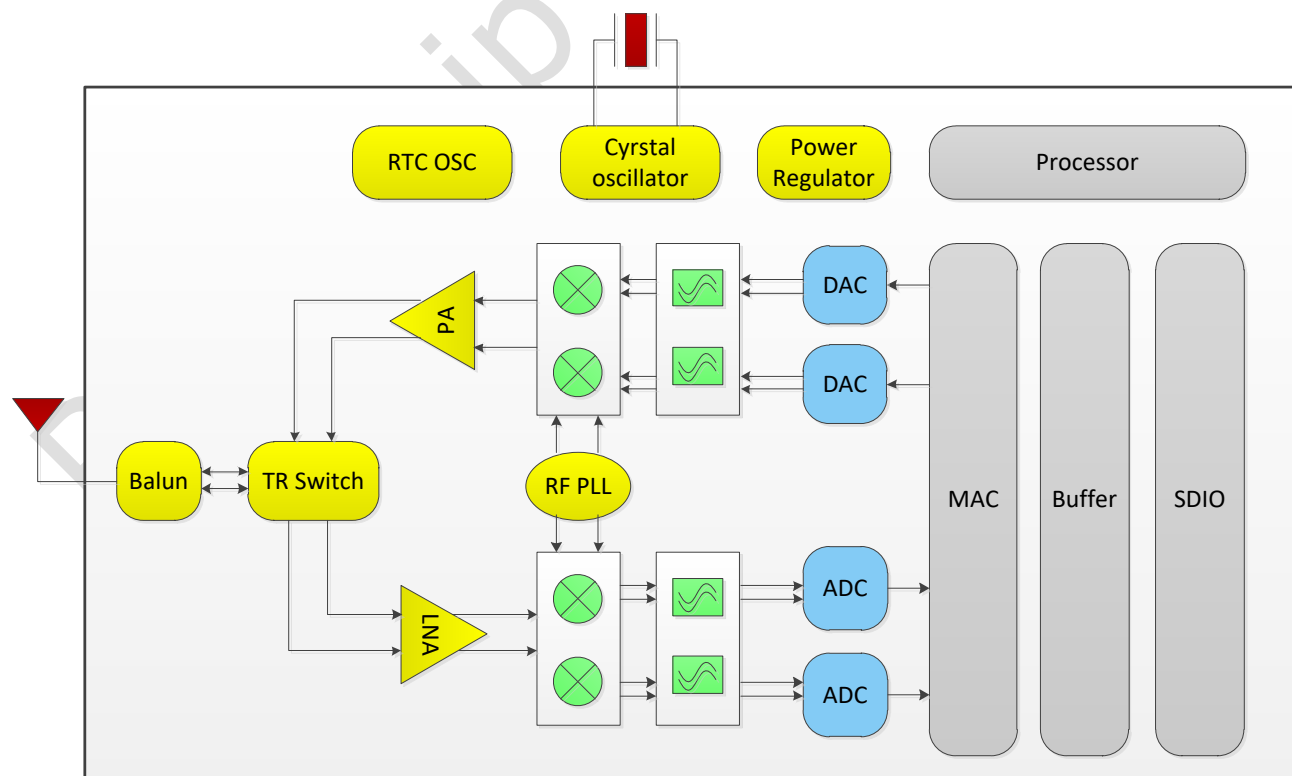


Fig. 1-1 Block Diagram

Chapter 2 Package information

2.1 Dimension

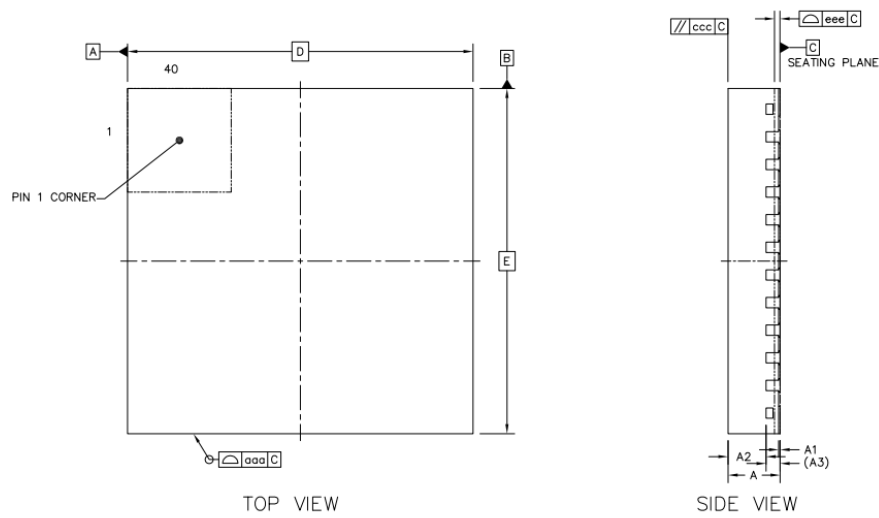


Fig. 2-1 Package Top and Side View

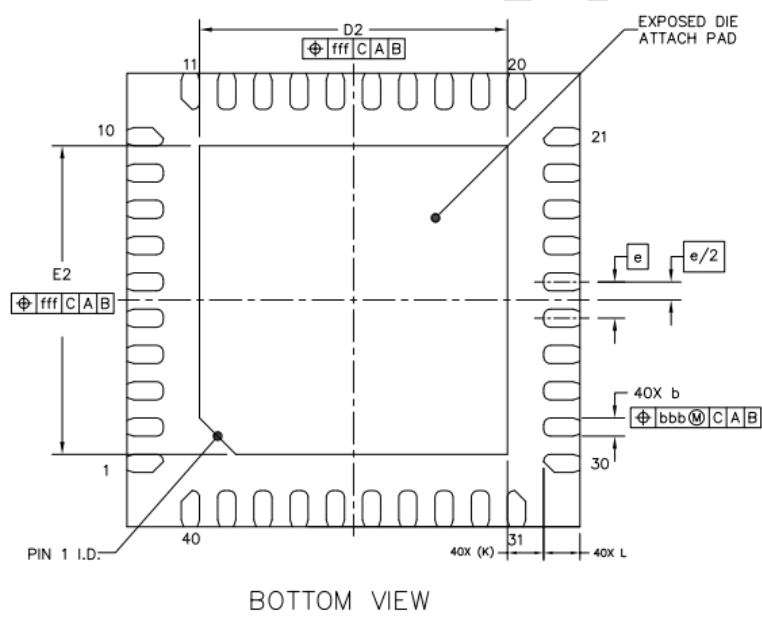


Fig. 2-2 Package Bottom View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	5 BSC		
	Y	E	5 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K	0.4 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.07		
EXPOSED PAD OFFSET		fff	0.1		

Fig. 2-3 Package Dimension

2.2 Ball Pin Number Order

Table 2-1 Ball Pin Number Order Information

Pin Number	Pin Name	Pin Number	Pin Name
1	IO_SDIOclk_SDIOgpio0a0	21	RF_PAD_QP_TRX
2	IO_SDIOcmd_SDIOgpio0a1	22	RF_PAD_QN_TRX
3	IO_SDIOdata0_SDIOgpio0a2	23	RF_PAD_IN_TRX
4	VSS	24	RF_PAD_IP_TRX
5	IO_SDIOdata1_M0JTAGtck_AONJTAGtck_PMUst0_SDIOgpio0a3	25	RF_VDD18_L0
6	IO_SDIOdata2_M0JTAGtms_AONJTAGtrstn_PMUst1_SDIOgpio0a4	26	VSS
7	VSS	27	RF_PAD_XI
8	IO_SDIOdata3_UARTDBGsout_AONJTAGtms_PMUst2_SDIOgpio0a5	28	RF_PAD_XO
9	IO_RTCclk32k_BTconfirm_BTpti0_SDIOgpio0a6	29	VSS
10	VDD	30	RF_VDD18_L1
11	VDD3318_GPIO	31	RF_VDD18_L2
12	VDD	32	RF_PAD_REFRES
13	IO_DEVICEirq_SDIOgpio0a7	33	RF_VDD18_T
14	VSS	34	RF_VDD18_T
15	IO_BTmbsy_PMUst3_SDIOgpio0b0	35	NC
16	IO_BTrntx_UARTDBGsoutb_AONJTAGtdi_PMUst4_SDIOgpio0b1	36	RF_PAD_RFIO
17	IO_BTdeny_TESTclkout_AONJTAGtdo_M0wfi_SDIOgpio0b2	37	NC
18	VSS	38	RF_VDD33
19	IO_TESTJTAGtrstn	39	IO_LDO_VDD_33V
20	IO_Npor	40	IO_LDO_VDD_18V

2.3 Power/ground IO descriptions

Table 2-2 Power/Ground IO information

Group	Pin#	Descriptions
VSS	4,7,14,18,26,29	Digital Ground
AVSS	Exposed-GND	Analog Ground
VDD	10,12	Logic Power
VDD3318_GPIO	11	GPIO Power
RF_VDD18_L0	25	RF Analog Power
RF_VDD18_L1	30	RF Analog Power
RF_VDD18_L2	31	RF Analog Power
RF_VDD18_T	33,34	RF Analog Power
RF_VDD33	38	RF Analog Power
IO_LDO_VDD_33V	39	LDO Analog Power

2.4 Power Sequence

Refer to 2.4.1 and 2.4.2 for Power up sequence. There is no special requirement for power down sequence

2.4.1 VDD3318_GPIO supply with 3.3V mode

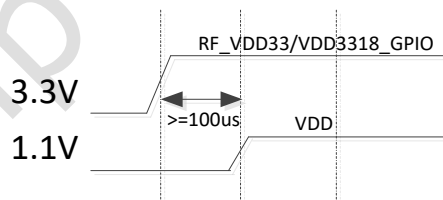


Fig. 2-4 Power Up Sequence with GPIO 3.3V mode

2.4.2 VDD3318_GPIO supply with 1.8V mode

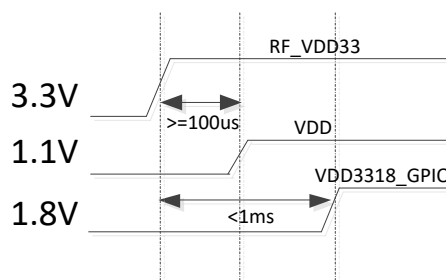


Fig. 2-5 Power Up Sequence with GPIO 1.8V mode

2.5 Function IO description

Table 2-3 Function IO description

Pad#	Pin#	func1	func2	func3	func4	Pad Type ^①	Drive Strength ^②	Pull	Power Supply
IO_SDIOclk_SDIOgpio0a0	1	sdio_clk				I/O	8mA	up	VDD3318_GPIO
IO_SDIOcmd_SDIOgpio0a1	2	sdio_cmd				I/O	8mA	up	
IO_SDIOdata0_SDIOgpio0a2	3	sdio_data0				I/O	8mA	up	
IO_SDIOdata1_M0JTAGtck_AONJT AGtck_PMuSt0_SDIOgpio0a3	5	sdio_data1	m0jtag_tck	aonjtag_tck	pmu_st0	I/O	8mA	up	
IO_SDIOdata2_M0JTAGtms_AONJ TAGtrstn_PMuSt1_SDIOgpio0a4	6	sdio_data2	m0jtag_tms	aonjtag_trstn	pmu_st1	I/O	8mA	up	
IO_SDIOdata3_UARTDBGsout_AO NJTAGtms_PMuSt2_SDIOgpio0a5	8	sdio_data3	uartdbg_sout	aonjtag_tms	pmu_st2	I/O	8mA	up	
IO_RTCclk32k_BTconfirm_BTpti0_ SDIOgpio0a6	9	rtc_clk32k	bt_confirm	bt_pti0		I/O	8mA	down	
IO_DEVICEirq_SDIOgpio0a7	13	device_irq				I/O	8mA	down	
IO_BTmbsy_PMuSt3_SDIOgpio0b0	15	bt_mbsy	pmu_st3			I/O	8mA	down	
IO_BTrxntx_UARTDBGsoutb_AONJ TAGtdi_PMuSt4_SDIOgpio0b1	16	bt_rxntx	uartdbg_soutb	aonjtag_tdi	pmu_st4	I/O	8mA	down	
IO_BTdeny_TESTclkout_AONJTAGt do_M0wfi_SDIOgpio0b2	17	bt_deny	test_clkout	aonjtag_tdo	m0_wfi	I/O	8mA	down	
IO_TESTJTAGtrstn	19					I	8mA	down	
IO_Npor	20					I	8mA	up	
IO_RFPADqptrx	21					A	NA	NA	RF
IO_RFPADqntx	22					A	NA	NA	
IO_RFPADintrx	23					A	NA	NA	
IO_RFPADiptrx	24					A	NA	NA	
IO_RFPADxi	27					A	NA	NA	
IO_RFPADxo	28					A	NA	NA	
IO_RFPADrefres	32					A	NA	NA	
IO_RFPADrfio	36					A	NA	NA	

Notes:

①: Pad types: I = input, O = output, I/O = input/output (bidirectional),

AP = Analog Power, AG = Analog Ground

DP = Digital Power, DG = Digital Ground

A = Analog

②: Output Drive strength is configurable, it's the suggested value in this table. Unit is mA, only Digital IO have drive value

③: Power supply means that all the related IOs are in this IO power domain. If multiple powers are included, they are connected together in one IO power ring

④: The pull up/pull down is configurable.

2.6 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 RK912 IO Function Description List

Interface	Pin Name	Direction	Description
MISC	RFPAD_XI	I	Clock input of 40MHz crystal
	RFPAD_XO	O	Clock output of 40MHz crystal
	NPOR	I	Chip hardware reset
	RTC_CLK32K	I	Chip sleep clock input
	DEVICE_IRQ	O	Chip interrupt output to host

Interface	Pin Name	Direction	Description
DEBUG	MOJTAG_TCK	I	JTAG interface tck signal for Cortex-M0
	MOJTAG_TMS	I/O	JTAG interface tms signal for Cortex-M0
	AONJTAG_TCK	I	JTAG interface tck signal for WiFi CPU
	AONJTAG_TMS	I	JTAG interface tms signal for WiFi CPU
	AONJTAG_TRSTN	I	JTAG interface trstn signal for WiFi CPU
	AONJTAG_TDI	I	JTAG interface tdi signal for WiFi CPU
	AONJTAG_TDO	O	JTAG interface tdo signal for WiFi CPU
	PMU_ST0	O	PMU state machine debug output signal
	PMU_ST1	O	PMU state machine debug output signal
	PMU_ST2	O	PMU state machine debug output signal
	PMU_ST3	O	PMU state machine debug output signal
	PMU_ST4	O	PMU state machine debug output signal
	M0_WFI	O	Cortex-M0 WFI indication debug signal

Interface	Pin Name	Direction	Description
SDIO	SDIO_CLK	I	sdio device clock.
	SDIO_CMD	I/O	sdio device command input and response output.
	SDIO_DATA <i>i</i> (<i>i</i> =0~3) (<i>x</i> =0,1)	I/O	sdio device data input and output.

Interface	Pin Name	Direction	Description
UART	UARTDBG_SOUT	O	uart serial data output.
	UARTDBG_SOUTB		

Interface	Pin Name	Direction	Description
BT Coexistence	BT_MBSY	I	BT coexistence signal
	BT_DENY	O	BT coexistence signal
	BT_CONFIRM	O	BT coexistence signal
	BT_RXNTX	I	BT coexistence signal

Interface	Pin Name	Direction	Description
	BT_PT10	I	BT coexistence signal

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RK912 Absolute Maximum Ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for internal digital logic	VDD	1.21	V
DC supply voltage for digital GPIO@3.3V mode	VDD3318_GPIO	3.60	V
DC supply voltage for digital GPIO@1.8V mode	VDD3318_GPIO	1.98	V
DC supply voltage for RF_VDD33	RF_VDD33	3.60	V
DC supply voltage for RF_VDD18	RF_VDD18_L0 RF_VDD18_L1 RF_VDD18_L2 RF_VDD18_T	1.98	V
DC supply voltage for IO_LDO_VDD_33V	IO_LDO_VDD_33V	3.60	V
Storage Temperature	Tstg	125	°C
Max Conjunction Temperature	Tj	125	°C

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

Following table describes the recommended operating condition.

Table 3-2 RK912 Recommended Operating Condition

Parameters	Symbol	Min	Type	Max	Unit
DC supply voltage for internal digital logic	VDD	0.99	1.10	1.21	V
DC supply voltage for digital GPIO@3.3V mode	VDD3318_GPIO	3.00	3.30	3.60	V
DC supply voltage for digital GPIO@1.8V mode	VDD3318_GPIO	1.62	1.80	1.98	V
DC supply voltage for RF_VDD33	RF_VDD33	3.00	3.30	3.60	V
DC supply voltage for RF_VDD18	RF_VDD18_L0 RF_VDD18_L1 RF_VDD18_L2 RF_VDD18_T	1.52	1.80	1.98	V
DC supply voltage for IO_LDO_VDD_33V	IO_LDO_VDD_33V	3.00	3.30	3.60	V
Operating Temperature		0	25	85	°C

3.3 DC Characteristics

Table 3-3 RK912 DC Characteristics

Parameters		Symbol	Min	Type	Max	Units
Digital GPIO @3.3V mode	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	3.6	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	NA	V
	Threshold Point	Vtr+	1.57	1.68	1.81	V
		Vtr-	1.21	1.32	1.45	V
	Pullup Resistor	Rpu	58	86	133	Kohm
Digital GPIO @1.8V mode	Pulldown Resistor	Rpd	52	78	128	Kohm
	Input Low Voltage	Vil	-0.3	NA	0.63	V
	Input High Voltage	Vih	1.17	NA	3.6	V
	Output Low Voltage	Vol	NA	NA	0.45	V
	Output High Voltage	Voh	1.35	NA	NA	V
	Threshold Point	Vtr+	0.93	1.02	1.11	V
		Vtr-	0.62	0.73	0.82	V
	Pullup Resistor	Rpu	117	194	331	Kohm
	Pulldown Resistor	Rpd	91	159	291	Kohm

Chapter 4 Power Consumption

Power consumption data refer to Table 4-1. Data is measured on 3.3V source power supply at 25C environment temperature with 99% tx/rx duty ration.

Table 4-1 RK912 Power Consumption Data

mode	Min	Type	Max	Units
TX 802.11b, DSSS 1Mbps, Pout = + 16dBm		~220		mA
TX 802.11b, CCK 11Mbps, Pout = + 16dBm		~220		mA
TX 802.11n, mcs0, Pout = + 16dBm		~220		mA
TX 802.11n, mcs7, Pout = + 9dBm		~190		mA
RX 802.11n, mcs7		~40		mA
Associated Idle		TBD		mA
Un-Associated Idle		TBD		mA

Chapter 5 RF Characteristic

RF Characteristic data refer to Table 5-1. Data is measured at 25C environment temperature.

Table 5-1 RK912 RF Characteristic Data

mode	Min	Type	Max	Units
Max Output Power		16		dBm
RX 802.11b, DSSS 1Mbps, Sensitivity		-94		dBm
RX 802.11b, CCK 11Mbps, Sensitivity		-83		dBm
RX 802.11g, 6Mbps, Sensitivity		-89		dBm
RX 802.11g, 54Mbps, Sensitivity		-72		dBm
RX 802.11n, mcs0, Sensitivity		-88		dBm
RX 802.11n, mcs7, Sensitivity		-67		dBm