

## RL78/G10

R01DS0207EJ0300

### RENESAS MCU

Rev.3.00

Nov 19, 2014

True Low Power Platform (as low as 46  $\mu$ A/MHz), 2.0 to 5.5V Operation,  
1 to 4 Kbyte Flash for General Purpose Applications

## 1. OUTLINE

### 1.1 Features

#### Ultra-Low Power Technology

- 2.0 to 5.5 V operation from a single supply
- Stop (RAM retained): 0.56  $\mu$ A
- Operating: 46  $\mu$ A /MHz

#### RL78-S1 Core

- Instruction execution: 78 % of instructions can be executed in 1 to 2 clock cycles
- CISC architecture (Harvard) with 3-stage pipeline
- Multiply: 8 x 8 to 16-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 2 clock cycle
- 1-wire on-chip debug function

#### Main Flash Memory

- Density: 1 to 4 Kbyte
- Flash memory rewritable voltage: 4.5 to 5.5 V

#### RAM

- 128 to 512 Byte size options
- Supports operands or instructions
- Back-up retention in all modes

#### High-speed On-chip Oscillator

- 20 MHz with +/- 2 % accuracy over voltage (2.0 to 5.5 V) and temperature (-20 to +85°C)
- Pre-configured settings: 20 MHz, 10 MHz, 5 MHz, 2.5 MHz, and 1.25 MHz

#### Reset and Supply Management

- Selectable power-on reset (SPOR) generator with 4 setting options

#### Multiple Communication Interfaces

- 1 x I<sup>2</sup>C master
- 1 x I<sup>2</sup>C multi-master (only for 16-pin product)
- 1 x UART (7-, 8-bit)
- Up to 2 x CSI/SPI (7-, 8-bit)

#### Extended-Function Timers

- Multi-function 16-bit timers: Up to 4 channels
- Interval timer: 12-bit, 1 channel (only for 16-pin product)
- 15 kHz watchdog timer : 1 channel

#### Rich Analog

- ADC: Up to 7 channels, 10-bit resolution, 3.4  $\mu$ s conversion time
- Supports 2.4 V
- Internal reference voltage (0.815 V (typ.))
- Comparator: 1 channel (only for 16-pin product)

#### Safety Features

- Detects execution of illegal instruction
- Detects watchdog timer program loop

#### General Purpose I/O

- High-current (up to 20 mA per pin)
- Open-drain, internal pull-up support

#### External Interrupt

- External interrupt input: Up to 4
- Key interrupt input: 6

#### Operating Ambient Temperature

- Standard: -40 to +85°C

#### Package Type and Pin Count

- SSOP: 10 and 16 pin

## ○ ROM, RAM capacities

| Flash ROM | RAM   | 10 pins  | 16 pins  |
|-----------|-------|----------|----------|
| 4 KB      | 512 B | R5F10Y17 | R5F10Y47 |
| 2 KB      | 256 B | R5F10Y16 | R5F10Y46 |
| 1 KB      | 128 B | R5F10Y14 | R5F10Y44 |

**Note** 16-pin products only

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G10

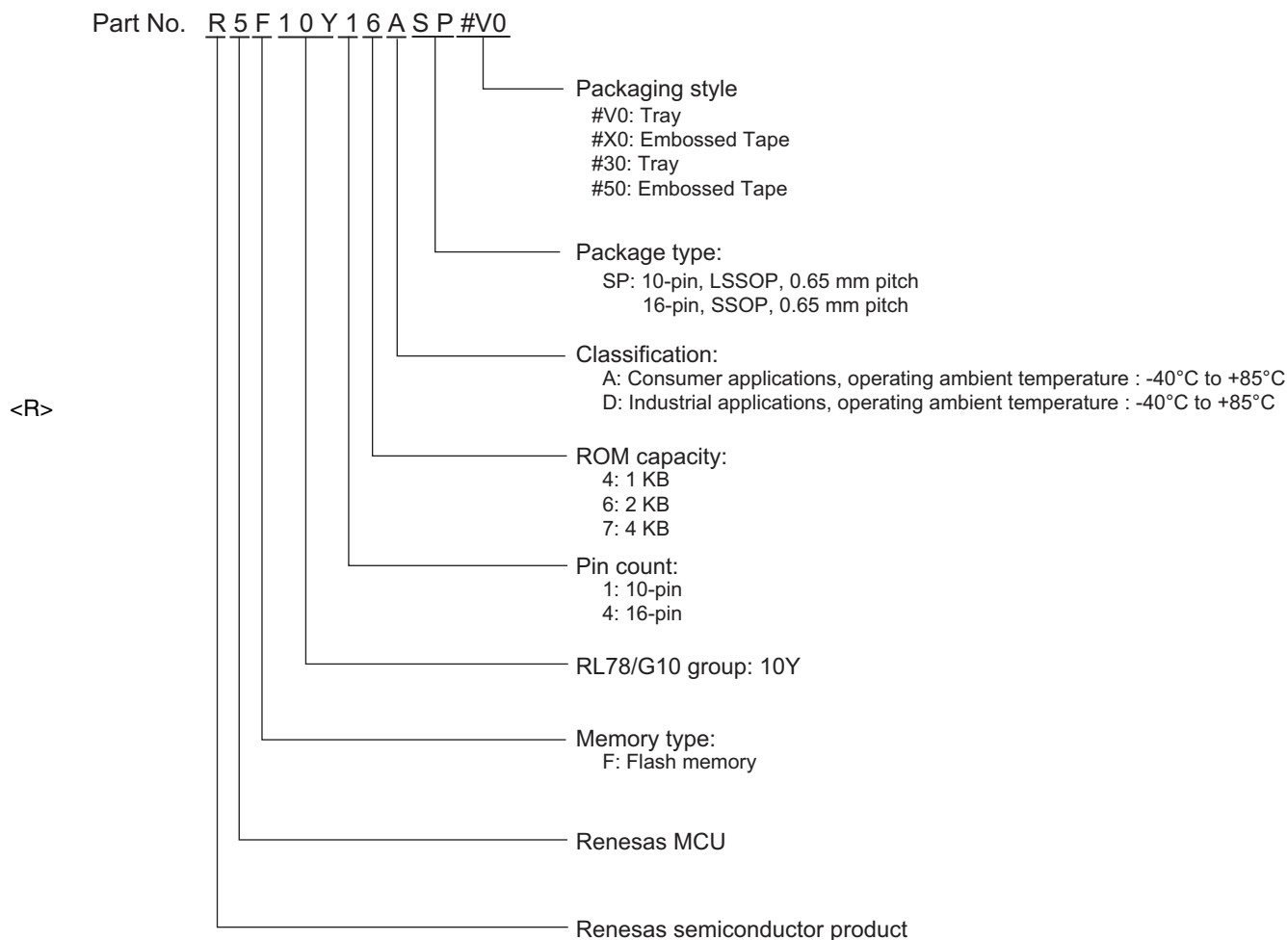


Table 1-1. List of Ordering Part Numbers

| Pin count | Package   | Fields of Application <sup>Note 1</sup> | Part Number  |
|-----------|---|---|--|
| 10 pins   | 10-pin plastic LSSOP<br>(4.4 × 3.6 mm, 0.65 mm pitch) | A                                       | R5F10Y17ASP#30, R5F10Y17ASP#50<br>R5F10Y16ASP#V0, R5F10Y16ASP#X0<br>R5F10Y14ASP#V0, R5F10Y14ASP#X0 |
|           |   | D <sup>Note 2</sup>                     | R5F10Y17DSP#30, R5F10Y17DSP#50<br>R5F10Y16DSP#V0, R5F10Y16DSP#X0<br>R5F10Y14DSP#V0, R5F10Y14DSP#X0 |
| 16 pins   | 16-pin plastic SSOP<br>(4.4 × 5.0 mm, 0.65 mm pitch)  | A                                       | R5F10Y47ASP#30, R5F10Y47ASP#50<br>R5F10Y46ASP#30, R5F10Y46ASP#50<br>R5F10Y44ASP#30, R5F10Y44ASP#50 |
|           |   | D <sup>Note 2</sup>                     | R5F10Y47DSP#30, R5F10Y47DSP#50<br>R5F10Y46DSP#30, R5F10Y46DSP#50<br>R5F10Y44DSP#30, R5F10Y44DSP#50 |

(Notes and Caution are listed on the next page.)

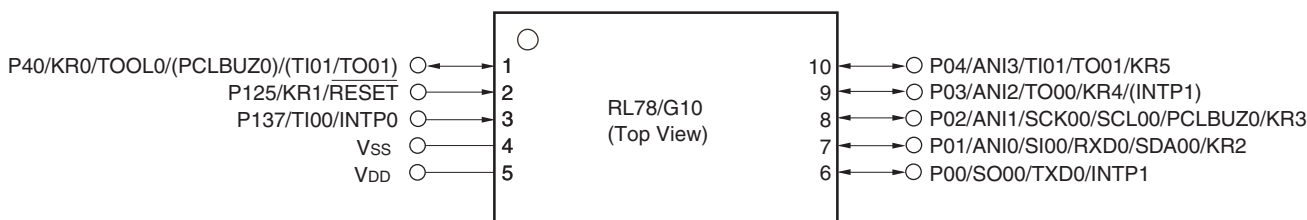
- Notes**
1. For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G10**.
  2. Under development

**Caution** The part number represents the number at the time of publication.  
 Be sure to review the latest part number through the target product page in the Renesas Electronics Corp. website.

### 1.3 Pin Configuration (Top View)

#### 1.3.1 10-pin products

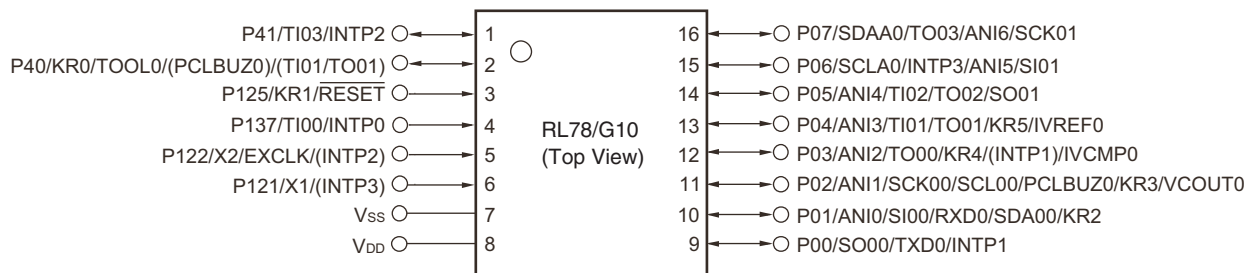
- <R> • 10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65 mm pitch)



- Remarks**
1. For pin identification, see **1.4 Pin Identification**.
  2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-6 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G10 User's Manual.

#### 1.3.2 16-pin products

- <R> • 16-pin plastic SSOP (4.4 × 5.0 mm, 0.65 mm pitch)



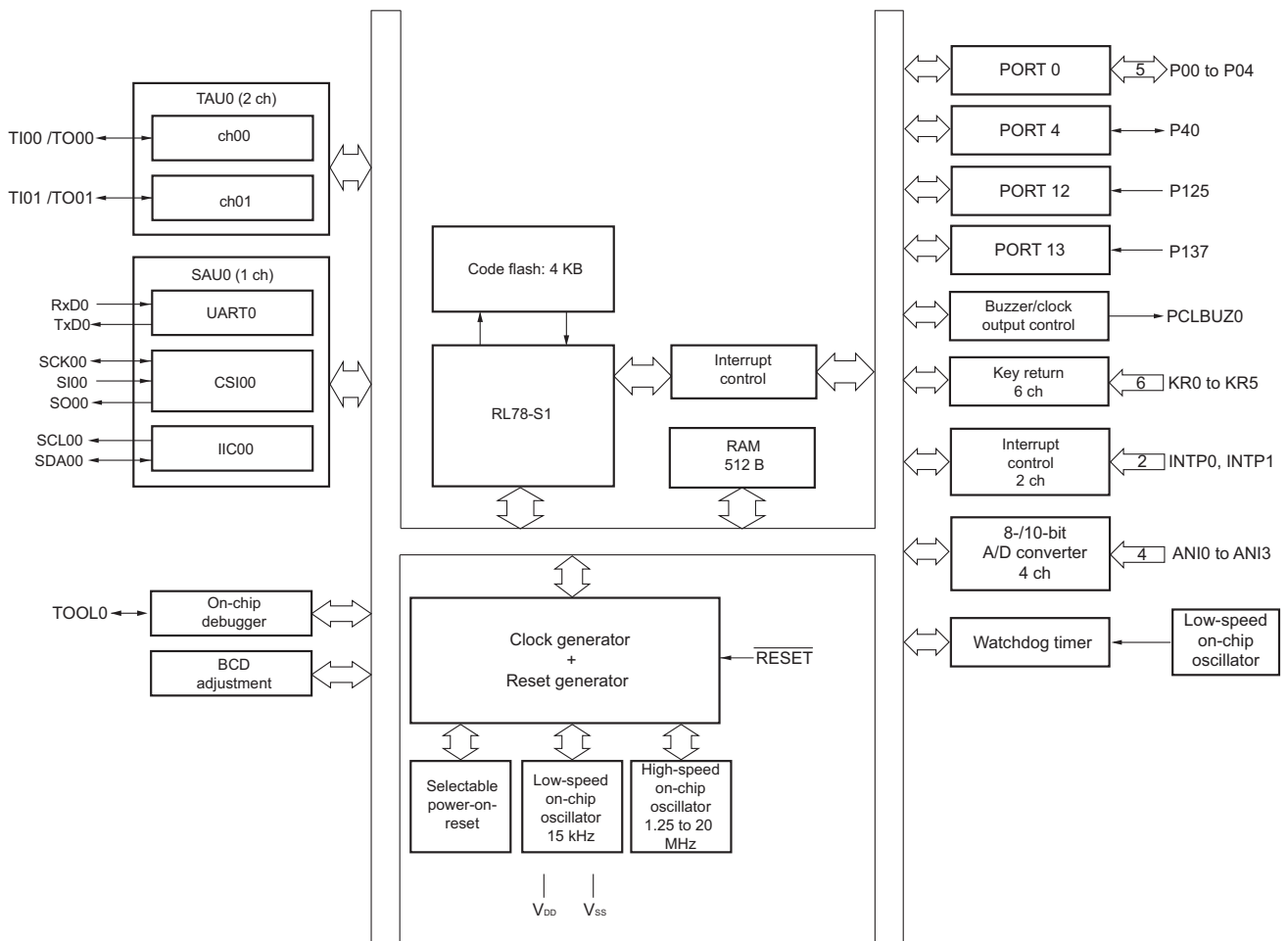
- Remarks**
1. For pin identification, see **1.4 Pin Identification**.
  2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-6 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G10 User's Manual.

## 1.4 Pin Identification

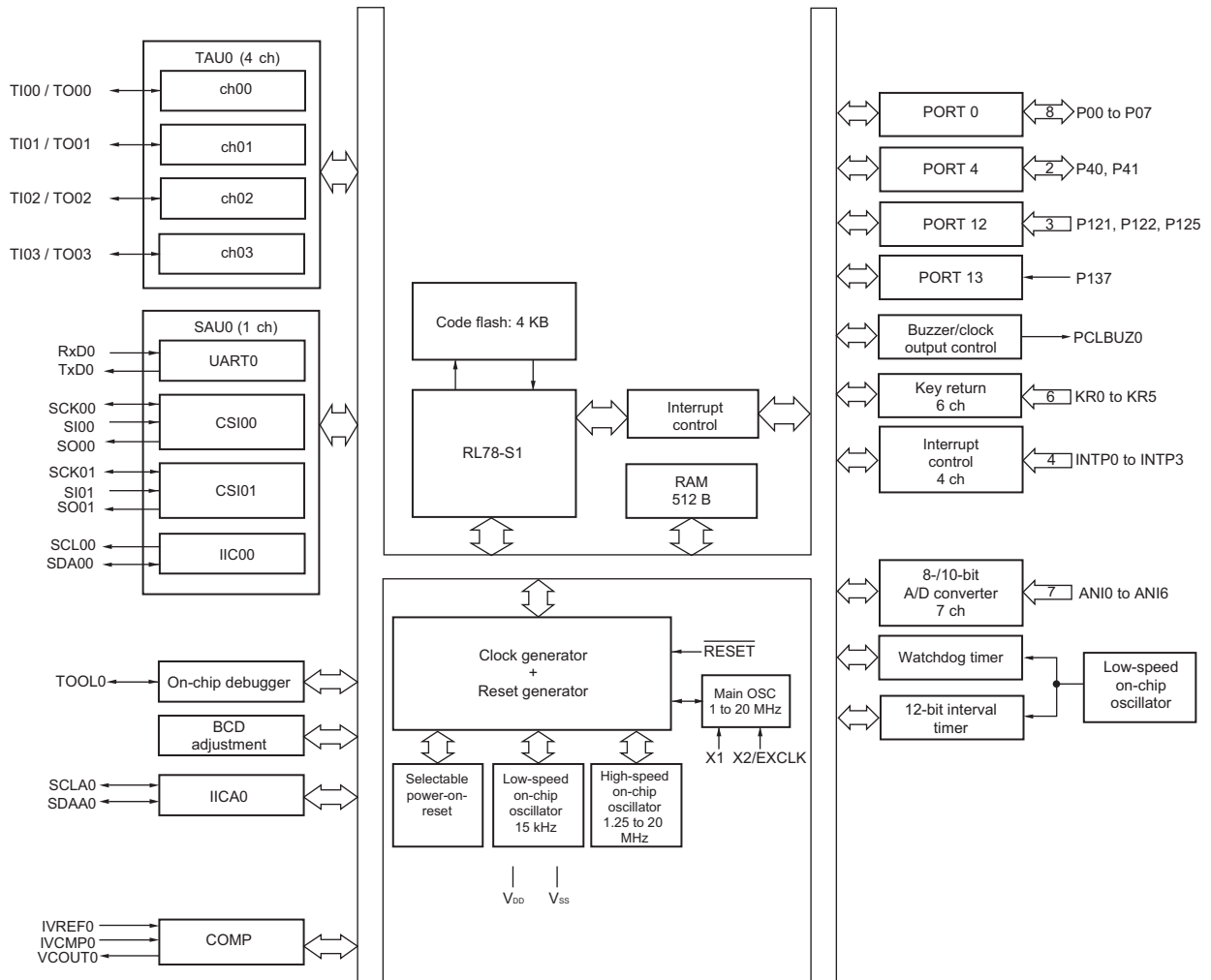
|                           |  |
|---------------------------|--|
| ANI0 to ANI6              | : Analog Input                             |
| INTP0 to INTP3            | : Interrupt Request From Peripheral        |
| KR0 to KR5                | : Key Return                               |
| P00 to P07                | : Port 0                                   |
| P40, P41                  | : Port 4                                   |
| P121, P122, P125          | : Port 12                                  |
| P137                      | : Port 13                                  |
| PCLBUZ0                   | : Programmable Clock Output/ Buzzer Output |
| EXCLK                     | : External Clock Input                     |
| X1, X2                    | : Crystal Oscillator (Main System Clock)   |
| IVCMP0                    | : Comparator Input                         |
| VCOUT0                    | : Comparator Output                        |
| IVREF0                    | : Comparator Reference Input               |
| $\overline{\text{RESET}}$ | : Reset                                    |
| RxD0                      | : Receive Data                             |
| SCK00, SCK01              | : Serial Clock Input/Output                |
| SCL00, SCLA0              | : Serial Clock Output                      |
| SDA00, SDAA0              | : Serial Data Input/Output                 |
| SI00, SI01                | : Serial Data Input                        |
| SO00, SO01                | : Serial Data Output                       |
| TI00 to TI03              | : Timer Input                              |
| TO00 to TO03              | : Timer Output                             |
| TOOL0                     | : Data Input/Output for Tool               |
| TxD0                      | : Transmit Data                            |
| V <sub>DD</sub>           | : Power Supply                             |
| V <sub>SS</sub>           | : Ground                                   |

### 1.5 Block Diagram

#### 1.5.1 10-pin products



1.5.2 16-pin products



## 1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

| Item                               |                                     | 10-pin   |          |          | 16-pin   |           |          |
|------------------------------------|-------------------------------------|--|----------|----------|--|-----------|----------|
|                                    |                                     | R5F10Y14   | R5F10Y16 | R5F10Y17 | R5F10Y44   | R5F10Y46  | R5F10Y47 |
| Code flash memory                  |                                     | 1 KB   | 2 KB     | 4 KB     | 1 KB   | 2 KB      | 4 KB     |
| RAM                                |                                     | 128 B  | 256 B    | 512 B    | 128 B  | 256 B     | 512 B    |
| Main system clock                  | High-speed system clock             | —  |          |          | X1, X2 (crystal/ceramic) oscillation, external main system clock input (EXCLK):<br>1 to 20 MHz: $V_{DD} = 2.7$ to $5.5$ V<br>1 to 5 MHz: $V_{DD} = 2.0$ to $5.5$ V <sup>Note 3</sup> |           |          |
|                                    | High-speed on-chip oscillator clock | <ul style="list-style-type: none"> <li>1.25 to 20 MHz (<math>V_{DD} = 2.7</math> to <math>5.5</math> V)</li> <li>1.25 to 5 MHz (<math>V_{DD} = 2.0</math> to <math>5.5</math> V <sup>Note 3</sup>)</li> </ul>  |          |          |  |           |          |
| Low-speed on-chip oscillator clock |                                     | 15 kHz (TYP)   |          |          |  |           |          |
| General-purpose register           |                                     | 8-bit register × 8   |          |          |  |           |          |
| Minimum instruction execution time |                                     | 0.05 μs (20 MHz operation)   |          |          |  |           |          |
| Instruction set                    |                                     | <ul style="list-style-type: none"> <li>Data transfer (8 bits)</li> <li>Adder and subtractor/logical operation (8 bits)</li> <li>Multiplication (8 bits × 8 bits)</li> <li>Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.</li> </ul>                              |          |          |  |           |          |
| I/O port                           | Total                               | 8  |          |          | 14   |           |          |
|                                    | CMOS I/O                            | 6 (N-ch open-drain output ( $V_{DD}$ tolerance): 2)  |          |          | 10 (N-ch open-drain output ( $V_{DD}$ tolerance): 4)   |           |          |
|                                    | CMOS input                          | 2  |          |          | 4  |           |          |
| Timer                              | 16-bit timer                        | 2 channels   |          |          | 4 channels   |           |          |
|                                    | Watchdog timer                      | 1 channel  |          |          |  |           |          |
|                                    | 12-bit interval timer               | —  |          |          | 1 channel  |           |          |
|                                    | Timer output                        | 2 channels (PWM output: 1)   |          |          | 4 channels (PWM outputs: 3 <sup>Note 1</sup> )   |           |          |
| Clock output/buzzer output         |                                     | 1  |          |          |  |           |          |
|                                    |                                     | 2.44 kHz to 10 MHz: (Peripheral hardware clock: $f_{MAIN} = 20$ MHz operation)   |          |          |  |           |          |
| Comparator                         |                                     | —  |          |          | 1  |           |          |
| 8-/10-bit resolution A/D converter |                                     | 4 channels   |          |          | 7 channels   |           |          |
| Serial interface                   |                                     | [10-pin products] CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel  |          |          | [16-pin products] CSI: 2 channels/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel   |           |          |
|                                    |                                     | I <sup>2</sup> C bus   | —        |          |  | 1 channel |          |
| Vectored interrupt sources         | Internal                            | 8  |          |          | 14   |           |          |
|                                    | External                            | 3  |          |          | 5  |           |          |
| Key interrupt                      |                                     | 6  |          |          |  |           |          |
| Reset                              |                                     | <ul style="list-style-type: none"> <li>Reset by RESET pin</li> <li>Internal reset by watchdog timer</li> <li>Internal reset by selectable power-on-reset</li> <li>Internal reset by illegal instruction execution <sup>Note 2</sup></li> <li>Internal reset by data retention lower limit voltage</li> </ul> |          |          |  |           |          |
| Selectable power-on-reset circuit  |                                     | <ul style="list-style-type: none"> <li>Detection voltage</li> <li>Rising edge (<math>V_{SPOR}</math>): 2.25 V/2.68 V/3.02 V/4.45 V (max.)</li> <li>Falling edge (<math>V_{SPDR}</math>): 2.20 V/2.62 V/2.96 V/4.37 V (max.)</li> </ul>   |          |          |  |           |          |



| Item                          | 10-pin   |          |          | 16-pin   |          |          |
|-------------------------------|--|----------|----------|----------|----------|----------|
|                               | R5F10Y14   | R5F10Y16 | R5F10Y17 | R5F10Y44 | R5F10Y46 | R5F10Y47 |
| On-chip debug function        | Provided   |          |          |          |          |          |
| Power supply voltage          | $V_{DD} = 2.0 \text{ to } 5.5 \text{ V}$ <sup>Note 3</sup> |          |          |          |          |          |
| Operating ambient temperature | $T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$         |          |          |          |          |          |

- Notes**
1. The number of outputs varies, depending on the setting of channels in use and the number of the master (see **6.9.4 Operation as multiple PWM output function** in the RL78/G10 User's Manual).
  2. The illegal instruction is generated when instruction code FFH is executed. Reset by the illegal instruction execution not issued by emulation with the on-chip debug emulator.
  3. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage ( $V_{SPOR}$ ) of the selectable power-on-reset (SPOR) circuit should also be considered.

## 2. ELECTRICAL SPECIFICATIONS

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  2. The pins mounted depend on the product. Refer to 2.1 Port Functions and 2.2.1 Functions for each product in the RL78/G10 User's Manual.
  3. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage ( $V_{SPOR}$ ) of the selectable power-on-reset (SPOR) circuit should also be considered.

## 2.1 Absolute Maximum Ratings

( $T_A = 25^\circ\text{C}$ )

| Parameter                     | Symbols   | Conditions        | Ratings                                | Unit             |    |
|-------------------------------|-----------|-------------------|--|------------------|----|
| Supply Voltage                | $V_{DD}$  |                   | -0.5 to +6.5                           | V                |    |
| Input Voltage                 | $V_{I1}$  |                   | -0.3 to $V_{DD} + 0.3$ <sup>Note</sup> | V                |    |
| Output Voltage                | $V_{O1}$  |                   | -0.3 to $V_{DD} + 0.3$                 | V                |    |
| Output current, high          | $I_{OH1}$ | Per pin           | -40                                    | mA               |    |
|                               |           | Total of all pins | P40, P41                               | -70              | mA |
|                               |           |                   | P00 to P07                             | -100             | mA |
| Output current, low           | $I_{OL1}$ | Per pin           | 40                                     | mA               |    |
|                               |           | Total of all pins | P40, P41                               | 70               | mA |
|                               |           |                   | P00 to P07                             | 100              | mA |
| Operating ambient temperature | $T_A$     |                   | -40 to +85                             | $^\circ\text{C}$ |    |
| Storage temperature           | $T_{stg}$ |                   | -65 to +150                            | $^\circ\text{C}$ |    |

**Note** Must be 6.5 V or lower.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks**

1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2. The reference voltage is  $V_{SS}$ .

## 2.2 Oscillator Characteristics

### 2.2.1 X1 oscillator characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter   | Resonator                               | Conditions                                   | MIN. | TYP. | MAX. | Unit |
|---|---|--|------|------|------|------|
| X1 clock oscillation frequency (fx) <sup>Note</sup> | Ceramic resonator/<br>crystal resonator | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1    |      | 20   | MHz  |
|   |   | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$    | 1    |      | 5    | MHz  |

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator, refer to 5.4 System Clock Oscillator in the RL78/G10 User's Manual.

### 2.2.2 On-chip oscillator characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Oscillators   | Parameters | Conditions                         | MIN. | TYP. | MAX. | Unit |
|---|------------|------------------------------------|------|------|------|------|
| High-speed on-chip oscillator oscillation clock frequency <sup>Notes 1, 2</sup> | $f_{IH}$   |                                    | 1.25 |      | 20   | MHz  |
| High-speed on-chip oscillator oscillation clock frequency accuracy              |            | $T_A = -20$ to $+85^\circ\text{C}$ | -2.0 |      | +2.0 | %    |
|   |            | $T_A = -40$ to $-20^\circ\text{C}$ | -3.0 |      | +3.0 | %    |
| Low-speed on-chip oscillator oscillation clock frequency                        | $f_{IL}$   |                                    |      | 15   |      | kHz  |
| Low-speed on-chip oscillator oscillation clock frequency accuracy               |            |                                    | -15  |      | +15  | %    |

- Notes**
- High-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (000C2H).
  - This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

(1/2)

| Parameter                      | Symbol           | Conditions   | MIN.   | TYP. | MAX.            | Unit  |
|--------------------------------|------------------|--|--|------|-----------------|-------|
| Output current, high<br>Note 1 | I <sub>OH1</sub> | Per pin for<br>10-pin products: P00 to P04, P40<br>16-pin products: P00 to P07, P40, P41                 |  |      | -10.0<br>Note 2 | mA    |
|                                |                  | Total of<br>10-pin products: P40<br>16-pin products: P40, P41<br>(When duty $\leq 70\%$ Note 3)          | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |      | -20.0           | mA    |
|                                |                  |  | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$    |      | -4.0            | mA    |
|                                |                  | Total of<br>10-pin products: P00 to P04<br>16-pin products: P00 to P07<br>(When duty $\leq 70\%$ Note 3) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |      | -60.0           | mA    |
|                                |                  |  | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$    |      | -12.0           | mA    |
|                                |                  |  | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$    |      | -9.0            | mA    |
|                                |                  | Total of all pins (When duty $\leq 70\%$ Note 3)   |  |      |                 | -80.0 |
| Output current, low<br>Note 4  | I <sub>OL1</sub> | Per pin for<br>10-pin products: P00 to P04, P40<br>16-pin products: P00 to P07, P40, P41                 |  |      | 20.0<br>Note 2  | mA    |
|                                |                  | Total of<br>10-pin products: P40<br>16-pin products: P40, P41<br>(When duty $\leq 70\%$ Note 3)          | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |      | 40.0            | mA    |
|                                |                  |  | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$    |      | 6.0             | mA    |
|                                |                  | Total of<br>10-pin products: P00 to P04<br>16-pin products: P00 to P07<br>(When duty $\leq 70\%$ Note 3) | $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |      | 80.0            | mA    |
|                                |                  |  | $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$    |      | 12.0            | mA    |
|                                |                  |  | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$    |      | 2.4             | mA    |
|                                |                  | Total of all pins (When duty $\leq 70\%$ Note 3)   |  |      |                 | 120.0 |

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from the  $V_{DD}$  pin to an output pin.

2. Do not exceed the total current value.

3. This is the output current value under conditions where the duty factor  $\leq 70\%$ .

The output current value when the duty factor  $> 70\%$  can be calculated with the following expression (when changing the duty factor to  $n\%$ ).

- Total output current of pins =  $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 80\%$  and  $I_{OH} = -10.0\text{ mA}$

Total output current of pins =  $(-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$

- Total output current of pins =  $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 80\%$  and  $I_{OL} = 10.0\text{ mA}$

Total output current of pins =  $(10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the  $V_{SS}$  pin.

**Caution** P00, P01, P06, and P07 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

(TA = -40 to +85°C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Parameter                      | Symbol            | Conditions   |                                       | MIN.                  | TYP. | MAX.                | Unit |
|--------------------------------|-------------------|--|---------------------------------------|-----------------------|------|---------------------|------|
| Input voltage, high            | V <sub>IH1</sub>  |  |                                       | 0.8 V <sub>DD</sub>   |      | V <sub>DD</sub>     | V    |
| Input voltage, low             | V <sub>IL1</sub>  |  |                                       | 0                     |      | 0.2 V <sub>DD</sub> | V    |
| Output voltage, high<br>Note 1 | V <sub>OH1</sub>  | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V                                      | I <sub>OH</sub> = -10 mA              | V <sub>DD</sub> - 1.5 |      |                     | V    |
|                                |                   |  | I <sub>OH</sub> = -3.0 mA             | V <sub>DD</sub> - 0.7 |      |                     | V    |
|                                |                   | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V                                      | I <sub>OH</sub> = -2.0 mA             | V <sub>DD</sub> - 0.6 |      |                     | V    |
|                                |                   | 2.0 V ≤ V <sub>DD</sub> ≤ 5.5 V                                      | I <sub>OH</sub> = -1.5 mA             | V <sub>DD</sub> - 0.5 |      |                     | V    |
| Output voltage, low<br>Note 2  | V <sub>OL1</sub>  | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V                                      | I <sub>OL</sub> = 20 mA               |                       |      | 1.3                 | V    |
|                                |                   |  | I <sub>OL</sub> = 8.5 mA              |                       |      | 0.7                 | V    |
|                                |                   | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V                                      | I <sub>OL</sub> = 3.0 mA              |                       |      | 0.6                 | V    |
|                                |                   |  | I <sub>OL</sub> = 1.5 mA              |                       |      | 0.4                 | V    |
|                                |                   | 2.0 V ≤ V <sub>DD</sub> ≤ 5.5 V                                      | I <sub>OL</sub> = 0.6 mA              |                       |      | 0.4                 | V    |
| Input leakage current, high    | I <sub>LIH1</sub> | P00 to P07, P40, P41, P125, P137<br>V <sub>i</sub> = V <sub>DD</sub> |                                       |                       |      | 1                   | μA   |
|                                | I <sub>LIH2</sub> | P121, P122 (X1, X2, EXCLK)<br>V <sub>i</sub> = V <sub>DD</sub>       | In input port or external clock input |                       |      | 1                   |      |
|                                |                   |  | In resonator connection               |                       |      | 10                  |      |
| Input leakage current, low     | I <sub>LIL1</sub> | P00 to P07, P40, P41, P125, P137<br>V <sub>i</sub> = V <sub>SS</sub> |                                       |                       |      | -1                  | μA   |
|                                | I <sub>LIL2</sub> | P121, P122 (X1, X2, EXCLK)<br>V <sub>i</sub> = V <sub>SS</sub>       | In input port or external clock input |                       |      | -1                  |      |
|                                |                   |  | In resonator connection               |                       |      | -10                 |      |
| On-chip pull-up resistance     | R <sub>U</sub>    | V <sub>i</sub> = V <sub>SS</sub>                                     |                                       | 10                    | 20   | 100                 | kΩ   |

**Notes** 1. The value under the condition which satisfies the high-level output current (I<sub>OH1</sub>).

2. The value under the condition which satisfies the low-level output current (I<sub>OL1</sub>).

**Caution** The maximum value of V<sub>IH</sub> of P00, P01, P06, and P07 is V<sub>DD</sub> even in N-ch open-drain mode. P00, P01, P06, and P07 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

## 2.3.2 Supply current characteristics

## (1) Flash ROM: 1 and 2 KB of 10-pin products

(TA = -40 to +85°C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter                | Symbol                 | Conditions              |                         |                                |                                | MIN. | TYP. | MAX. | Unit |
|--------------------------|------------------------|-------------------------|-------------------------|--------------------------------|--------------------------------|------|------|------|------|
| Supply current<br>Note 1 | IDD1                   | Operating mode          | Basic operation         | f <sub>IH</sub> = 20 MHz       | V <sub>DD</sub> = 3.0 V, 5.0 V |      | 0.91 |      | mA   |
|                          |                        |                         | Normal operation        | f <sub>IH</sub> = 20 MHz       | V <sub>DD</sub> = 3.0 V, 5.0 V |      | 1.57 | 2.04 |      |
|                          |                        | f <sub>IH</sub> = 5 MHz |                         | V <sub>DD</sub> = 3.0 V, 5.0 V |                                | 0.85 | 1.15 |      |      |
|                          | IDD2 <sup>Note 2</sup> | HALT mode               |                         | f <sub>IH</sub> = 20 MHz       | V <sub>DD</sub> = 3.0 V, 5.0 V |      | 350  | 820  | μA   |
|                          |                        |                         |                         | f <sub>IH</sub> = 5 MHz        | V <sub>DD</sub> = 3.0 V, 5.0 V |      | 290  | 600  |      |
| IDD3 <sup>Note 3</sup>   | STOP mode              |                         | V <sub>DD</sub> = 3.0 V |                                |                                | 0.56 | 2.00 | μA   |      |

- Notes**
- Total current flowing into V<sub>DD</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub> or V<sub>SS</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, I/O port, and on-chip pull-up/pull-down resistors.
  - During HALT instruction execution by flash memory.
  - Not including the current flowing into the watchdog timer.

- Remarks**
- f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  - Temperature condition of the typical value is T<sub>A</sub> = 25°C

## (2) Flash ROM: 4 KB of 10-pin products, and 16-pin products

(T<sub>A</sub> = -40 to +85°C, 2.0 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

| Parameter  | Symbol                             | Conditions              |   | MIN.   | TYP.                           | MAX. | Unit |      |    |
|--|------------------------------------|-------------------------|---|--|--------------------------------|------|------|------|----|
| Supply current <sup>Note 1</sup>                 | I <sub>DD1</sub>                   | Operating mode          | Basic operation                                   | f <sub>IH</sub> = 20 MHz<br><sup>Note 4</sup>    | V <sub>DD</sub> = 3.0 V, 5.0 V |      | 0.92 |      | mA |
|  |                                    |                         | Normal operation                                  | f <sub>IH</sub> = 20 MHz<br><sup>Note 4</sup>    | V <sub>DD</sub> = 3.0 V, 5.0 V |      | 1.59 | 2.14 |    |
|  |                                    |                         |   | f <sub>IH</sub> = 5 MHz<br><sup>Note 4</sup>     | V <sub>DD</sub> = 3.0 V, 5.0 V |      | 0.87 | 1.20 |    |
|  |                                    |                         | f <sub>MX</sub> = 20 MHz<br><sup>Notes 5, 6</sup> | Square wave input                                |                                | 1.43 | 1.93 |      |    |
|  |                                    |                         |   | Resonator connection                             |                                | 1.54 | 2.13 |      |    |
|  |                                    |                         |   | f <sub>MX</sub> = 5 MHz<br><sup>Notes 5, 6</sup> | Square wave input              |      | 0.67 | 1.02 |    |
|  | Resonator connection               |                         | 0.72  |  | 1.12                           |      |      |      |    |
|  | I <sub>DD2</sub> <sup>Note 2</sup> | HALT mode               | f <sub>IH</sub> = 20 MHz<br><sup>Note 4</sup>     | V <sub>DD</sub> = 3.0 V, 5.0 V                   |                                | 360  | 900  | μA   |    |
|  |                                    |                         | f <sub>IH</sub> = 5 MHz<br><sup>Note 4</sup>      | V <sub>DD</sub> = 3.0 V, 5.0 V                   |                                | 310  | 660  |      |    |
|  |                                    |                         | f <sub>MX</sub> = 20 MHz<br><sup>Notes 5, 6</sup> | Square wave input                                |                                | 200  | 700  |      |    |
|  |                                    |                         |   | Resonator connection                             |                                | 300  | 900  |      |    |
| f <sub>MX</sub> = 5 MHz<br><sup>Notes 5, 6</sup> |                                    |                         | Square wave input                                 |  | 100                            | 440  |      |      |    |
|  | Resonator connection               |                         | 150   | 540  |                                |      |      |      |    |
| I <sub>DD3</sub> <sup>Note 3</sup>               | STOP mode                          | V <sub>DD</sub> = 3.0 V |   |  | 0.61                           | 2.25 | μA   |      |    |

**Notes 1.** Total current flowing into V<sub>DD</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub> or V<sub>SS</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator (16-pin products only), I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.
3. Not including the current flowing into the 12-bit interval timer and watchdog timer.
4. When the high-speed system clock is stopped.
5. When the high-speed on-chip oscillator is stopped.
6. 16-pin products only

**Remarks**

1. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
2. f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillator frequency or external main system clock frequency)
3. Temperature condition of the typical value is T<sub>A</sub> = 25°C



**(3) Peripheral Functions (Common to all products)****( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

| Parameter                                      | Symbol                       | Conditions                       |                         | MIN. | TYP. | MAX. | Unit          |
|--|------------------------------|----------------------------------|-------------------------|------|------|------|---------------|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ <sup>Note 1</sup>  |                                  |                         |      | 0.30 |      | $\mu\text{A}$ |
| 12-bit interval timer operating current        | $I_{TMKA}$<br>Notes 1, 2, 3  |                                  |                         |      | 0.01 |      | $\mu\text{A}$ |
| Watchdog timer operating current               | $I_{WDT}$<br>Notes 1, 4      |                                  |                         |      | 0.01 |      | $\mu\text{A}$ |
| A/D converter operating current                | $I_{ADC}$<br>Notes 1, 5      | When conversion at maximum speed | $V_{DD} = 5.0\text{ V}$ |      | 1.30 | 1.90 | $\text{mA}$   |
|  |                              |                                  | $V_{DD} = 3.0\text{ V}$ |      | 0.50 |      | $\text{mA}$   |
| Comparator operating current                   | $I_{CMP}$<br>Notes 1, 6      | In high-speed mode               | $V_{DD} = 5.0\text{ V}$ |      | 6.50 |      | $\mu\text{A}$ |
|  |                              | In low-speed mode                | $V_{DD} = 5.0\text{ V}$ |      | 1.70 |      | $\mu\text{A}$ |
| Internal reference voltage operating current   | $I_{VREG}$ <sup>Note 1</sup> |                                  |                         |      | 10   |      | $\mu\text{A}$ |

**Notes** 1. Current flowing to  $V_{DD}$ .

2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{FIL}$  and  $I_{TMKA}$ , when the 12-bit interval timer is in operation.
4. Current flowing only to the watchdog timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{FIL}$  and  $I_{WDT}$  when the watchdog timer is in operation.
5. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$  or  $I_{DD2}$  and  $I_{ADC}$  when the A/D converter operates in an operation mode or the HALT mode.
6. Current flowing only to the comparator. The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{CMP}$  when the comparator is in operation.

- Remarks**
1.  $f_{IL}$ : Low-speed on-chip oscillator clock frequency
  2. Temperature condition of the typical value is  $T_A = 25^\circ\text{C}$

## 2.4 AC Characteristics

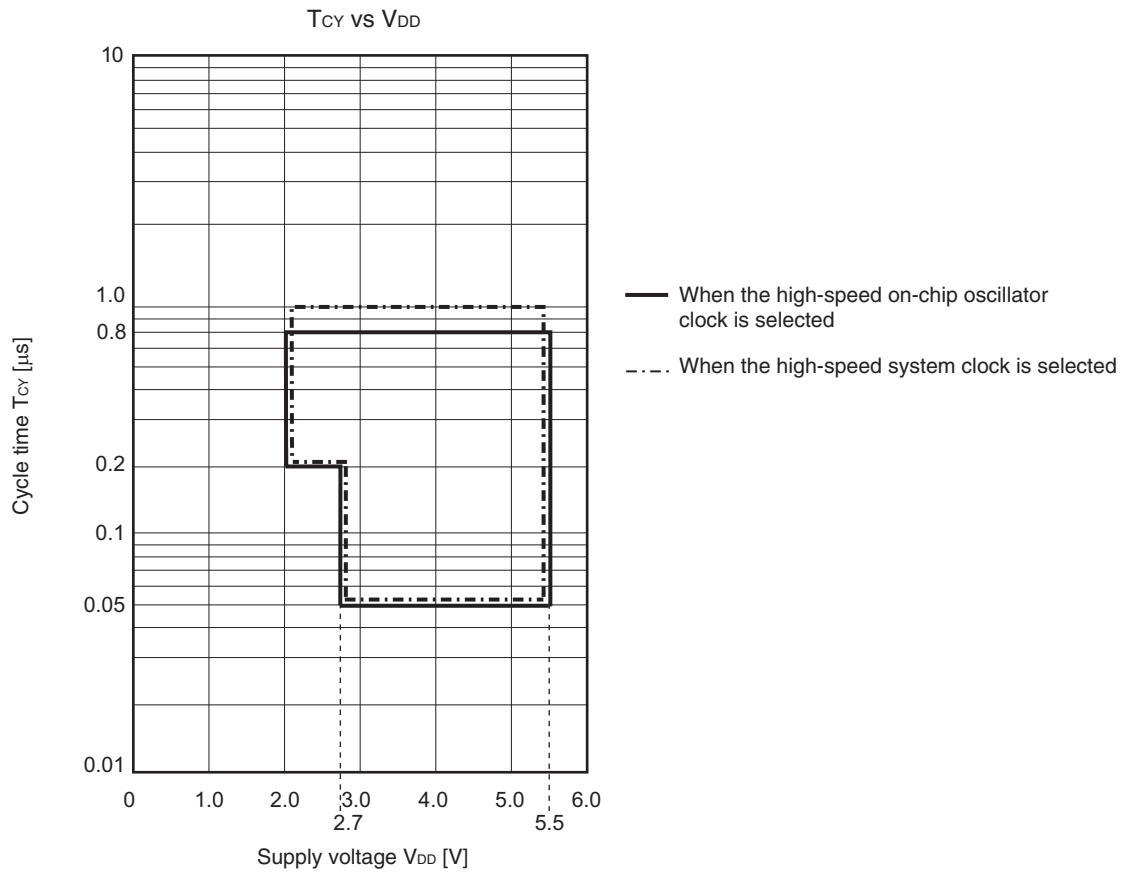
(T<sub>A</sub> = -40 to +85°C, 2.0 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

| Items   | Symbol                              | Conditions  | MIN.                            | TYP. | MAX. | Unit |
|---|-------------------------------------|---|---------------------------------|------|------|------|
| Instruction cycle (minimum instruction execution time)        | T <sub>CY</sub>                     | When high-speed on-chip oscillator clock (f <sub>IH</sub> ) is selected | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V | 0.05 | 0.8  | μs   |
|   |                                     |   | 2.0 V ≤ V <sub>DD</sub> < 2.7 V | 0.2  | 0.8  | μs   |
|   |                                     | When high-speed system clock (f <sub>MX</sub> ) is selected             | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V | 0.05 | 1.0  | μs   |
|   |                                     |   | 2.0 V ≤ V <sub>DD</sub> < 2.7 V | 0.2  | 1.0  | μs   |
| External system clock frequency                               | T <sub>EX</sub>                     | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V   | 1.0                             |      | 20   | MHz  |
|   |                                     | 2.0 V ≤ V <sub>DD</sub> < 2.7 V   | 1.0                             |      | 5    | MHz  |
| External system clock input high-level width, low-level width | T <sub>EXH</sub> , T <sub>EXL</sub> | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V   | 24                              |      |      | ns   |
|   |                                     | 2.0 V ≤ V <sub>DD</sub> < 2.7 V   | 95                              |      |      | ns   |
| TI00 to TI03 input high-level width, low-level width          | t <sub>TIH</sub> , t <sub>TIL</sub> | Noise filter is not used  | 1/f <sub>MCK</sub> + 10         |      |      | ns   |
| TO00 to TO03 output frequency                                 | f <sub>TO</sub>                     | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V   |                                 |      | 10   | MHz  |
|   |                                     | 2.7 V ≤ V <sub>DD</sub> < 4.0 V   |                                 |      | 5    | MHz  |
|   |                                     | 2.0 V ≤ V <sub>DD</sub> < 2.7 V   |                                 |      | 2.5  | MHz  |
| PCLBUZ0 output frequency                                      | f <sub>PCL</sub>                    | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V   |                                 |      | 10   | MHz  |
|   |                                     | 2.7 V ≤ V <sub>DD</sub> < 4.0 V   |                                 |      | 5    | MHz  |
|   |                                     | 2.0 V ≤ V <sub>DD</sub> < 2.7 V   |                                 |      | 2.5  | MHz  |
| $\overline{\text{RESET}}$ low-level width                     | t <sub>RSL</sub>                    |   | 10                              |      |      | μs   |

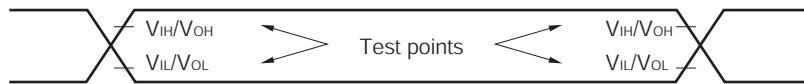
**Remark** f<sub>MCK</sub>: Timer array unit operation clock frequency

(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n1 bit of timer mode register 0nH (TMR0nH). n: Channel number (n = 0 to 3))

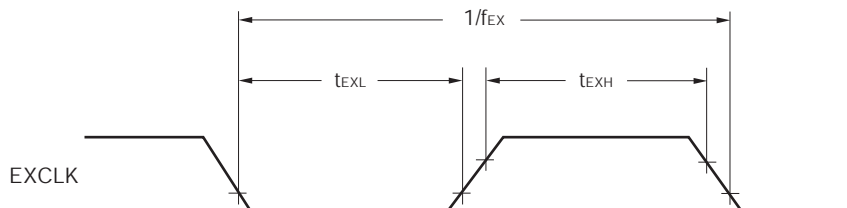
**Minimum Instruction Execution Time during Main System Clock Operation**

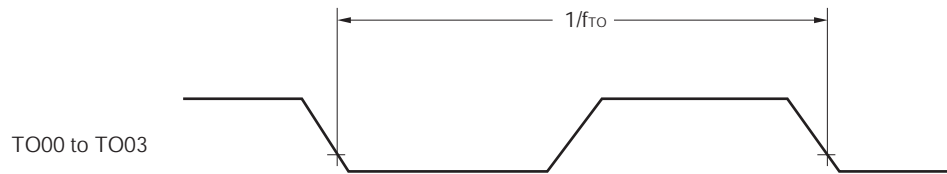
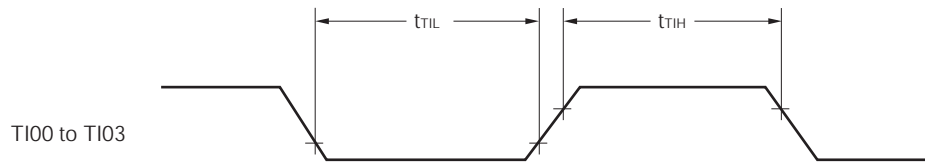
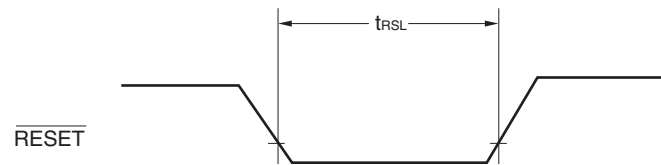


**AC Timing Test Points**



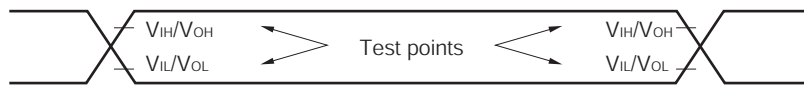
**External System Clock Timing**



**TI/TO Timing****RESET Input Timing**

2.5 Serial Interface Characteristics

AC Timing Test Points



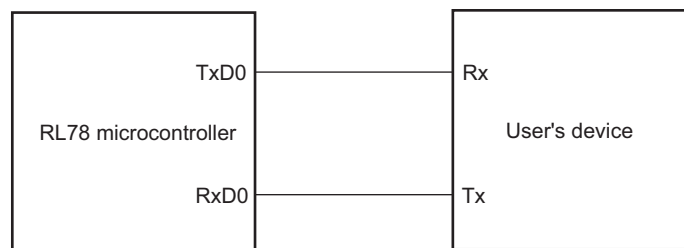
2.5.1 Serial array unit

(1) UART mode

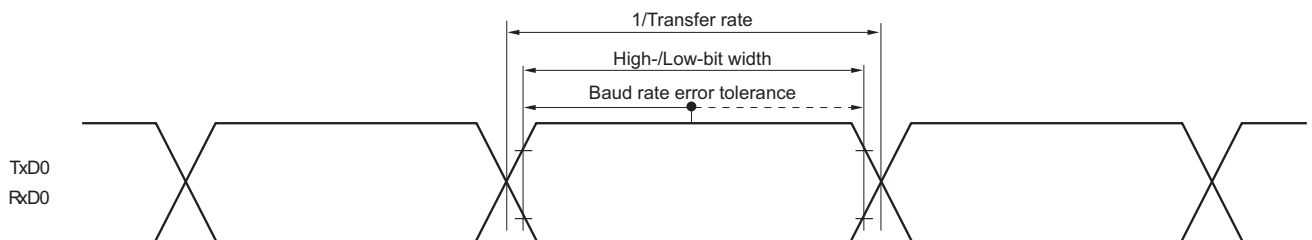
(T<sub>A</sub> = -40 to +85°C, 2.0 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

| Parameter     | Symbol | Conditions   | MIN. | TYP. | MAX.                | Unit |
|---------------|--------|--|------|------|---------------------|------|
| Transfer rate |        |  |      |      | f <sub>mck</sub> /6 | bps  |
|               |        | Theoretical value of the maximum transfer rate<br>f <sub>CLK</sub> = f <sub>mck</sub> = 20 MHz |      |      | 3.3                 | Mbps |

UART mode connection diagram



UART mode bit width (reference)



**Remark** f<sub>mck</sub>: Serial array unit operation clock frequency  
 (Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0, 1))

**(2) CSI mode (master mode, SCKp... internal clock output)****( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

| Parameter   | Symbol             | Conditions                                   | MIN.   | TYP. | MAX. | Unit |
|---|--------------------|--|--|------|------|------|
| SCKp cycle time   | $t_{KCY1}$         | $t_{KCY1} \geq 4/f_{CLK}$                    | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 200  |      | ns   |
|   |                    |  | $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 800  |      | ns   |
| SCKp high-/low-level width  | $t_{KH1}, t_{KL1}$ | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $t_{KCY1}/2 - 18$                            |      |      | ns   |
|   |                    | $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $t_{KCY1}/2 - 50$                            |      |      | ns   |
| Slp setup time (to SCKp $\uparrow$ ) <sup>Note 1</sup>            | $t_{SIK1}$         | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 47   |      |      | ns   |
|   |                    | $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 110  |      |      | ns   |
| Slp hold time (from SCKp $\uparrow$ ) <sup>Note 1</sup>           | $t_{KSH1}$         |  | 19   |      |      | ns   |
| Delay time from SCKp $\downarrow$ to SOp output <sup>Note 2</sup> | $t_{KS01}$         | $C = 30\text{ pF}$ <sup>Note 3</sup>         |  |      | 25   | ns   |

- Notes**
1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The Slp setup time becomes “to SCKp $\downarrow$ ” and Slp hold time becomes “from SCKp $\downarrow$ ” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.
  2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.
  3. C is the load capacitance of the SCKp and SOp output lines.

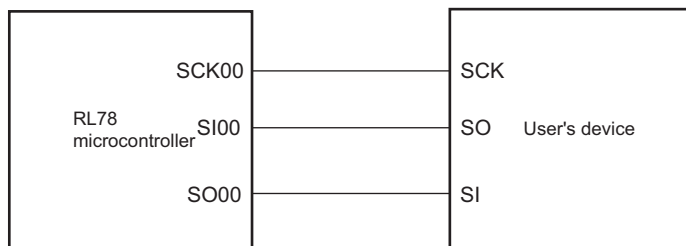
**(3) CSI mode (slave mode, SCKp... external clock input)****( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

| Parameter   | Symbol             | Conditions                                   | MIN.   | TYP.        | MAX.              | Unit |
|---|--------------------|--|--|-------------|-------------------|------|
| SCKp cycle time   | $t_{KCY2}$         | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $f_{MCK} > 16\text{ MHz}$                    | $8/f_{MCK}$ |                   | ns   |
|   |                    |  | $f_{MCK} \leq 16\text{ MHz}$                 | $6/f_{MCK}$ |                   | ns   |
|   |                    | $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $6/f_{MCK}$                                  |             | ns                |      |
| SCKp high-/low-level width  | $t_{KH2}, t_{KL2}$ | $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $t_{KCY2}/2 - 18$                            |             |                   | ns   |
| Slp setup time (to SCKp $\uparrow$ ) <sup>Note 1</sup>            | $t_{SIK2}$         | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $1/f_{MCK} + 20$                             |             |                   | ns   |
|   |                    | $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $1/f_{MCK} + 30$                             |             |                   | ns   |
| Slp hold time (from SCKp $\uparrow$ ) <sup>Note 1</sup>           | $t_{KSH2}$         | $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $1/f_{MCK} + 31$                             |             |                   | ns   |
| Delay time from SCKp $\downarrow$ to SOp output <sup>Note 2</sup> | $t_{KS02}$         | $C = 30\text{ pF}$ <sup>Note 3</sup>         | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |             | $2/f_{MCK} + 50$  | ns   |
|   |                    |  | $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |             | $2/f_{MCK} + 110$ | ns   |

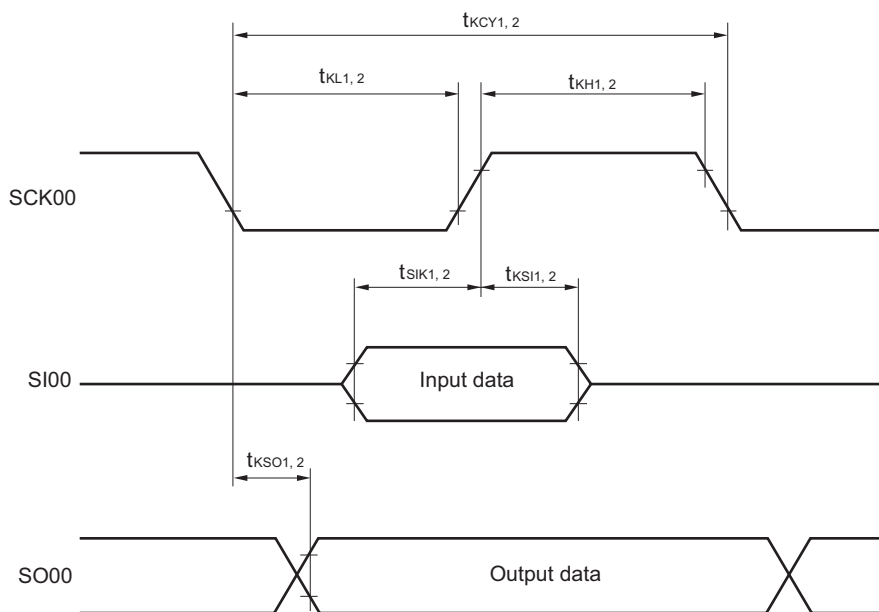
- Notes**
1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The Slp setup time becomes “to SCKp $\downarrow$ ” and the Slp hold time becomes “from SCKp $\downarrow$ ” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.
  2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.
  3. C is the load capacitance of the SOp output lines.

- Remarks**
1. p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)
  2.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0, 1))

**CSI mode connection diagram**



**CSI mode serial transfer timing**  
 (When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1.)



**Remark** p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

**(4) Simplified I<sup>2</sup>C mode**

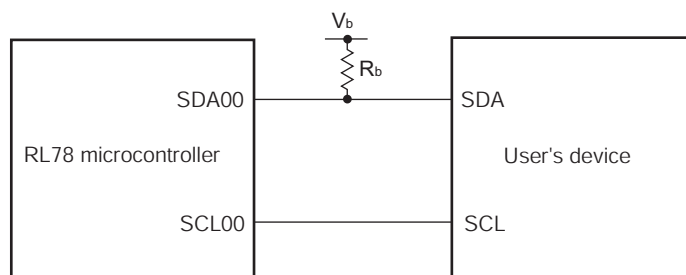
(T<sub>A</sub> = -40 to +85°C, 2.0 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

| Parameter                     | Symbol               | Conditions                                     | MIN.                                       | MAX.                  | Unit |
|-------------------------------|----------------------|--|--|-----------------------|------|
| SCLr clock frequency          | f <sub>SCL</sub>     | C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ |  | 400 <sup>Note 1</sup> | kHz  |
| Hold time when SCLr = "L"     | t <sub>LOW</sub>     | C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ | 1150                                       |                       | ns   |
| Hold time when SCLr = "H"     | t <sub>HIGH</sub>    | C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ | 1150                                       |                       | ns   |
| Data setup time (reception)   | t <sub>SU: DAT</sub> | C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ | 1/f <sub>MCK</sub> + 145 <sup>Note 2</sup> |                       | ns   |
| Data hold time (transmission) | t <sub>HD: DAT</sub> | C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ | 0  | 355                   | ns   |

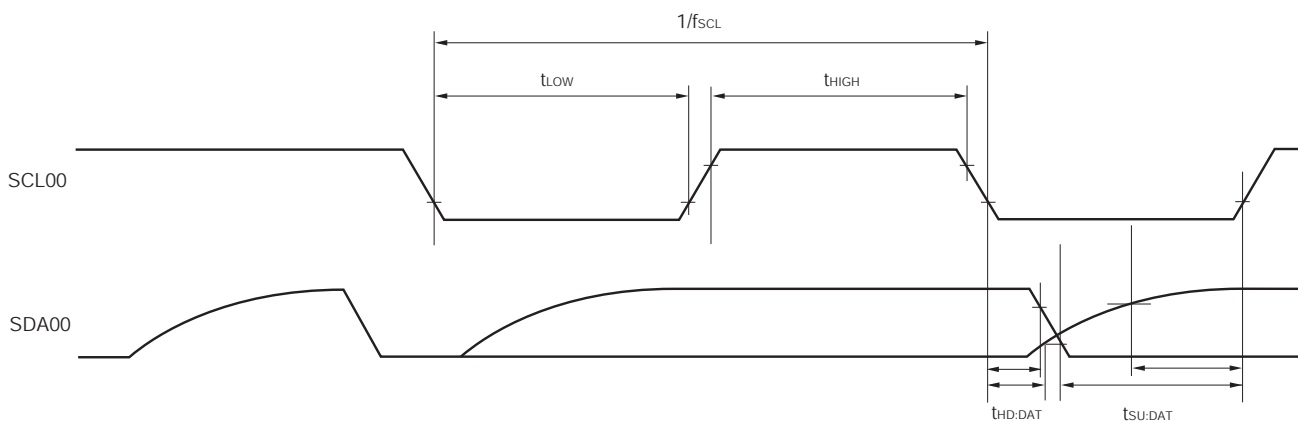
- Notes**
1. The value must also be equal to or less than f<sub>MCK</sub>/4.
  2. Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the N-ch open drain output (V<sub>DD</sub> tolerance) mode for the SDAr pin by using the port output mode register 0 (POM0).

**Simplified I<sup>2</sup>C mode connection diagram**



**Simplified I<sup>2</sup>C mode serial transfer timing**



- Remarks**
1. R<sub>b</sub> [Ω]: Communication line (SDAr) pull-up resistance,  
C<sub>b</sub> [F]: Communication line (SCLr, SDAr) load capacitance
  2. r: IIC number (r = 00)
  3. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0))



2.5.2 Serial interface IICA

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

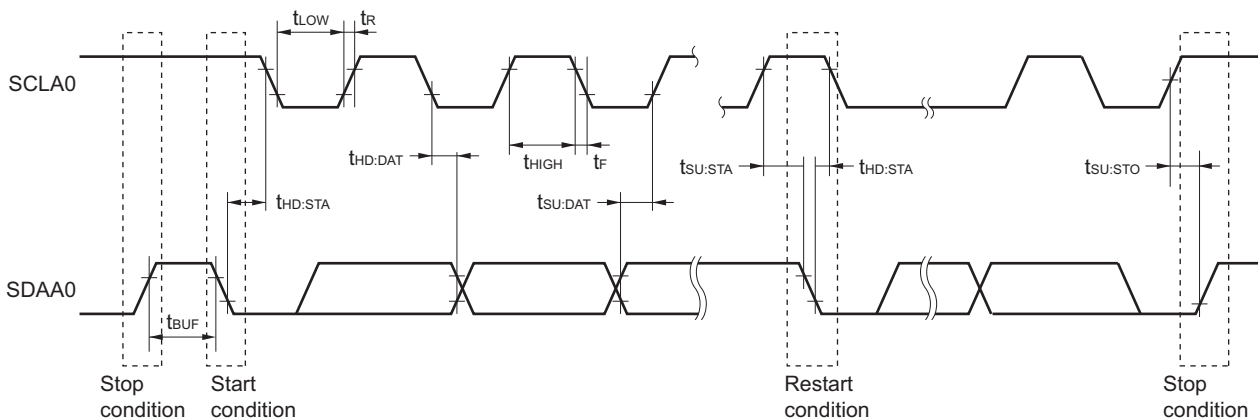
| Parameter                                       | Symbol       | Conditions                                 | Standard Mode |      | Fast Mode |      | Unit          |
|---|--------------|--|---------------|------|-----------|------|---------------|
|   |              |  | MIN.          | MAX. | MIN.      | MAX. |               |
| SCLA0 clock frequency                           | $f_{SCL}$    | Fast mode: $f_{CLK} \geq 3.5\text{ MHz}$   |               |      | 0         | 400  | kHz           |
|   |              | Standard mode: $f_{CLK} \geq 1\text{ MHz}$ | 0             | 100  |           |      |               |
| Setup time of restart condition                 | $t_{SU:STA}$ |  | 4.7           |      | 0.6       |      | $\mu\text{S}$ |
| Hold time <sup>Note 1</sup>                     | $t_{HD:STA}$ |  | 4.0           |      | 0.6       |      | $\mu\text{S}$ |
| Hold time when SCLA0 = "L"                      | $t_{LOW}$    |  | 4.7           |      | 1.3       |      | $\mu\text{S}$ |
| Hold time when SCLA0 = "H"                      | $t_{HIGH}$   |  | 4.0           |      | 0.6       |      | $\mu\text{S}$ |
| Data setup time (reception)                     | $t_{SU:DAT}$ |  | 250           |      | 100       |      | ns            |
| Data hold time (transmission) <sup>Note 2</sup> | $t_{HD:DAT}$ |  | 0             | 3.45 | 0         | 0.9  | $\mu\text{S}$ |
| Setup time of stop condition                    | $t_{SU:STO}$ |  | 4.0           |      | 0.6       |      | $\mu\text{S}$ |
| Bus-free time                                   | $t_{BUF}$    |  | 4.7           |      | 1.3       |      | $\mu\text{S}$ |

- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
  - The maximum value (MAX.) of  $t_{HD:DAT}$  is during normal transfer and a wait state is inserted in the  $\overline{\text{ACK}}$  (acknowledge) timing.

**Remark** The maximum value of  $C_b$  (communication line capacitance) and the value of  $R_b$  (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode:  $C_b = 400\text{ pF}$ ,  $R_b = 2.7\text{ k}\Omega$   
 Fast mode:  $C_b = 200\text{ pF}$ ,  $R_b = 1.7\text{ k}\Omega$

IICA serial transfer timing



## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

(Target pin: ANI0 to ANI6, internal reference voltage)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter   | Symbol            | Conditions  |  | MIN.                               | TYP.      | MAX.            | Unit          |
|---|-------------------|---|--|------------------------------------|-----------|-----------------|---------------|
| Resolution  | RES               |   |  | 8                                  |           | 10              | bit           |
| Overall error <sup>Notes 1, 2, 3</sup>                | AINL              | 10-bit resolution   | $V_{DD} = 5\text{ V}$  |                                    | $\pm 1.7$ | $\pm 3.1$       | LSB           |
|   |                   |   | $V_{DD} = 3\text{ V}$  |                                    | $\pm 2.3$ | $\pm 4.5$       | LSB           |
| Conversion time                                       | $t_{\text{conv}}$ | 10-bit resolution<br>Target pin: ANI0 to ANI6                                       | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   | 3.4                                |           | 18.4            | $\mu\text{s}$ |
|   |                   |   | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ <sup>Note 5</sup> | 4.6                                |           | 18.4            | $\mu\text{s}$ |
|   |                   | 10-bit resolution<br>Target pin:<br>internal reference<br>voltage <sup>Note 6</sup> | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   | 4.6                                |           | 18.4            | $\mu\text{s}$ |
| Zero-scale error <sup>Notes 1, 2, 3, 4</sup>          | E <sub>ZS</sub>   | 10-bit resolution   | $V_{DD} = 5\text{ V}$  |                                    |           | $\pm 0.19$      | %FSR          |
|   |                   |   | $V_{DD} = 3\text{ V}$  |                                    |           | $\pm 0.39$      | %FSR          |
| Full-scale error <sup>Notes 1, 2, 3, 4</sup>          | E <sub>FS</sub>   | 10-bit resolution   | $V_{DD} = 5\text{ V}$  |                                    |           | $\pm 0.29$      | %FSR          |
|   |                   |   | $V_{DD} = 3\text{ V}$  |                                    |           | $\pm 0.42$      | %FSR          |
| Integral linearity error <sup>Notes 1, 2, 3</sup>     | ILE               | 10-bit resolution   | $V_{DD} = 5\text{ V}$  |                                    |           | $\pm 1.8$       | LSB           |
|   |                   |   | $V_{DD} = 3\text{ V}$  |                                    |           | $\pm 1.7$       | LSB           |
| Differential linearity error <sup>Notes 1, 2, 3</sup> | DLE               | 10-bit resolution   | $V_{DD} = 5\text{ V}$  |                                    |           | $\pm 1.4$       | LSB           |
|   |                   |   | $V_{DD} = 3\text{ V}$  |                                    |           | $\pm 1.5$       | LSB           |
| Analog input voltage                                  | V <sub>AIN</sub>  | Target pin: ANI0 to ANI6  |  | 0                                  |           | V <sub>DD</sub> | V             |
|   |                   | Target pin: internal reference voltage <sup>Note 6</sup>                            |  | V <sub>REG</sub> <sup>Note 7</sup> |           |                 | V             |

**Notes** 1. TYP. Value is the average value at  $T_A = 25^\circ\text{C}$ . MAX. value is the average value  $\pm 3\sigma$  at normal distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error ( $\pm 1/2$  LSB).

4. This value is indicated as a ratio (%FSR) to the full-scale value.

5. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when conversion is done in the operating voltage range of  $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$ .

6. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when the internal reference voltage is selected as the target for conversion.

7. Refer to **2.6.3 Internal reference voltage characteristics**.

**Cautions** 1. Arrange wiring and insert the capacitor so that no noise appears on the power supply/ground line.

2. Do not allow any pulses that rapidly change such as digital signals to be input/output to/from the pins adjacent to the conversion pin during A/D conversion.

3. Note that the internal reference voltage cannot be used as the reference voltage of the comparator when the internal reference voltage is selected as the target for A/D conversion.

### 2.6.2 Comparator characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                         | Symbol           | Conditions  | MIN.                               | TYP. | MAX.           | Unit |
|-----------------------------------|------------------|---|------------------------------------|------|----------------|------|
| Input voltage range               | IVREF            | IVREF0 pin input (when C0VFR bit = 0)                             | 0                                  |      | $V_{DD} - 1.4$ | V    |
|                                   |                  | Internal reference voltage (when C0VRF bit = 1) <sup>Note 1</sup> | V <sub>REG</sub> <sup>Note 2</sup> |      |                | V    |
|                                   | IVCMP            | IVCMP0 pin input  | -0.3                               |      | $V_{DD} + 0.3$ | V    |
| Output delay                      | td               | V <sub>DD</sub> = 3.0 V,<br>input slew rate > 50<br>mV/μs         | High-speed mode                    |      | 0.5            | μs   |
|                                   |                  |   | Low-speed mode                     |      | 2.0            | μs   |
| Operation stabilization wait time | t <sub>CMP</sub> |   | 100                                |      |                | μs   |

- Notes**
1. When the internal reference voltage is selected as the reference voltage of the comparator, the internal reference voltage cannot be used as the target for A/D conversion.
  2. Refer to 2.6.3 Internal reference voltage characteristics.

### 2.6.3 Internal reference voltage characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                         | Symbol           | Conditions   | MIN. | TYP.  | MAX. | Unit |
|-----------------------------------|------------------|--|------|-------|------|------|
| Internal reference voltage        | V <sub>REG</sub> |  | 0.74 | 0.815 | 0.89 | V    |
| Operation stabilization wait time | t <sub>AMP</sub> | When A/D converter is used<br>(ADS register = 07H) | 5    |       |      | μs   |

**Note** The internal reference voltage cannot be simultaneously used by the A/D converter and the comparator; only one of them must be selected.

2.6.4 SPOR circuit characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0$  V)

| Parameter                           |                            | Symbol      | Conditions             | MIN. | TYP. | MAX. | Unit          |
|-------------------------------------|----------------------------|-------------|------------------------|------|------|------|---------------|
| Detection voltage                   | Power supply voltage level | $V_{SPOR0}$ | Power supply rise time | 4.08 | 4.28 | 4.45 | V             |
|                                     |                            |             | Power supply fall time | 4.00 | 4.20 | 4.37 | V             |
|                                     |                            | $V_{SPOR1}$ | Power supply rise time | 2.76 | 2.90 | 3.02 | V             |
|                                     |                            |             | Power supply fall time | 2.70 | 2.84 | 2.96 | V             |
|                                     |                            | $V_{SPOR2}$ | Power supply rise time | 2.44 | 2.57 | 2.68 | V             |
|                                     |                            |             | Power supply fall time | 2.40 | 2.52 | 2.62 | V             |
|                                     |                            | $V_{SPOR3}$ | Power supply rise time | 2.05 | 2.16 | 2.25 | V             |
|                                     |                            |             | Power supply fall time | 2.00 | 2.11 | 2.20 | V             |
| Minimum pulse width <sup>Note</sup> |                            | $T_{LSPW}$  |                        | 300  |      |      | $\mu\text{s}$ |

**Note** Time required for the reset operation by the SPOR when  $V_{DD}$  becomes under  $V_{SPOR}$ .

**Caution** Set the detection voltage ( $V_{SPOR}$ ) in the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H). The operating voltage range is as follows:

When the CPU operating frequency is from 1 MHz to 20 MHz:  $V_{DD} = 2.7$  to 5.5 V

When the CPU operating frequency is from 1 MHz to 5 MHz:  $V_{DD} = 2.0$  to 5.5 V

2.6.5 Power supply voltage rising slope characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0$  V)

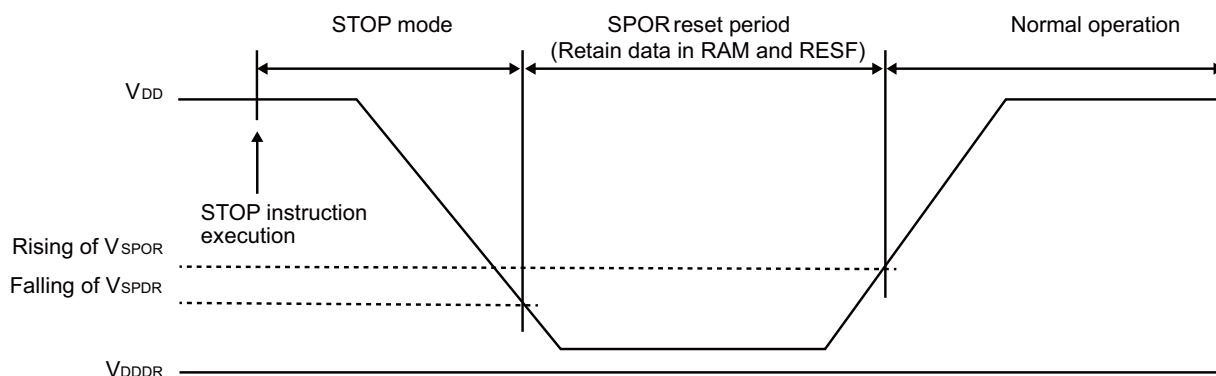
| Parameter                         | Symbol    | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|-----------|------------|------|------|------|------|
| Power supply voltage rising slope | $S_{VDD}$ |            |      |      | 54   | V/ms |

<R> 2.7 RAM Data Retention Characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0$  V)

| Parameter                           | Symbol     | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|------------|------------|------|------|------|------|
| Data retention power supply voltage | $V_{DDDR}$ |            | 1.9  |      | 5.5  | V    |

**Caution** Data in RAM is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage ( $V_{DDDR}$ ). Note that data in the RESF register might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage ( $V_{DDDR}$ ).



## 2.8 Flash Memory Programming Characteristics

( $T_A = 0$  to  $+40^\circ\text{C}$ ,  $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter   | Symbol     | Conditions             |                           | MIN. | TYP. | MAX. | Unit  |
|---|------------|------------------------|---------------------------|------|------|------|-------|
| Code flash memory rewritable times <sup>Notes 1, 2, 3</sup> | $C_{erwr}$ | Retained for 20 years. | $T_A = +85^\circ\text{C}$ | 1000 |      |      | Times |

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
  2. When using flash memory programmer.
  3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

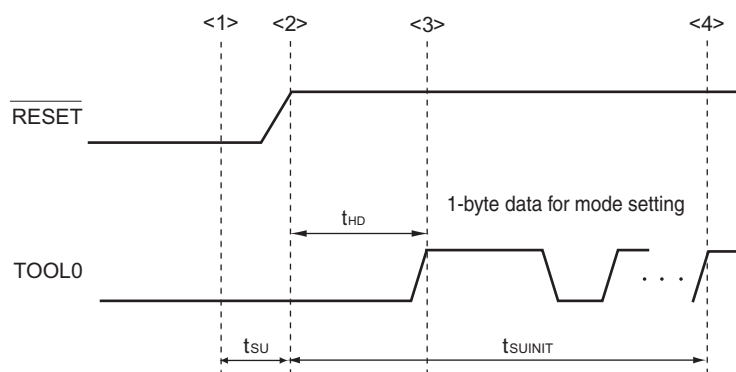
( $T_A = 0$  to  $+40^\circ\text{C}$ ,  $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter     | Symbol | Conditions | MIN. | TYP.    | MAX. | Unit |
|---------------|--------|------------|------|---------|------|------|
| Transfer rate |        |            |      | 115,200 |      | bps  |

**Remark** The transfer rate during flash memory programming is fixed to 115,200 bps.

2.10 Timing of Entry to Flash Memory Programming Modes

| Parameter   | Symbol       | Conditions   | MIN. | TYP. | MAX. | Unit    |
|---|--------------|--|------|------|------|---------|
| Time to complete the communication for the initial setting after the external reset is released | $t_{SUINIT}$ | SPOR reset must be released before the external reset is released. |      |      | 100  | ms      |
| Time to release the external reset after the TOOL0 pin is set to the low level                  | $t_{SU}$     | SPOR reset must be released before the external reset is released. | 10   |      |      | $\mu$ s |
| Time to hold the TOOL0 pin at the low level after the external reset is released                | $t_{HD}$     | SPOR reset must be released before the external reset is released. | 1    |      |      | ms      |



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (SPOR reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of entry to the flash memory programming mode by UART reception is completed.

**Remark**  $t_{SUINIT}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{SU}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{HD}$ : Time to hold the TOOL0 pin at the low level after the external reset is released

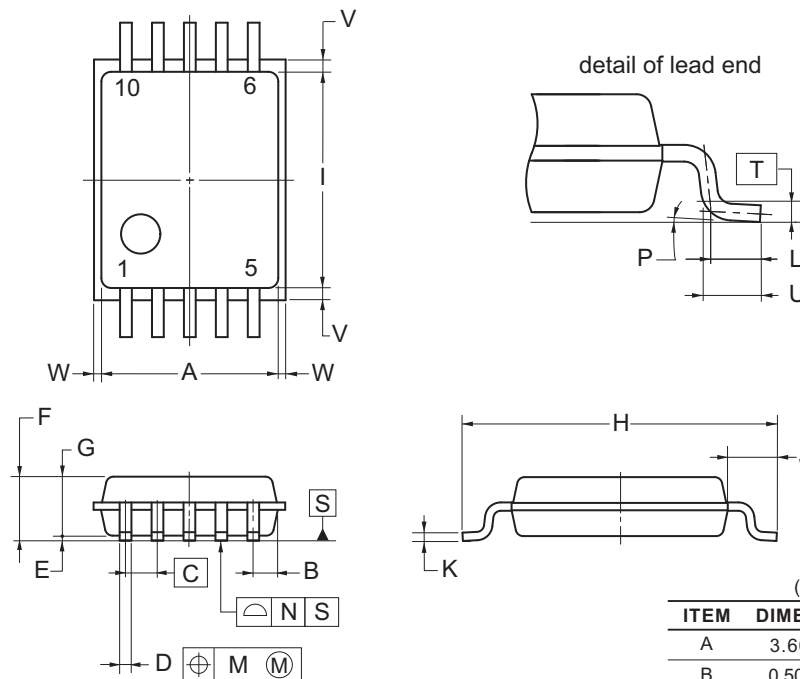
3. PACKAGE DRAWINGS

3.1 10-pin products

R5F10Y17ASP, R5F10Y16ASP, R5F10Y14ASP

<R> R5F10Y17DSP<sup>Note</sup>, R5F10Y16DSP<sup>Note</sup>, R5F10Y14DSP<sup>Note</sup>

|                        |              |                |                 |
|------------------------|--------------|----------------|-----------------|
| JEITA Package Code     | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
| P-LSSOP10-4.4x3.6-0.65 | PLSP0010JA-A | P10MA-65-CAC-2 | 0.05            |



**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

(UNIT: mm)

| ITEM | DIMENSIONS                             |
|------|--|
| A    | 3.60±0.10                              |
| B    | 0.50                                   |
| C    | 0.65 (T.P.)                            |
| D    | 0.24±0.08                              |
| E    | 0.10±0.05                              |
| F    | 1.45 MAX.                              |
| G    | 1.20±0.10                              |
| H    | 6.40±0.20                              |
| I    | 4.40±0.10                              |
| J    | 1.00±0.20                              |
| K    | 0.17 <sup>+0.08</sup> <sub>-0.07</sub> |
| L    | 0.50                                   |
| M    | 0.13                                   |
| N    | 0.10                                   |
| P    | 3° <sup>+5°</sup> <sub>-3°</sub>       |
| T    | 0.25 (T.P.)                            |
| U    | 0.60±0.15                              |
| V    | 0.25 MAX.                              |
| W    | 0.15 MAX.                              |

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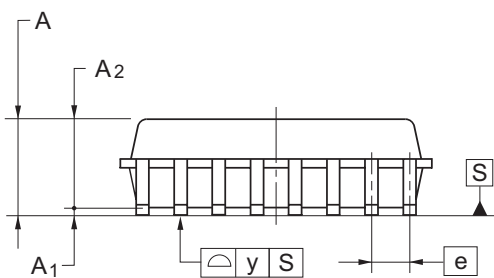
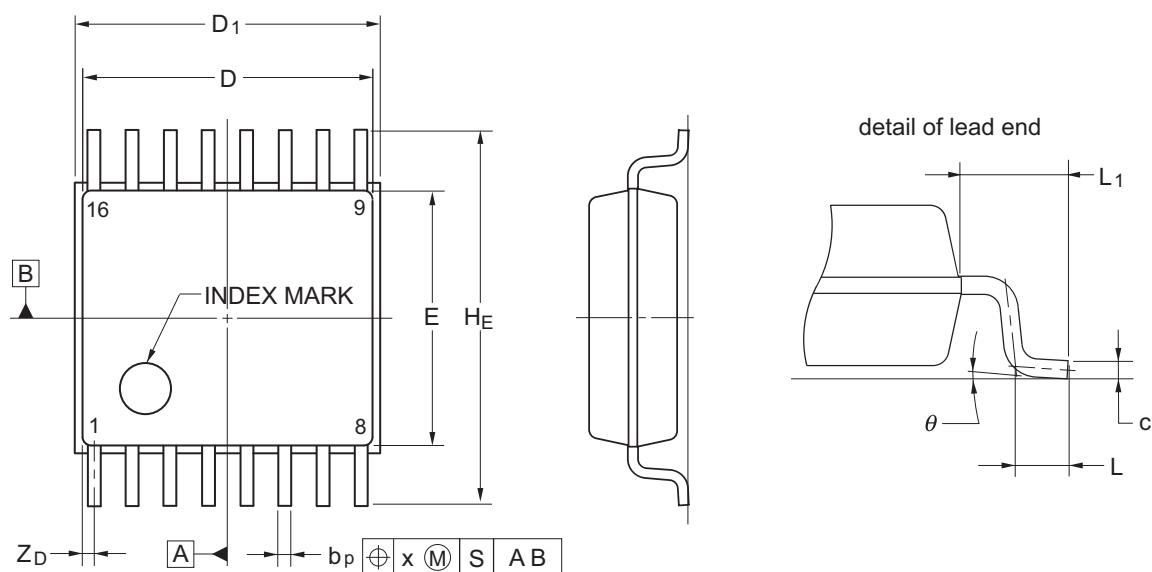
**Note** Under development

3.2 16-pin products

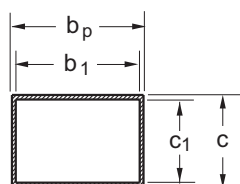
R5F10Y47ASP, R5F10Y46ASP, R5F10Y44ASP

<R> R5F10Y47DSP <sup>Note</sup>, R5F10Y46DSP <sup>Note</sup>, R5F10Y44DSP <sup>Note</sup>

|     |                     |              |                |               |
|-----|---------------------|--------------|----------------|---------------|
| <R> | JEITA Package code  | RENESAS code | Previous code  | MASS(TYP.)[g] |
|     | P-SSOP16-4.4x5-0.65 | PRSP0016JC-B | P16MA-65-FAB-1 | 0.08          |



Terminal cross section



| Reference Symbol | Dimension in Millimeters |       |       |
|------------------|--------------------------|-------|-------|
|                  | Min                      | Nom   | Max   |
| D                | 4.85                     | 5.00  | 5.15  |
| D <sub>1</sub>   | 5.05                     | 5.20  | 5.35  |
| E                | 4.20                     | 4.40  | 4.60  |
| A <sub>2</sub>   | —                        | 1.50  | —     |
| A <sub>1</sub>   | 0.075                    | 0.125 | 0.175 |
| A                | —                        | —     | 1.725 |
| b <sub>p</sub>   | 0.17                     | 0.24  | 0.32  |
| b <sub>1</sub>   | —                        | 0.22  | —     |
| c                | 0.14                     | 0.17  | 0.20  |
| c <sub>1</sub>   | —                        | 0.15  | —     |
| θ                | 0°                       | —     | 8°    |
| H <sub>E</sub>   | 6.20                     | 6.40  | 6.60  |
| e                | —                        | 0.65  | —     |
| x                | —                        | —     | 0.13  |
| y                | —                        | —     | 0.10  |
| Z <sub>D</sub>   | —                        | 0.225 | —     |
| L                | 0.35                     | 0.50  | 0.65  |
| L <sub>1</sub>   | —                        | 1.00  | —     |

**Note** Under development



|                         |                           |
|-------------------------|---------------------------|
| <b>Revision History</b> | <b>RL78/G10 Datasheet</b> |
|-------------------------|---------------------------|

| Rev. | Date  | Description |   |
|------|---|-------------|---|
|      |   | Page        | Summary   |
| 1.00 | Apr 15, 2013  | -           | First Edition issued  |
| 2.00 | Jan 10, 2014  | 1, 2        | Modification of descriptions in 1.1 Features  |
|      |   | 3           | Modification of description in 1.2 List of Part Numbers   |
|      |   | 4           | Modification of remark 2 in 1.3.1 10-pin products and 1.3.2 16-pin products   |
|      |   | 8, 9        | Addition of description of R5F10Y17ASP in 1.6 Outline of Functions  |
|      |   | 11          | Modification of description in 2.1 Absolute Maximum Ratings   |
|      |   | 12          | Modification of description in 2.2 Oscillator Characteristics   |
|      |   | 13, 14      | Modification of description, notes 1 to 4, and caution in 2.3.1 Pin characteristics                                       |
|      |   | 16          | Addition of description, notes 1 to 6, and remarks 1 and 2 in (2) Flash ROM: 4 KB of 10-pin products, and 16-pin products |
|      |   | 17          | Addition of description, notes 1 to 6, and remarks 1 to 3 in (3) Peripheral Functions (Common to all products)            |
|      |   | 18          | Modification of description in 2.4 AC Characteristics   |
|      |   | 19          | Addition of figure of Minimum Instruction Execution Time during Main System Clock Operation                               |
|      |   | 19          | Addition of figure of External System Clock Timing  |
|      |   | 20          | Modification of TI/TO Timing  |
|      |   | 25          | Addition of description in 2.5.2 Serial interface IICA  |
|      |   | 26          | Modification of description and notes 1 to 6 in 2.6.1 A/D converter characteristics                                       |
|      |   | 27          | Addition of description, notes 1 and 2 in 2.6.2 Comparator characteristics  |
|      |   | 27          | Addition of description and note in 2.6.3 Internal reference voltage characteristics                                      |
|      |   | 28          | Addition of caution in 2.6.4 SPOR Circuit characteristics   |
|      |   | 28          | Addition of figure in 2.6.6 Data retention power supply voltage characteristics   |
| 3.00 | Nov 19, 2014  | 31          | Addition of R5F10Y17ASP in 3.1 10-pin products  |
|      |   | 32          | Modification of package drawing in 3.2 16-pin products  |
|      |   | 3           | Addition of industrial applications in Figure 1-1 Part Number, Memory Size, and Package of RL78/G10                       |
|      |   | 3           | Addition of industrial applications in Table 1-1 List of Ordering Part Numbers  |
|      |   | 4           | Addition of description to pin configuration in 1.3.1 10-pin products and 1.3.2 16-pin products                           |
|      |   | 22          | Correction of error in 2.5.1 Serial array unit, (3) CSI mode (slave mode, SCKp... external clock input)                   |
|      |   | 28          | Renamed to 2.7 RAM Data Retention Characteristics and modification of figure  |
| 31   | Addition of industrial application in 3.1 10-pin products                                     |             |   |
| 32   | Addition of industrial application in 3.2 16-pin products and modification of package drawing |             |   |

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## NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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