

**0.3A, 60V, 6 Ohm, ESD Rated, Current Limited, Voltage Clamped, Logic Level N-Channel Power MOSFETs**

These are intelligent monolithic power circuits which incorporate a lateral bipolar transistor, resistors, zener diodes and a power MOS transistor. The current limiting of these devices allow it to be used safely in circuits where a shorted load condition may be encountered. The drain to source voltage clamping offers precision control of the circuit voltage when switching inductive loads. The "Logic Level" gate allows this device to be fully biased on with only 5V from gate to source, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

These devices incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

Formerly developmental type TA49028.

**Ordering Information**

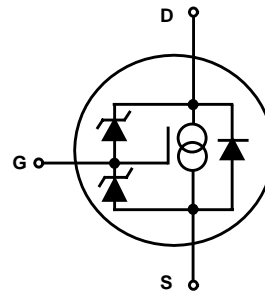
PART NUMBER	PACKAGE	BRAND
RLD03N06CLE	TO-251AA	03N06C
RLD03N06CLESM	TO-252AA	03N06C
RLP03N06CLE	TO-220AB	03N06CLE

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e. RLD03N06CLESM9A.

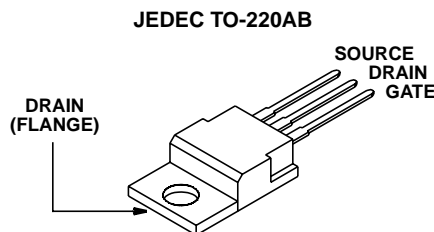
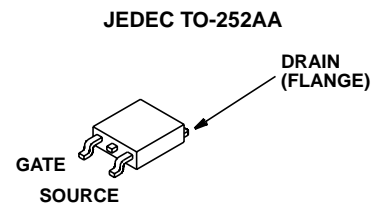
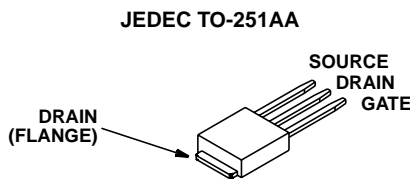
**Features**

- 0.30A, 60V
- $r_{DS(ON)} = 6.0\Omega$
- Built in Current Limit  $I_{LIMIT}$  0.140 to 0.210A at 150°C
- Built in Voltage Clamp
- Temperature Compensating PSPICE® Model
- 2kV ESD Protected
- Controlled Switching Limits EMI and RFI
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**



**Packaging**



# RLD03N06CLE, RLD03N06CLESM, RLP03N06CLE

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RLD03N06CLE, RLD03N06CLESM, RLP03N06CLE	UNITS
Drain to Source Voltage (Note 1)	60	V
Drain to Gate Voltage	60	V
Gate to Source Voltage (Reverse Voltage Gate Bias Not Allowed)	+5.5	V
Continuous Drain Current	Self Limited	
Power Dissipation	30	W
Derate Above $25^\circ\text{C}$	0.2	W/ $^\circ\text{C}$
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	2	KV
Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	60	-	85	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	1	-	2.5	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 45\text{V}$ , $V_{GS} = 0\text{V}$	$T_J = 25^\circ\text{C}$	-	-	25	$\mu\text{A}$
			$T_J = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = 5\text{V}$	$T_J = 25^\circ\text{C}$	-	-	5	$\mu\text{A}$
			$T_J = 150^\circ\text{C}$	-	-	20	$\mu\text{A}$
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 0.100\text{A}$ , $V_{GS} = 5\text{V}$	$T_J = 25^\circ\text{C}$	-	-	6.0	$\Omega$
			$T_J = 150^\circ\text{C}$	-	-	12.0	$\Omega$
Limiting Current	$I_{DS(LIMIT)}$	$V_{DS} = 15\text{V}$ , $V_{GS} = 5\text{V}$	$T_J = 25^\circ\text{C}$	280	-	420	mA
			$T_J = 150^\circ\text{C}$	140	-	210	mA
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}$ , $I_D = 0.10\text{A}$ , $R_L = 300\Omega$ , $V_{GS} = 5\text{V}$ , $R_{GS} = 25\Omega$	-	-	7.5	$\mu\text{s}$	
Turn-On Delay Time	$t_{d(ON)}$		-	-	2.5	$\mu\text{s}$	
Rise Time	$t_r$		-	-	5.0	$\mu\text{s}$	
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	7.5	$\mu\text{s}$	
Fall Time	$t_f$		-	-	5.0	$\mu\text{s}$	
Turn-Off Time	$t_{OFF}$		-	-	12.5	$\mu\text{s}$	
Input Capacitance	$C_{ISS}$		$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	100	-	pF
Output Capacitance	$C_{OSS}$	-		65	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$	-		3.0	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	5.0	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220 Package	-	-	80	$^\circ\text{C/W}$	
		TO-251 and TO-252 Packages	-	-	100	$^\circ\text{C/W}$	

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 0.1\text{A}$	-	-	1.5	V
Diode Reverse Recovery Time	$t_{rr}$	$I_{SD} = 0.1\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	1.0	ms

### NOTES:

- Pulsed: pulse duration =  $\leq 300\mu\text{s}$  maximum, duty cycle =  $\leq 2\%$ .
- Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

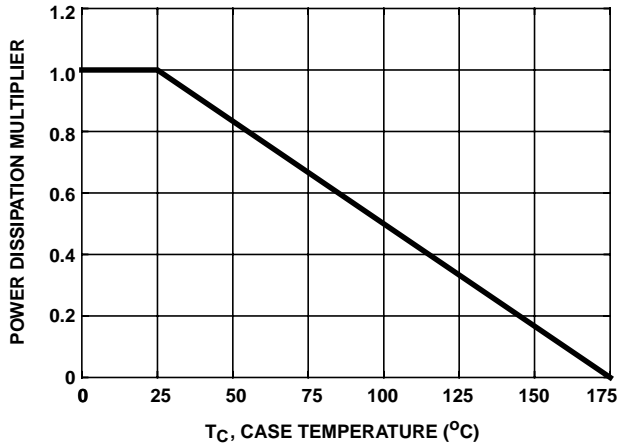


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

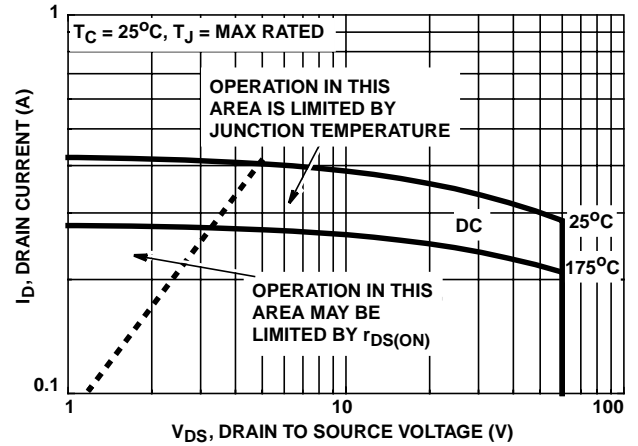


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

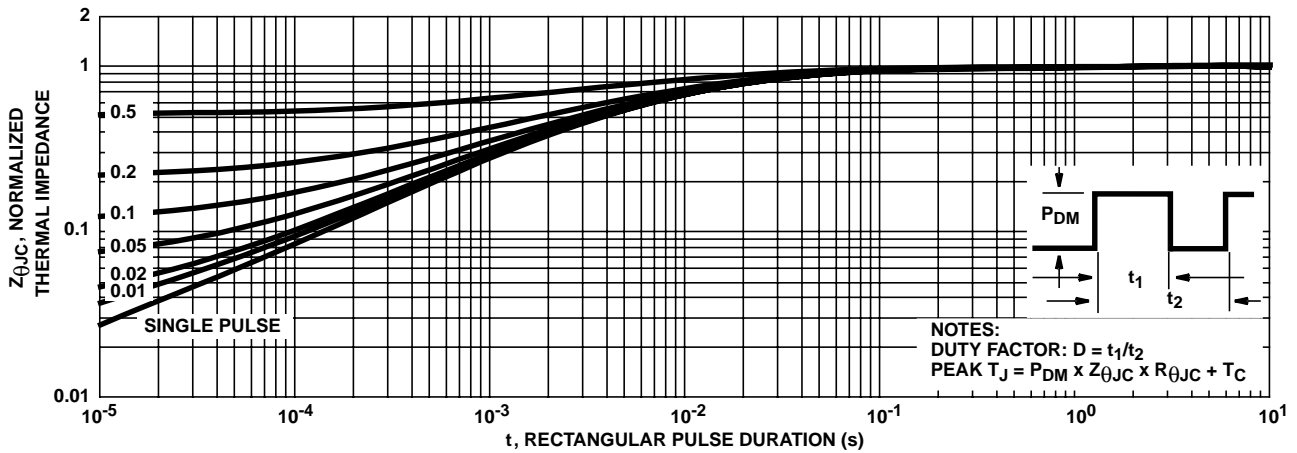


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

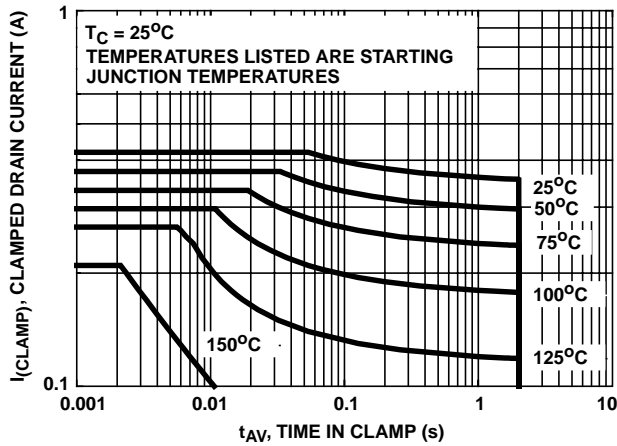


FIGURE 4. SELF-CLAMPED INDUCTIVE SWITCHING

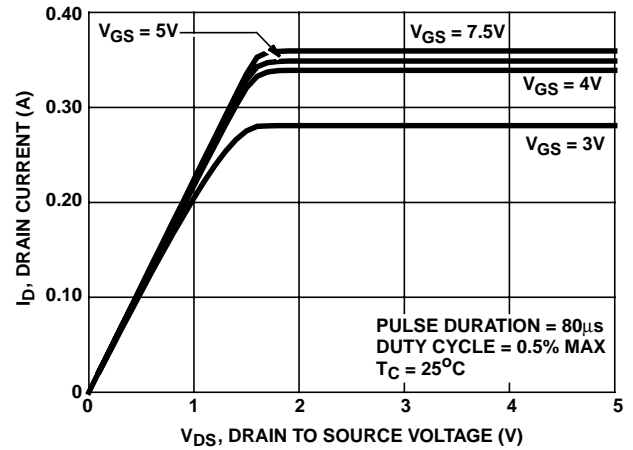


FIGURE 5. SATURATION CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

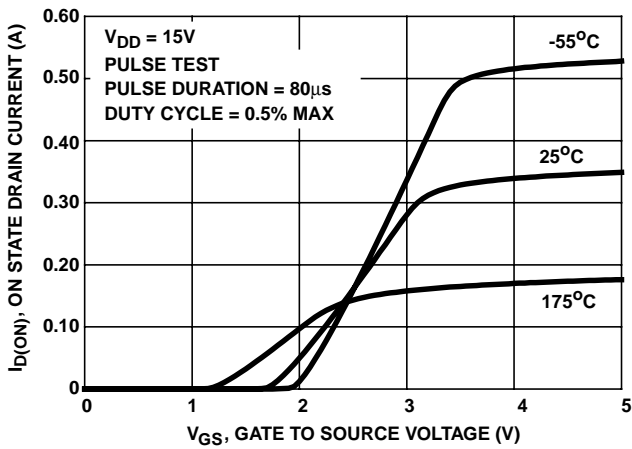


FIGURE 6. TRANSFER CHARACTERISTICS

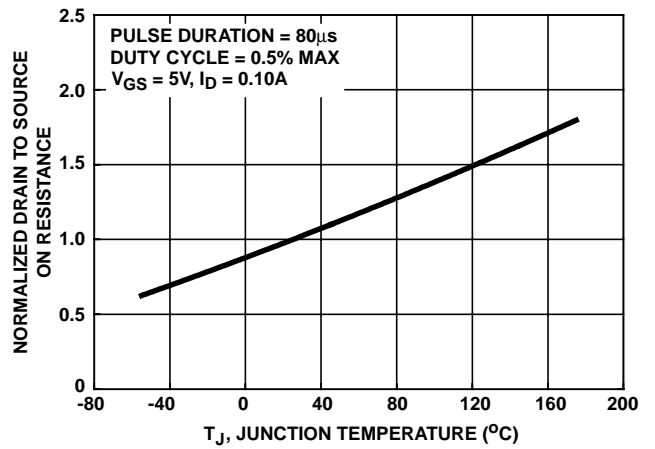


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

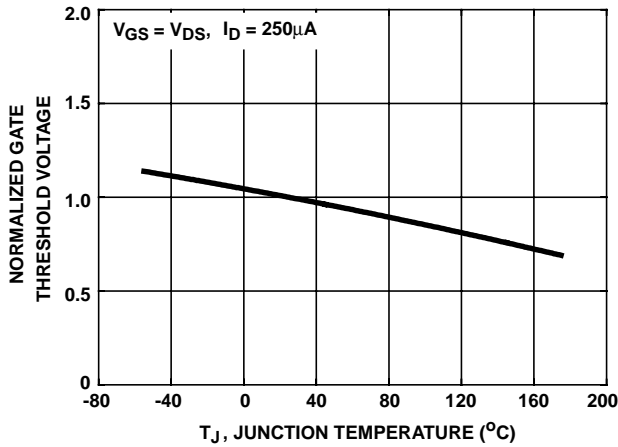


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

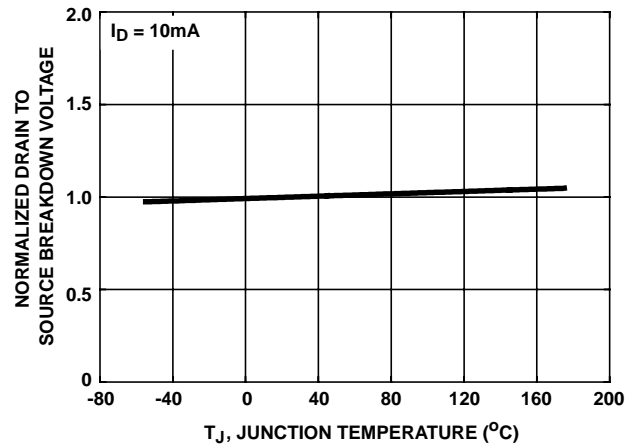


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

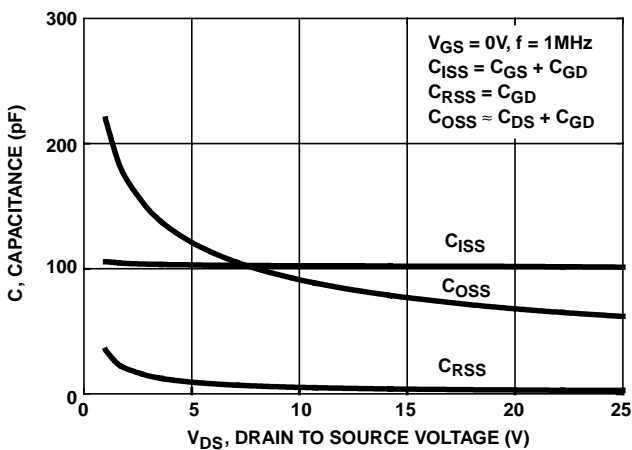


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

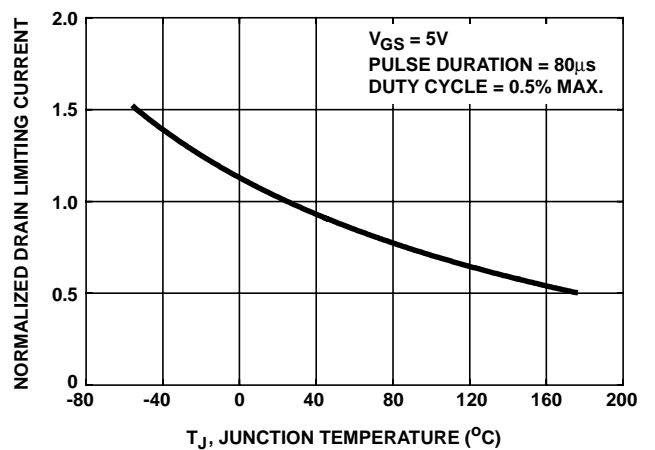
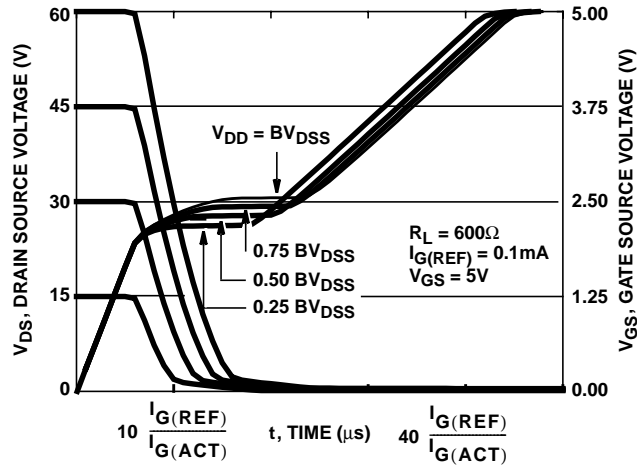


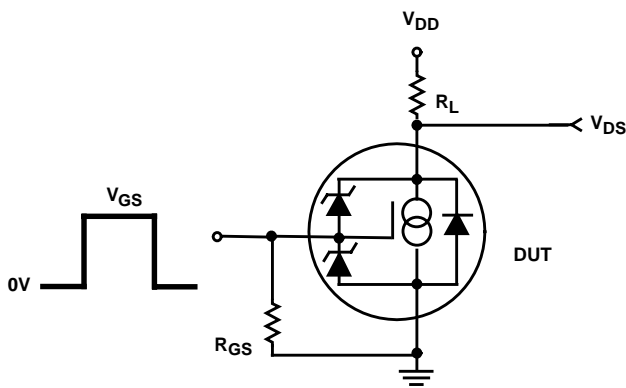
FIGURE 11. NORMALIZED DRAIN LIMITING CURRENT vs JUNCTION TEMPERATURE

**Typical Performance Curves** Unless Otherwise Specified (Continued)

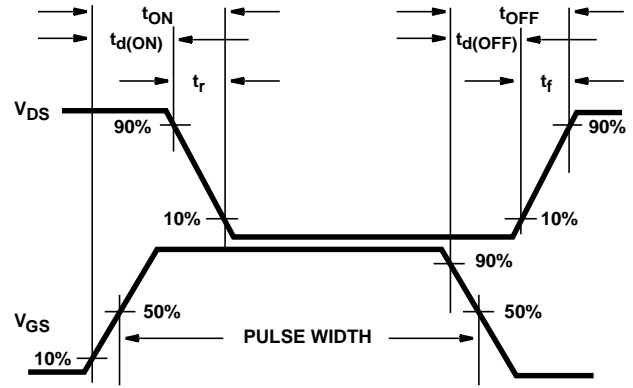


NOTE: Refer to Intersil Application Notes AN7254 and AN7260.  
**FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT.**

**Test Circuits and Waveforms**



**FIGURE 13. RESISTIVE SWITCHING TEST CIRCUIT**



**FIGURE 14. RESISTIVE SWITCHING WAVEFORMS**

**Detailed Description**

**Temperature Dependence of Current Limiting and Switching Speed Performance**

The RLD03N06CLE, CLESM and RLP03N06CLE are monolithic power devices which incorporate a Logic Level power MOSFET transistor with a current sensing scheme and control circuitry to enable the device to self limit the drain source current flow. The current sensing scheme supplies current to a resistor that is connected across the base to emitter of a bipolar transistor in the control section. The collector of this bipolar transistor is connected to the gate of the power MOSFET transistor. When the ratiometric current from the current sensing reaches the value required to forward bias the base emitter junction of this bipolar transistor, the bipolar “turns on”. A resistor is incorporated in series with the gate of the power MOSFET transistor allowing the bipolar transistor to adjust the drive on the gate of the power MOSFET transistor to a voltage which then maintains a constant current in the power MOSFET transistor. Since both the ratiometric current sensing scheme and the base emitter junction

voltage of the bipolar transistor vary with temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 3.

The resistor in series with the gate of the power MOSFET transistor also results in much slower switching performance than in standard power MOSFET transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable.

**DC Operation**

The limit on the drain to source voltage for operation in current limiting on a steady state (DC) basis is shown in the equation below. The dissipation in the device is simply the applied drain to source voltage multiplied by the limiting current. This device, like most power MOSFET devices today, is limited to 175°C. The maximum voltage allowable can, therefore, be expressed as shown in Equation 1:

$$V_{DS} = \frac{(150^{\circ}\text{C} - T_{\text{AMBIENT}})}{I_{\text{LM}} \cdot (R_{\theta\text{JC}} + R_{\theta\text{JA}})} \quad (\text{EQ. 1})$$

The results of this equation are plotted in Figure 15 for various heatsinks.

**Duty Cycle Operation**

In many applications either the drain to source voltage or the gate drive is not available 100% of the time. The copper header on which the RLD03N06CLE, CLESM and RLP03N06CLE is mounted has a very large thermal storage capability, so for pulse widths of less than 1ms, the temperature of the header can be considered a constant, thereby the junction temperature can be calculated simply as shown in Equation 2:

$$T_C = (V_{DS} \cdot I_D \cdot D \cdot R_{\theta CA}) + T_{AMBIENT} \quad (EQ.2)$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to 175°C and using the  $T_C$  calculated in Equation 2, the expression for maximum  $V_{DS}$  under duty cycle operation is shown in Equation 3

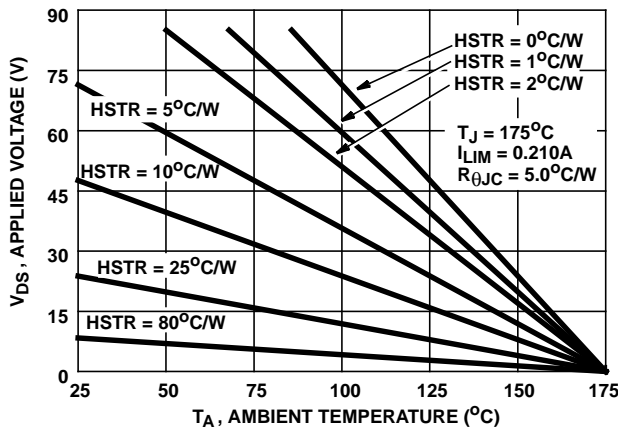
$$V_{DS} = \frac{150^\circ C - T_C}{I_{LM} \cdot D \cdot R_{\theta JC}} \quad (EQ.3)$$

These values are plotted as Figures 16 through 21 for various heatsink thermal resistances.

**Limited Time Operations**

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 ms, thereby the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures 22 through 25 (RLP03N06CLE) and Figure 26 through 29 (RLD03N06CLE and RLD03N06CLESM) give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 175°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

**Typical Performance Curves**



NOTE: Heat Sink Thermal Resistance = HSTR.

FIGURE 15. DC OPERATION IN CURRENT LIMITING

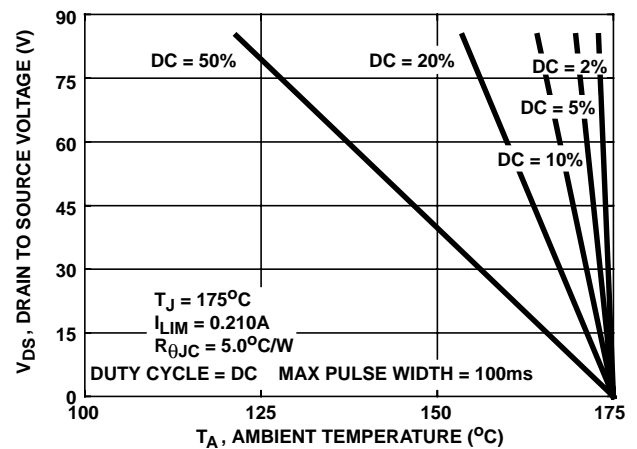


FIGURE 16. MAXIMUM  $V_{DS}$  vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 1°C/W)

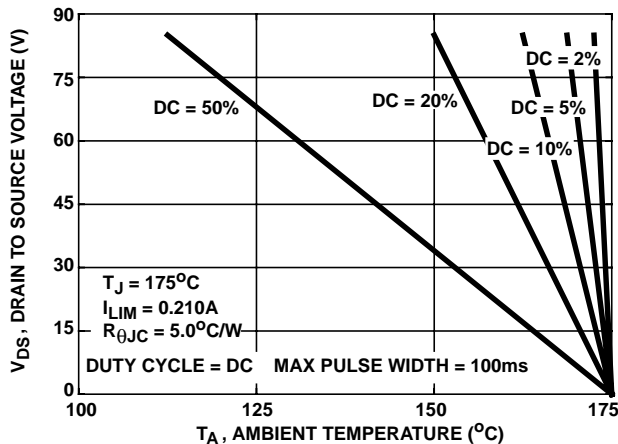


FIGURE 17. MAXIMUM  $V_{DS}$  vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 2°C/W)

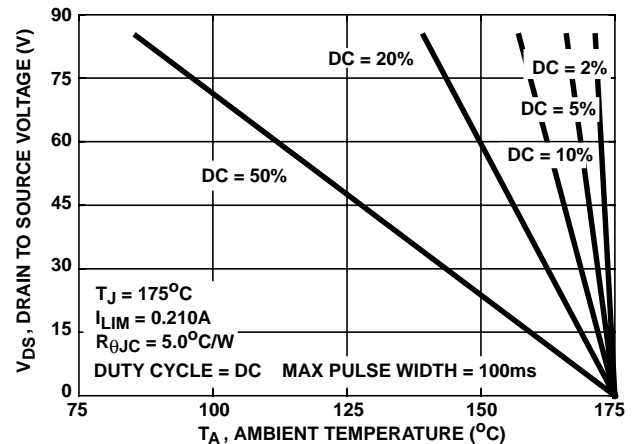


FIGURE 18. MAXIMUM  $V_{DS}$  vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 5°C/W)

Typical Performance Curves (Continued)

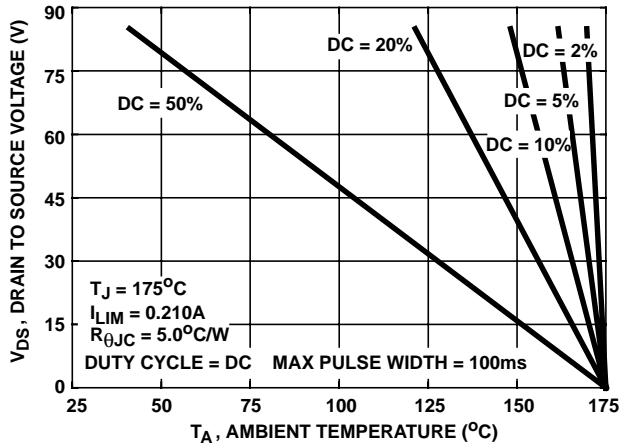


FIGURE 19. MAXIMUM  $V_{DS}$  vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 10°C/W)

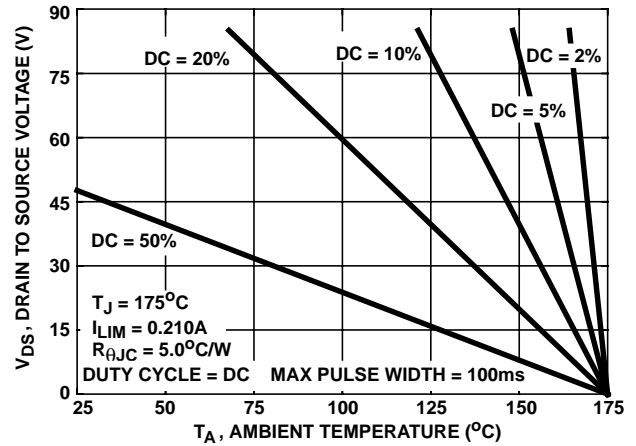
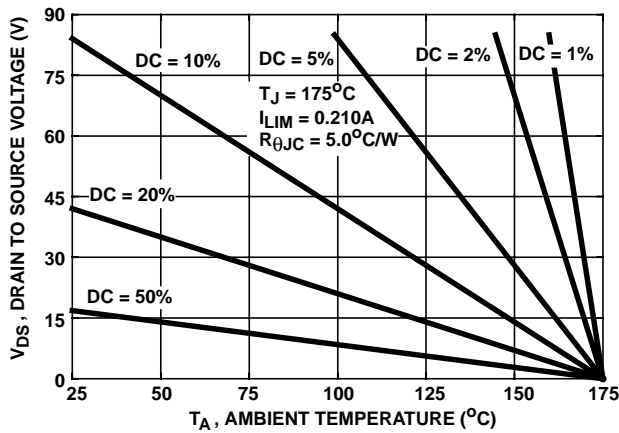


FIGURE 20. MAXIMUM  $V_{DS}$  vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 25°C/W)



NOTE: Duty Cycle = DC, Max Pulse Width = 100ms.

FIGURE 21. MAXIMUM  $V_{DS}$  vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 80°C/W)

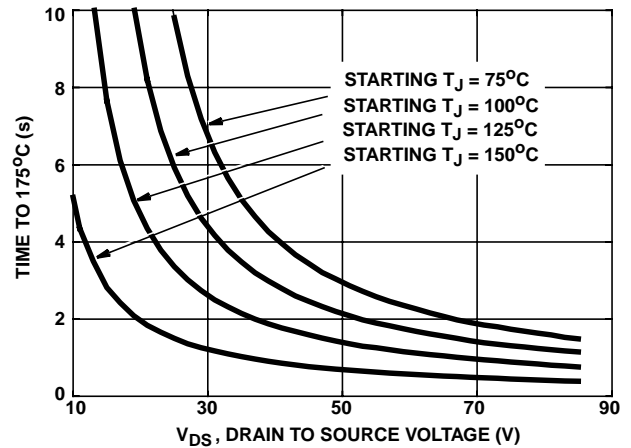


FIGURE 22. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 25°C/W) (HEATSINK THERMAL CAPACITANCE = 0.5J/°C)

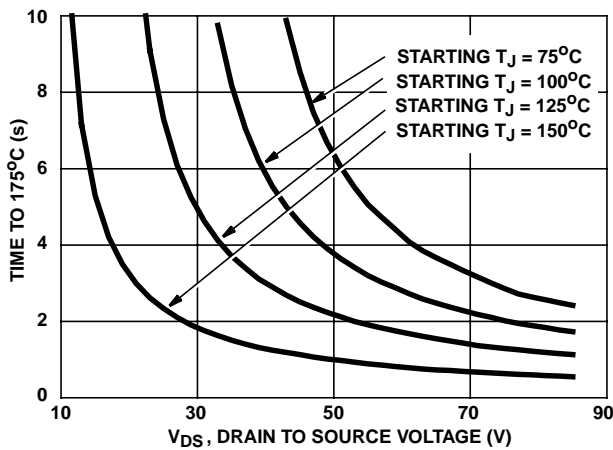


FIGURE 23. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 10°C/W) (HEATSINK THERMAL CAPACITANCE = 1.0J/°C)

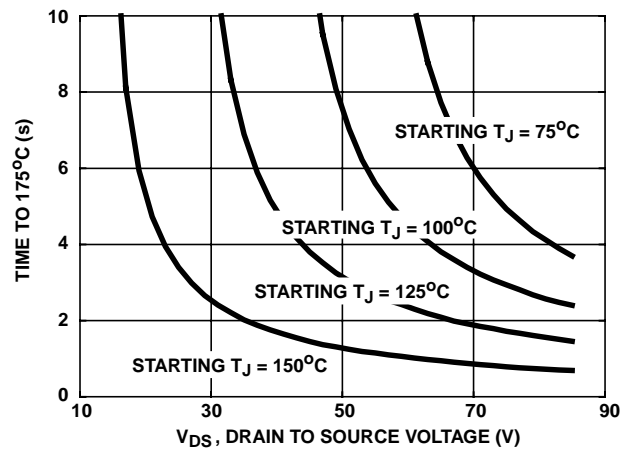


FIGURE 24. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 5°C/W) (HEATSINK THERMAL CAPACITANCE = 2.0J/°C)

Typical Performance Curves (Continued)

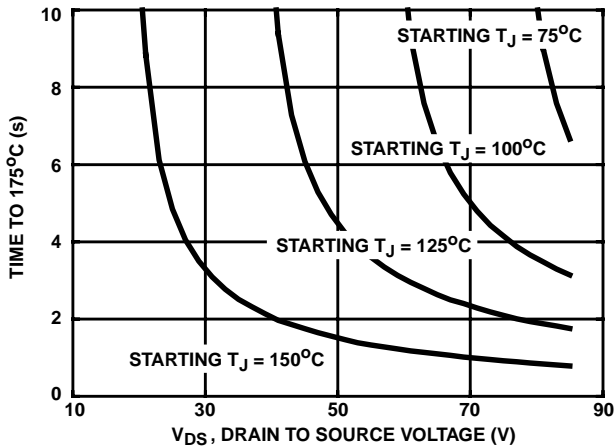


FIGURE 25. TIME TO 175°C IN CURRENT LIMITING  
(HEATSINK THERMAL RESISTANCE = 2°C/W)  
(HEATSINK THERMAL CAPACITANCE = 4J/°C)

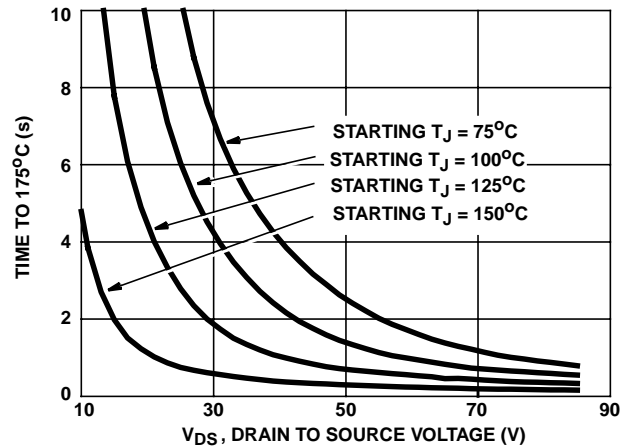


FIGURE 26. TIME TO 175°C IN CURRENT LIMITING  
(HEATSINK THERMAL RESISTANCE = 25°C/W)  
(HEATSINK THERMAL CAPACITANCE = 0.5J/°C)

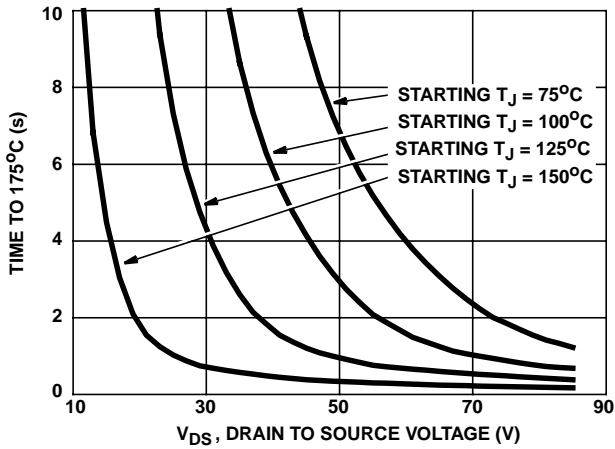


FIGURE 27. TIME TO 175°C IN CURRENT LIMITING  
(HEATSINK THERMAL RESISTANCE = 10°C/W)  
(HEATSINK THERMAL CAPACITANCE = 1.0J/°C)

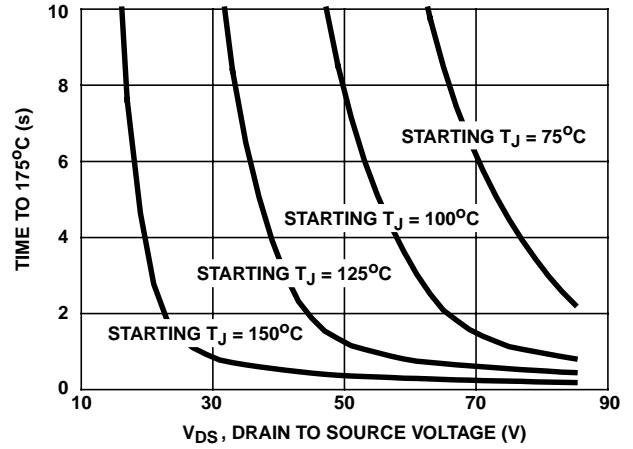


FIGURE 28. TIME TO 175°C IN CURRENT LIMITING  
(HEATSINK THERMAL RESISTANCE = 5°C/W)  
(HEATSINK THERMAL CAPACITANCE = 2.0J/°C)

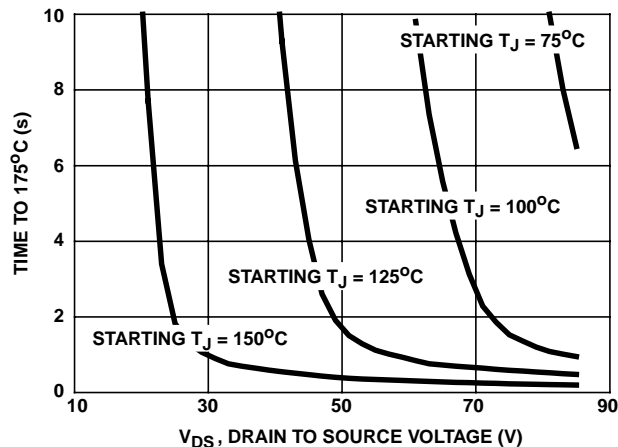


FIGURE 29. TIME TO 175°C IN CURRENT LIMITING  
(HEATSINK THERMAL RESISTANCE = 2°C/W)  
(HEATSINK THERMAL CAPACITANCE = 4J/°C)



**PSPICE Electrical Model**

SUBCKT RLD03N06CLE 2 1 3; rev 4/18/94

CA 12 8 0.547e-9

CB 15 14 0.547e-9

CIN 6 8 0.301e-9

DBODY 7 5 DBDMOD  
 DBREAK 5 11 DBKMOD  
 DESD1 91 9 DESD1MOD  
 DESD2 91 7 DESD2MOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 20 17 18 66.5  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 2.96e-9  
 LSOURCE 3 7 2.96e-9

MOS1 16 6 8 8 MOSMOD M = 0.99  
 MOS2 16 21 8 8 MOSMOD M = 0.01

QCONTROL 20 70 7 QMOD 1

RBREAK 17 18 RBKMOD 1  
 RDRAIN 5 16 RDSMOD 1.123  
 RGATE 9 20 3200  
 RIN 6 8 1e9  
 RSOURCE1 8 70 RDSMOD 1.12  
 RSOURCE2 70 7 RSMOD 2.16  
 RVTO 18 19 RVTOMOD 1

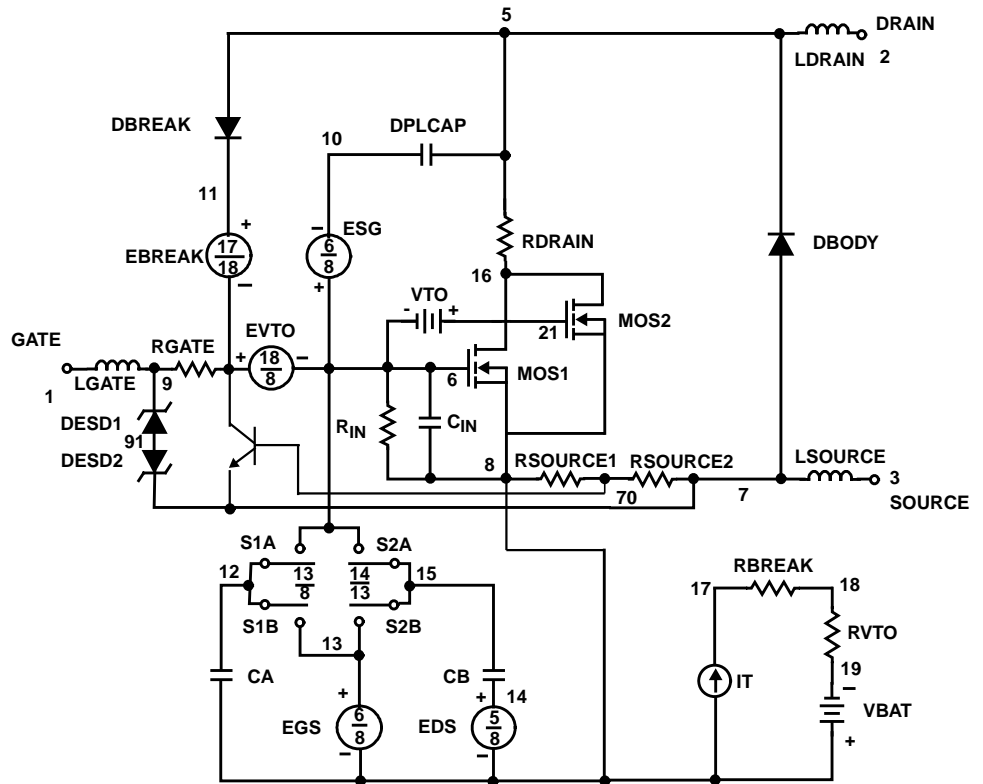
S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1  
 VTO 21 6 0.22

.MODEL DBDMOD D (IS = 7.97e-17 RS = 1.82 TRS1 = 3.91e-3 TRS2 = 1.24e-5 CJO = 3.00e-10 TT = 1.83e-7)  
 .MODEL DBKMOD D (RS = 3150 TRS1 = 0 TRS2 = 0)  
 .MODEL DESD1MOD D (BV = 13.54 TBV1 = 0 TBV2 = 0 RS = 45.5 TRS1 = 0 TRS2 = 0)  
 .MODEL DESD2MOD D (BV = 11.46 TBV1 = -7.576e-4 TBV2 = -3.0e-6 RS = 0 TRS1 = 0 TRS2 = 0)  
 .MODEL DPLCAPMOD D (CJO = 74.2e-12 IS = 1e-30 N = 10)  
 .MODEL MOSMOD NMOS (VTO = 1.67 KP = 3.40 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL QMOD NPN (BF = 5)  
 .MODEL RBKMOD RES (TC1 = 4e-4 TC2 = 1.13e-8)  
 .MODEL RDSMOD RES (TC1 = 6.80e-3 TC2 = 6.5e-6)  
 .MODEL RSMOD RES (TC1 = 2.95e-3 TC2 = -1e-6)  
 .MODEL RVTOMOD RES (TC1 = -2.22e-3 TC2 = -1.95e-6)  
 .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3 VOFF = -1)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1 VOFF = -3)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.85 VOFF = 2.15)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.15 VOFF = -2.85)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records 1991.



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