Data Sheet April 1999 File Number 2252.3

1A, 80V, 0.750 Ohm, Current Limited, N-Channel Power MOSFET

The RLP1N08LE is a semi-smart monolithic power circuit which incorporates a lateral bipolar transistor, two resistors, a zener diode, and a PowerMOS transistor. Good control of the current limiting levels allows use of these devices where a shorted load condition may be encountered. “Logic level” gates allow this device to be fully biased on with only 5V from gate to source. The zener diode provides ESD protection up to 2kV. These devices can be produced on the standard PowerMOS production line.

Formerly developmental type TA09842.

Ordering Information

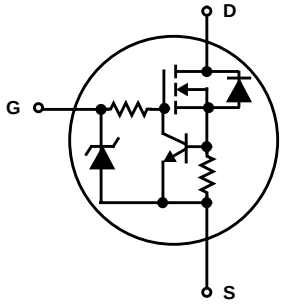
PART NUMBER	PACKAGE	BRAND
RLP1N08LE	TO-220AB	L1N08LE

NOTE: When ordering, use the entire part number.

Features

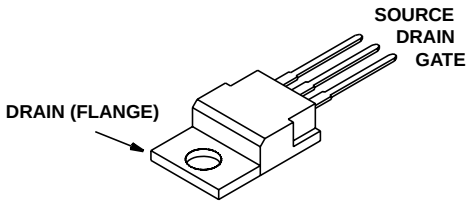
- 1A, 80V
- $r_{DS(ON)} = 0.750\Omega$
- I_{LIMIT} at 150^oC = 1.5A Maximum
- Built-in Current Limiting
- ESD Protected
- Controlled Switching Limits EMI and RFI
- Specified for 150^oC Operation
- Temperature Compensated Spice Model Provided
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RLP1N08LE	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	80	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	80	V
Electrostatic Voltage at 100pF, 1500Ω	ESD	2	kV
Continuous Drain Current	I_D	Self Limited	
Gate to Source Voltage (Reverse Voltage Gate Bias Not Allowed)	V_{GS}	5.5	V
Maximum Power Dissipation	P_D	30	W
Power Dissipation Derating		0.24	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V, Figure 7		80	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA, Figure 8		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V, V_{GS} = 0V	$T_C = 25^oC$	-	-	1	µA
			$T_C = 150^oC$	-	-	50	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = 5V, $T_C = 150^oC$		-	-	50	µA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 1A, V_{GS} = 5V Figure 6	$T_C = 25^oC$	-	-	0.750	Ω
			$T_C = 150^oC$	-	-	1.5	Ω
Limiting Current	$I_{DS(Lim)}$	V_{DS} = 15V, V_{GS} = 5V Figure 3	$T_C = 25^oC$	1.8	-	3	A
			$T_C = 150^oC$	1.1	-	1.5	A
Turn-On Time	$t_{(ON)}$	V_{DD} = 30V, I_D = 1A, V_{GS} = 5V, R_{GS} = 25Ω R_L = 30Ω		-	-	6.5	µs
Turn-On Delay Time	$t_{d(ON)}$			-	-	1.5	µs
Rise Time	t_r			1	-	5	µs
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	7.5	µs
Fall Time	t_f			1	-	5	µs
Turn-Off Time	$t_{(OFF)}$			-	-	12.5	µs
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	4.17	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220AB		-	-	62	$^oC/W$
Electrostatic Voltage	ESD	Human Model (100pF, 1.5kΩ)		2000	-	-	V

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 1A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 1A	-	-	1	ms

NOTES:

2. Pulsed: pulse duration = ≤ 300µs maximum, duty cycle = ≤ 2%.
3. Repititive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

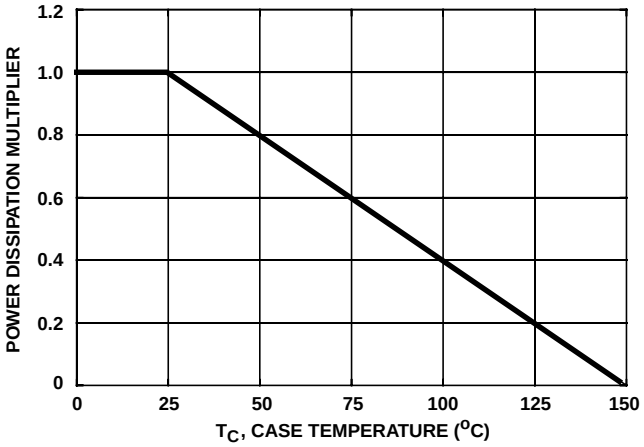


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

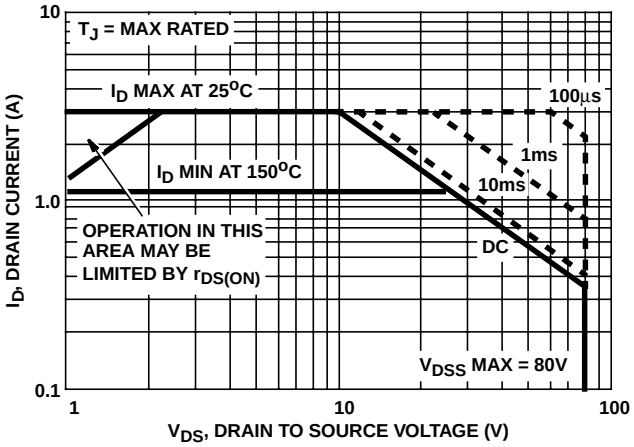


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

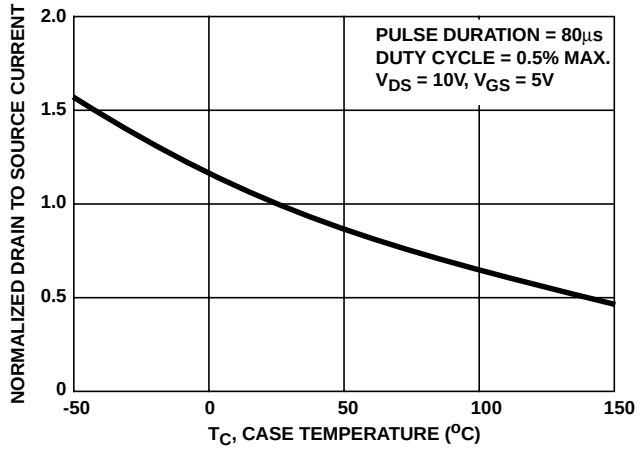


FIGURE 3. NORMALIZED CURRENT LIMIT vs CASE TEMPERATURE

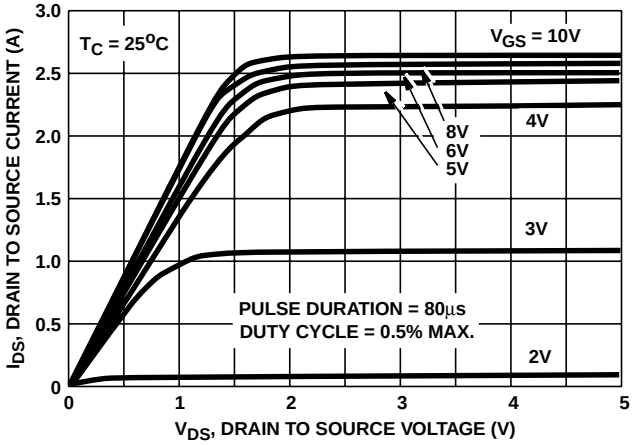


FIGURE 4. SATURATION CHARACTERISTICS

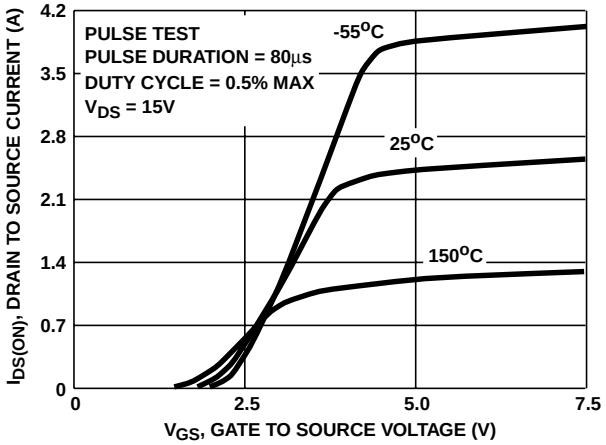


FIGURE 5. TRANSFER CHARACTERISTICS

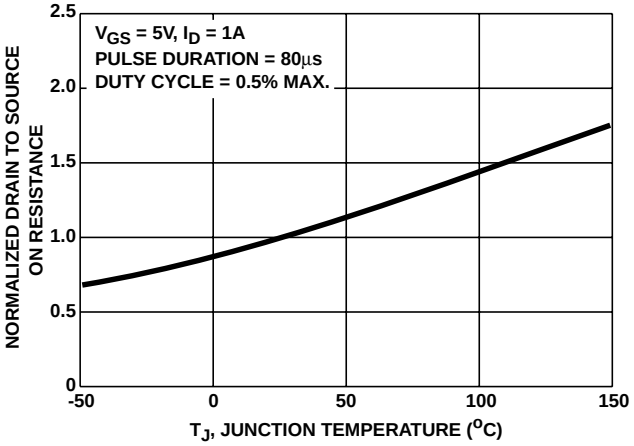


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

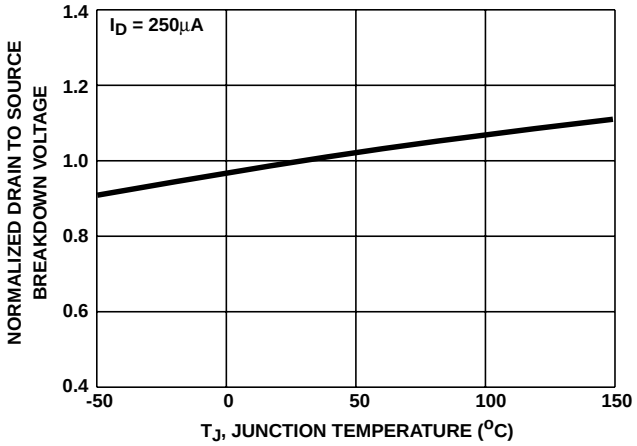


FIGURE 7. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

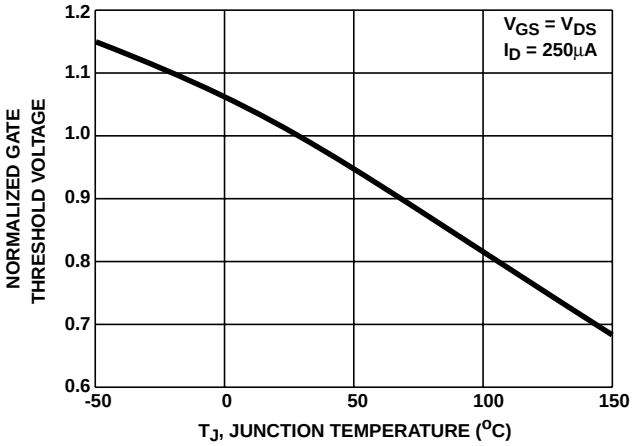


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

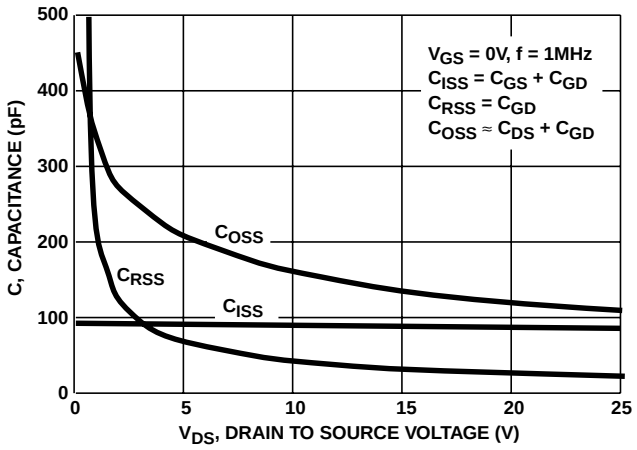


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

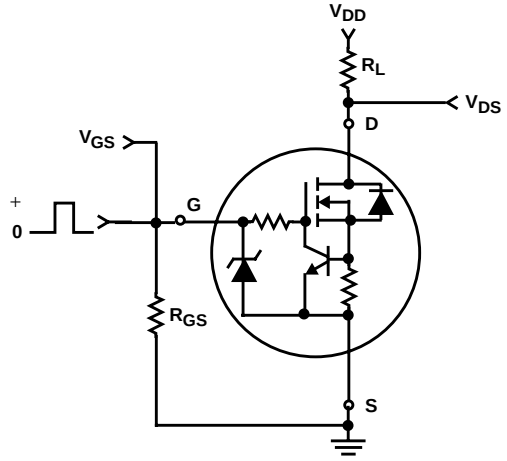


FIGURE 10. SWITCHING TEST CIRCUIT

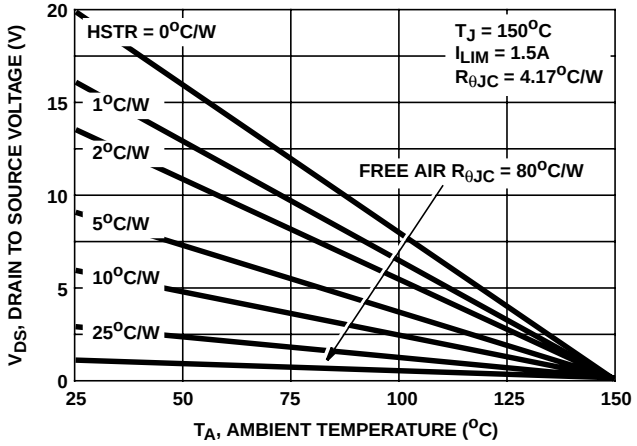
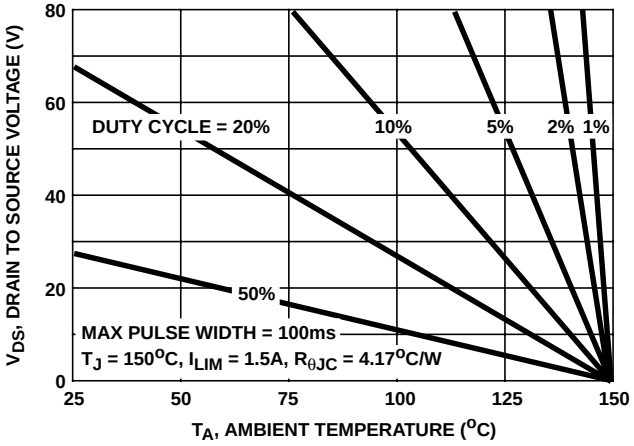


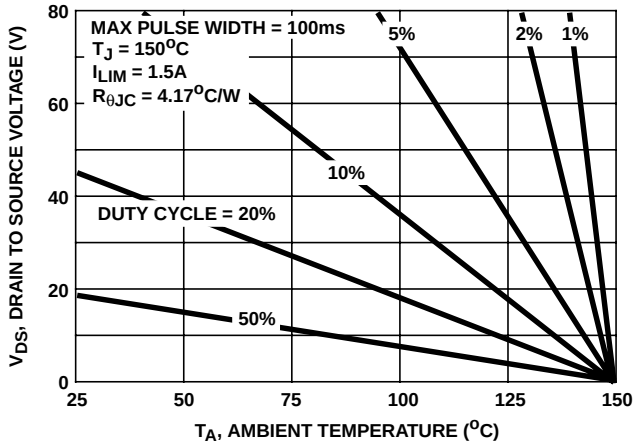
FIGURE 11. DC OPERATION IN CURRENT LIMITING



NOTE: Heatsink thermal resistance = 2^{O}C/W

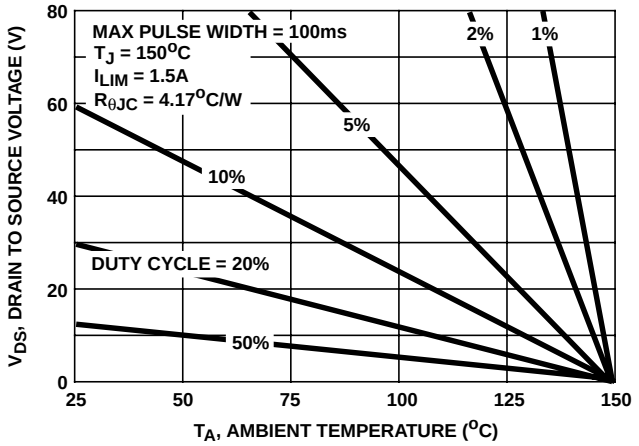
FIGURE 12. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING

Typical Performance Curves Unless Otherwise Specified **(Continued)**



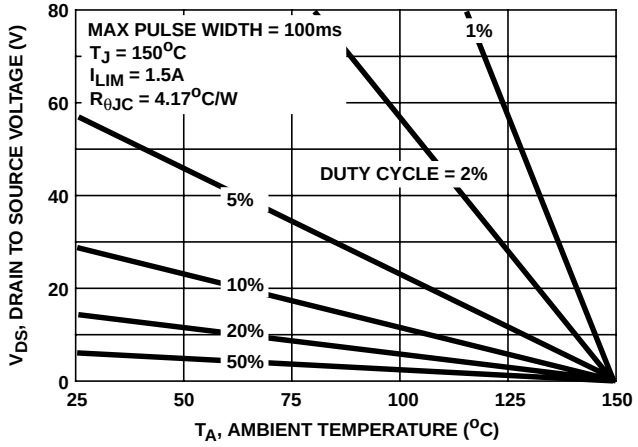
NOTE: Heatsink thermal resistance = 5°C/W

FIGURE 13. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING



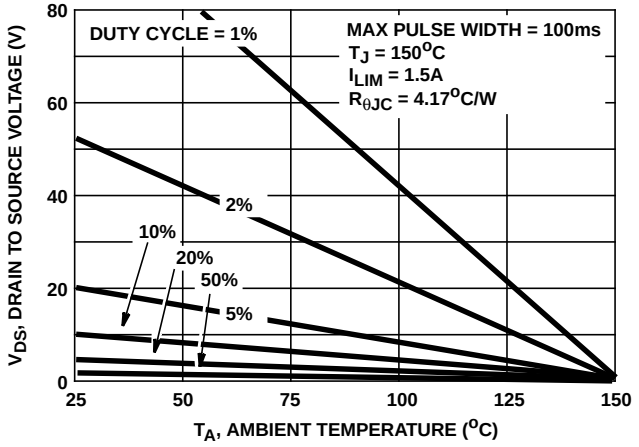
NOTE: Heatsink thermal resistance = 10°C/W

FIGURE 14. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING



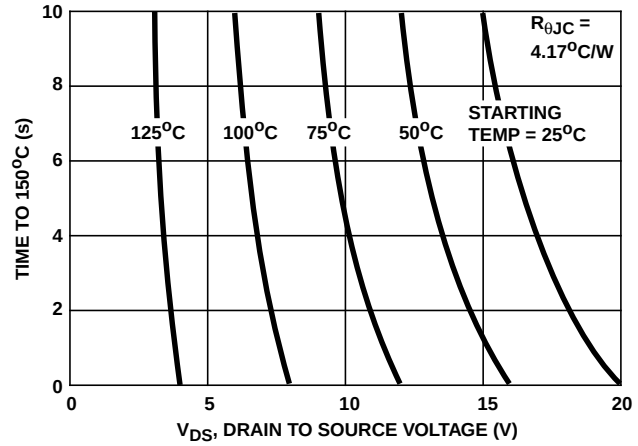
NOTE: Heatsink thermal resistance = 25°C/W

FIGURE 15. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING



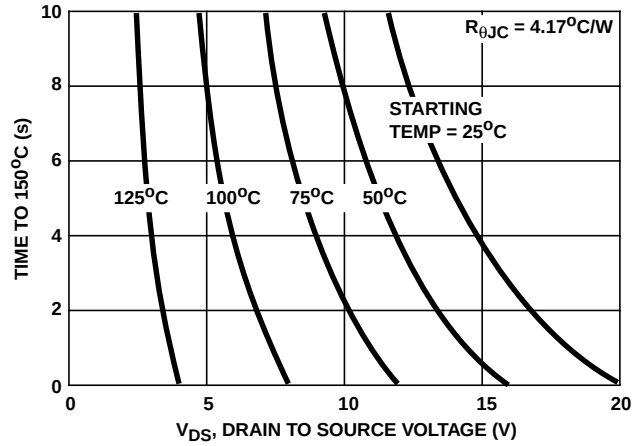
NOTE: No external heatsink.

FIGURE 16. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING



NOTE: Heatsink thermal resistance = 2°C/W
Heatsink thermal capacitance = 4j/°C

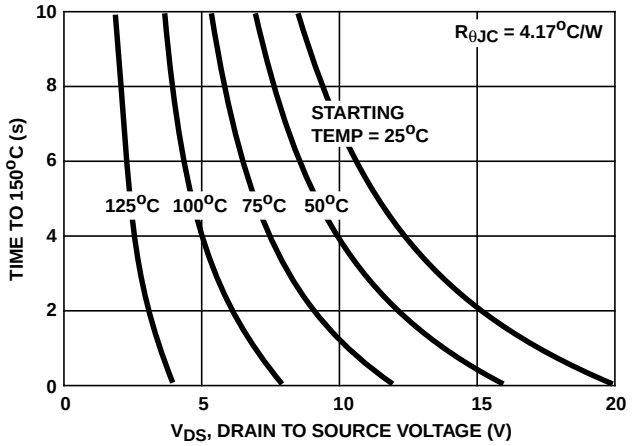
FIGURE 17. TIME TO 150°C IN CURRENT LIMITING



NOTE: Heatsink thermal resistance = 5°C/W
Heatsink thermal capacitance = 2j/°C

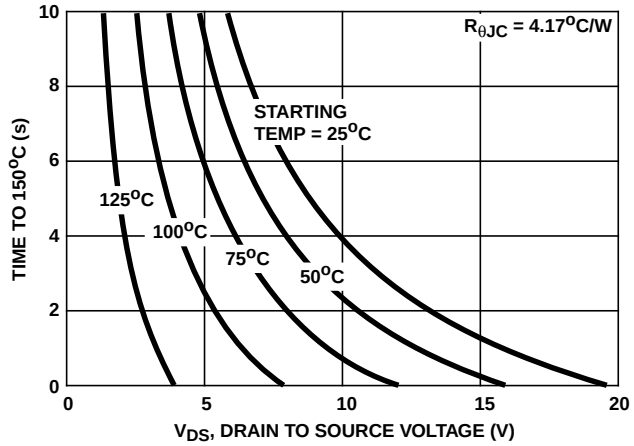
FIGURE 18. TIME TO 150°C IN CURRENT LIMITING

Typical Performance Curves Unless Otherwise Specified **(Continued)**



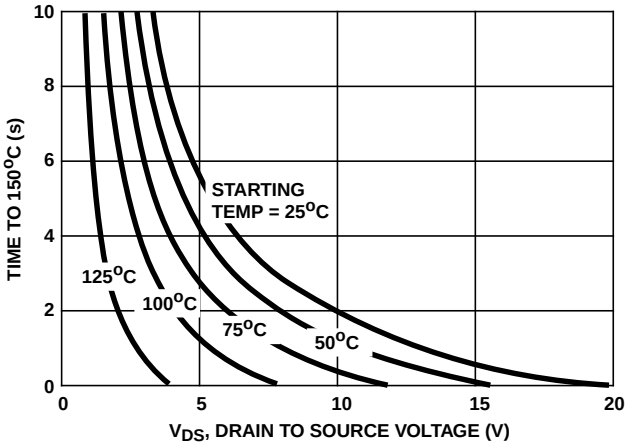
NOTE: Heatsink thermal resistance = 10°C/W
Heatsink thermal capacitance = 1j/°C

FIGURE 19. TIME TO 150°C IN CURRENT LIMITING



NOTE: Heatsink thermal resistance = 25°C/W
Heatsink thermal capacitance = 0.5j/°C

FIGURE 20. TIME TO 150°C IN CURRENT LIMITING



NOTE: No external heatsink.

FIGURE 21. TIME TO 150°C IN CURRENT LIMITING

Temperature Dependence of Current Limiting and Switching Speed

The RLP1N08LE is a monolithic power device which incorporates a logic level PowerMOS transistor with a resistor in series with the source. The base and emitter of a lateral bipolar transistor is connected across this resistor, and the collector of the bipolar transistor is connected to the gate of the PowerMOS transistor. When the voltage across the resistor reaches the value required to forward bias the emitter base junction of the bipolar transistor, the bipolar transistor “turns on”. A series resistor is incorporated in series with the gate of the PowerMOS transistor allowing the bipolar transistor to drive the gate of the PowerMOS transistors to a voltage which just maintains a constant current in the PowerMOS transistor. Since both the resistance of the resistor in series with the PowerMOS transistor source and voltage required to forward bias the base emitter junction of the bipolar transistor vary with the temperature, the current at which the device limits is a function of temperature. This dependence is shown in figure 3.

The resistor in series with the gate of the PowerMOS transistor results in much slower switching than in most PowerMOS transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable, and a minimum as well as maximum fall time is given in the device characteristics for this type.

DC Operation of the RLP1N08LE

The limit of the drain to source voltage for operation in current limiting on a steady state (DC) basis is shown as Figure 11. The dissipation in the device is simply the applied drain to source voltage multiplied by the limiting current. This device, like most Power MOSFET devices today, is limited to $150^{o}C$. The maximum voltage allowable can, therefore be expressed as:

$$V_{DS} = \frac{(150^{o}C - T_{AMBIENT})}{I_{LIM} \times (R_{\theta JC} + R_{\theta CA})} \quad \text{(EQ. 1)}$$

Duty Cycle Operation of the RLP1N08LE

In many applications either the drain to source voltage or the gate drive is not available 100% of the time. The copper header on which the RLP1N08LE is mounted has a very large thermal storage capability, so for pulse widths of less than 100 milliseconds, the temperature of the header can be considered a constant case temperature calculated simply as:

$$T_C = (V_{DS} \times I_D \times D \times R_{\theta CA}) + T_{AMBIENT} \quad \text{(EQ. 2)}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to $150^{o}C$ and using the TC calculated above, the expression for maximum V_{DS} under duty cycle operation is:

$$V_{DS} = \frac{150 - T_C}{I_{LIM} \times D \times R_{\theta JC}} \quad \text{(EQ. 3)}$$

These values are plotted as Figures 12 thru 16 for various heat sink thermal resistances.

Limited Time Operations of the RLP1N08LE

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as figures 17 thru 21 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified $150^{o}C$ junction termperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

Spice Model (RLP1N08LE)

```
.SUBCKT RLP1N08LE  2  1  3;  rev 09/16/91
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=1.7  KP=2.1  IS=1e-30  N=10  TOS=1  L=1u  W=1u)
Vto  21  6  0.33
Rsource  8  7  RDSMOD  0.28
Rdrain  5  16  RDSMOD  0.2
.MODEL RDSMOD RES (TC1=7.54E-3  TC2=2.23E-5)
.MODEL RVTOMOD RES (TC1=-2.23E3  TC2=-5.29E-7)
.MODEL RVTOMOD2 RES (TC1=0  TC2=0)
Ebreak 11  7  17  18  107.3
.MODEL RBKMOD RES (TC1=1.11E-3  TC2=-6.83E-7)
.MODEL DBKMOD D (RS=2.78  TRS1=-8.88E-3  TRS2=2.55E-5)
.MODEL DBDMOD D (IS=9.91E-15  RS=3.01E-1  TRS1=3.79E-3  TRS2=1.11E-6  +CJO=4.32E-10  TT=2E-7
Cin  6  8  3.75E-10
Ca  12  8  6.5E-10
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-3  VOFF=-1)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1  VOFF=-3)
.MODEL DPLCAPMOD D (CJO=2E-10  IS=1e-30  N=10)
Cb  12  14  6.5E-10
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1.65  VOFF=3.35)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=3.35  VOFF=-1.65)
Rgate  9  20  4.48E3
Lgate  1  9  9.5E-10
Ldrain  2  5  2.5E-9
Lsource  3  7  2.5E-9
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
MOS1  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
*Current Limiting Control Section
.MODEL RSMOD RES (TC1=3.2E-3)
Q Control 20  8  7  QMOD  10
.MODEL QMOD NPN (BF=5  VJE=0.5)
*ESD Protection
DESD  7  9  DESMOD
.MODEL DESMOD D(BV=7.185  TBV1=3.5E-4  TBV2=2.2E-6)
.ENDS
```

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