RM333X Series
32-256Kbit Ultra Low Power Non-volatile Serial Memory - SPI Bus

ADVANCE DATASHEET

Features

- Memory array: 32-256Kbit EEPROM-compatible non-volatile serial memory
- Multiple supply voltages for minimum power consumption
  - V_{DDC}: 1.17-1.23V
  - V_{DDIO}: 3.0-3.6V
- Serial peripheral interface (SPI) compatible
  -Supports SPI modes 0 and 3
- 1.0 MHz maximum clock rate
- Flexible Programming
  - Byte/Page Program (1 to 32 or 64Bytes)
  - Page size: 32 or 64 Bytes
- Ultra Low Energy Word Write
  -32 bit Word Write consuming 50 nJ
- Low power consumption
  -10 µA active Read current @ 500 kbit/s (Typical)
  -10 µA active Write current @ 10 kbit/s (Typical)
  -50 nA Ultra-Deep Power-Down current
- Auto Ultra-Deep Power-Down
  -Device can enter Ultra-Deep Power-Down automatically after finishing a Write operation
- Self-timed write cycles
- Hardware reset
- 8-lead SOIC package
- RoHS-compliant and halogen-free packaging
- Data Retention: 10 years
- Based on Adesto's proprietary CBRAM® technology

Description

The Adesto® RM333X Series is a 32-256Kbit, serial memory device that utilizes Adesto's CBRAM® resistive technology.

The memory device is optimized for low power operation offering lowest available power for data-transfer, power-down, and writing. In order to efficiently optimize power consumption, the device makes use of two supplies V_{DDC}, and V_{DDIO}. The two V_{DDIO} supply signals must be tied together to supply write and I/O voltage (see Figure 5-2). Read power is supplied from the V_{DDC} and the device consumes less than10µW at 500Kbit/s.

The RM333X Series is accessed through a 4-wire SPI interface consisting of a Serial Data Input (SDI), Serial Data Output (SDO), Serial Clock (SCK), and Chip Select ($\overline{CS}$). The maximum clock (SCK) frequency in read mode is 1.0MHz.

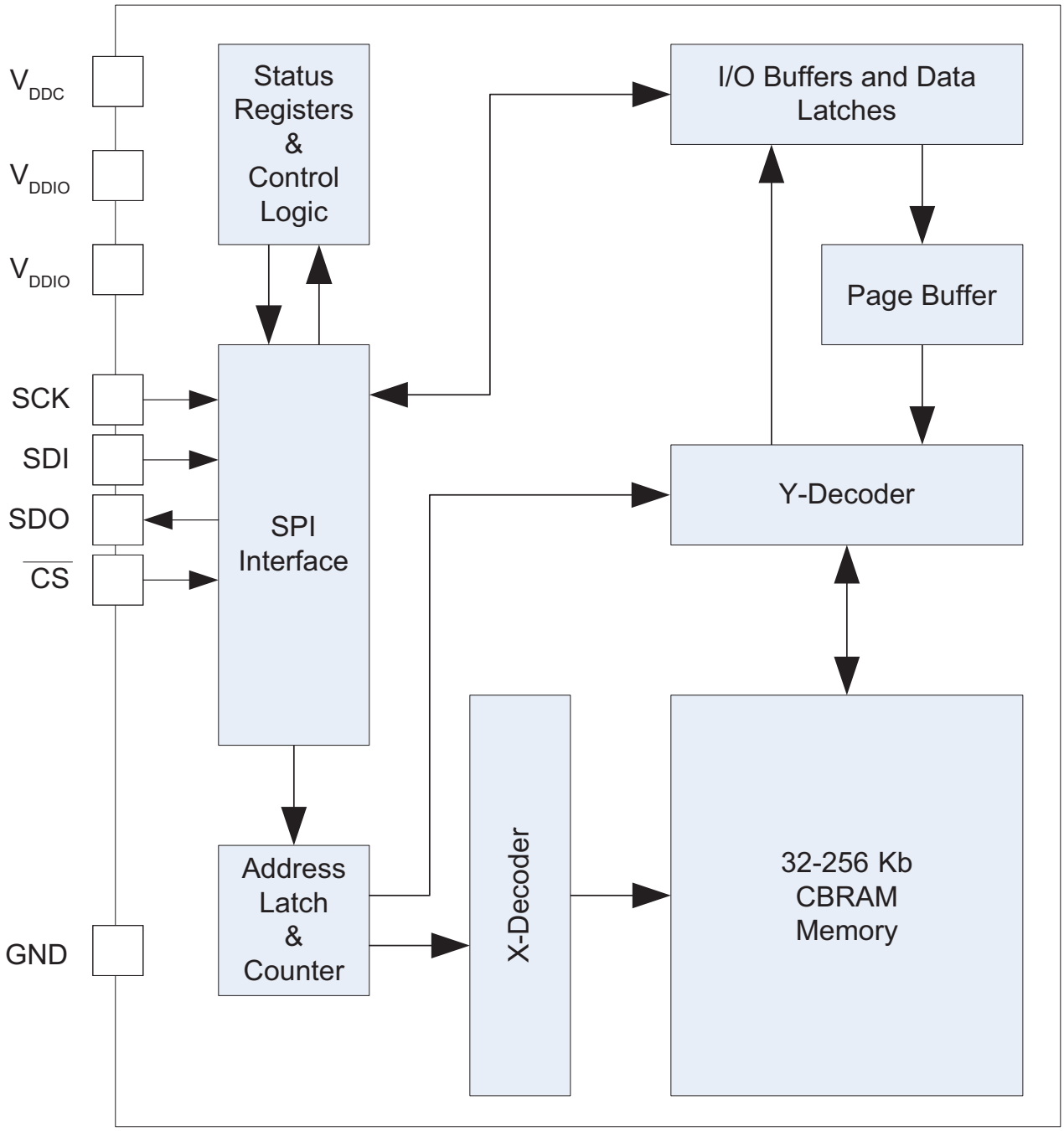
The device supports direct write eliminating the need to pre-erase. Writing into the device can be done from 1 to 32 or 64 bytes at a time and consumes less than 40uW. All writing is internally self-timed.

The device has both Byte Word Write and Page Write capability. Page Write is from 1 to 32 or 64 bytes. The 32 bit word Write operation of CBRAM consumes only 10% of the energy consumed by a 32 bit word Write operation of EEPROM devices of similar size.

Both random and sequential reads are available. Sequential reads are capable of reading the entire memory in one operation.

1. Block Diagram

Figure 1-1. Block Diagram



2. Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings[1]

Parameter	Specification
Operating ambient temp range	-40°C to +105°C
Storage temperature range	-65°C to +105°C
Input supply voltage, V_{DDC} to GND	- 0.3V to 1.25V
Input supply voltage, V_{DDIO} to GND	-0.3V to 3.6V
Voltage on any pin with respect to GND	-0.5V to (V_{DDIO}+ 0.5V)
ESD protection on all pins (Human Body Model)	1kV
Junction temperature	105°C
DC output current	5mA

1. CAUTION: Stresses greater than Absolute Maximum Ratings may cause permanent damage to the devices. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in other sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may reduce device reliability.

3. Electrical Characteristics

3.1 DC Operating Characteristics

Applicable over recommended operating range: T_A = -40°C to +85° C, V_{DDIO} = 3.0V - 3.6V, V_{DDC} = 1.17-1.23V, C_L = 3pF (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDC}	Core Supply Range (1) (2)		1.17	1.20	1.23	V
V_{DDIO}	I/O Supply Range(1)(2)		3.0	3.3	3.6	V
I_{DD1}	Supply current, Read	V_{DDC} = 1.2V @ 500 kbit/s		5.5		µA
		V_{DDIO} = 3.3V @ 500 kbit/s		4.5		µA
I_{DD2}	Supply Current, Standby	V_{DDC} = 1.2V		1.0	10.0	µA
		V_{DDIO} = 3.3V		1.0	10.0	µA
I_{DD3}	Supply Current, Write	V_{DDC} = 1.2V @ 10 kbit/s		4.5		µA
		V_{DDIO} = 3.3V @ 10 kbit/s		10		µA
I_{DD5}	Supply Current, Ultra-Deep Power-Down Mode 1	V_{DDC} = 1.2V		0.020		µA
		V_{DDIO} = 3.3V		0.05	0.50	µA
I_{DD6} (3)	Supply Current, Ultra-Deep Power-Down Mode 2	V_{DDC} = 0V		0		µA
		V_{DDIO} = 0V		0.05	0.10	µA
I_{IL}	Input Leakage	SCK, SDI, $\overline{CS}$ V_{IN}=0V to V_{DDIO}			1	µA
I_{OL}	Output Leakage	SCK, SDI, $\overline{CS}$ =V_{DDIO} V_{IN}=0V to V_{DDIO}			1	µA
V_{IL}	Input Low Voltage	SCK, SDI, $\overline{CS}$	-0.3		V_{DDIO} x 0.3	V
V_{IH}	Input High Voltage	SCK, SDI, $\overline{CS}$	V_{DDIO} x 0.7		V_{DDIO} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{DDIO} - 0.2			V

1. There are no brownout or under voltage detectors. Users must ensure that V_{DDC} and V_{DDIO} are within operating range for correct operation of the device. Failure to follow this instruction may cause damage to the device.
2. A low ESR 100nF capacitor should be connected between each supply pin and GND (see Figure 5-2).
3. The Ultra-Deep Power Down Mode can be used as an extra protection mechanism against inadvertent program and erase operations.

3.2 AC Operating Characteristics

Applicable over recommended operating range: T_A = -40°C to +85° C, V_{DDIO} = 3.0V - 3.6V, V_{DDC} = 1.17-1.23V, C_L = 3pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Clock Frequency for Read Mode	0		1.0	MHz
t_{RI}	SCK Input Rise Time			1	µs
t_{FL}	SCK Input Fall Time			1	µs
t_{SCKH}	SCK High Time	7.5			ns
t_{SCKL}	SCK Low Time	7.5			ns
t_{CS}	$\overline{CS}$ High Time	100			ns
t_{CL}	$\overline{CS}$ Low Time	100			ns
t_{CSS}	$\overline{CS}$ Setup Time	10			ns
t_{CSH}	$\overline{CS}$ Hold Time	10			ns
t_{DS}	Data In Setup Time	4			ns
t_{DH}	Data In Hold Time	4			ns
t_{OV}	Output Valid			6.5	ns
t_{OH}	Output Hold Time Normal Mode	0			ns
t_{DIS}	Output Disable Time			100	ns
t_{PW}	Page Write Cycle Time, 32/64 byte page		18/36		ms
t_{BP}	4 Byte Write Cycle Time		2.2		ms
t_{PUD}	V_{cc} Power-up Delay			75	µs
t_{XUDPD}	Exit Ultra-Deep Power-Down Time	200			µs
t_{RDPD}	Chip Select High to Standby Mode			8	µs
C_{IN}	SCK, SDI, $\overline{CS}$, V_{IN}=0V			6	pF
C_{OUT}	SDO V_{IN}=0V			3	pF
Endurance		10000			Write Cycles
Retention		10			Years

1. There are no brownout or under voltage detectors. Users must ensure that V_{DDC} and V_{DDIO} are within operating range for correct operation of the device. Failure to follow this instruction may cause damage to the device.

3.3 AC Test Conditions

AC Waveform	Timing Measurement Reference Level	
V_{LO} = 0.2V	Input	0.5 V_{DDIO}
V_{HI} = V_{DDIO} = 1.8V	Output	0.5 V_{DDIO}
C_L = 3pF (for max1.0 MHz SCK)		

4. Timing Diagrams

Figure 4-1. Synchronous Data Timing

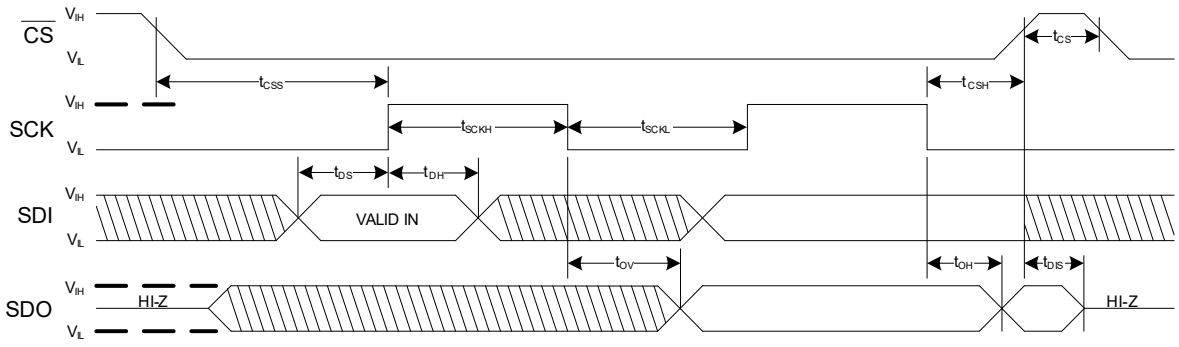
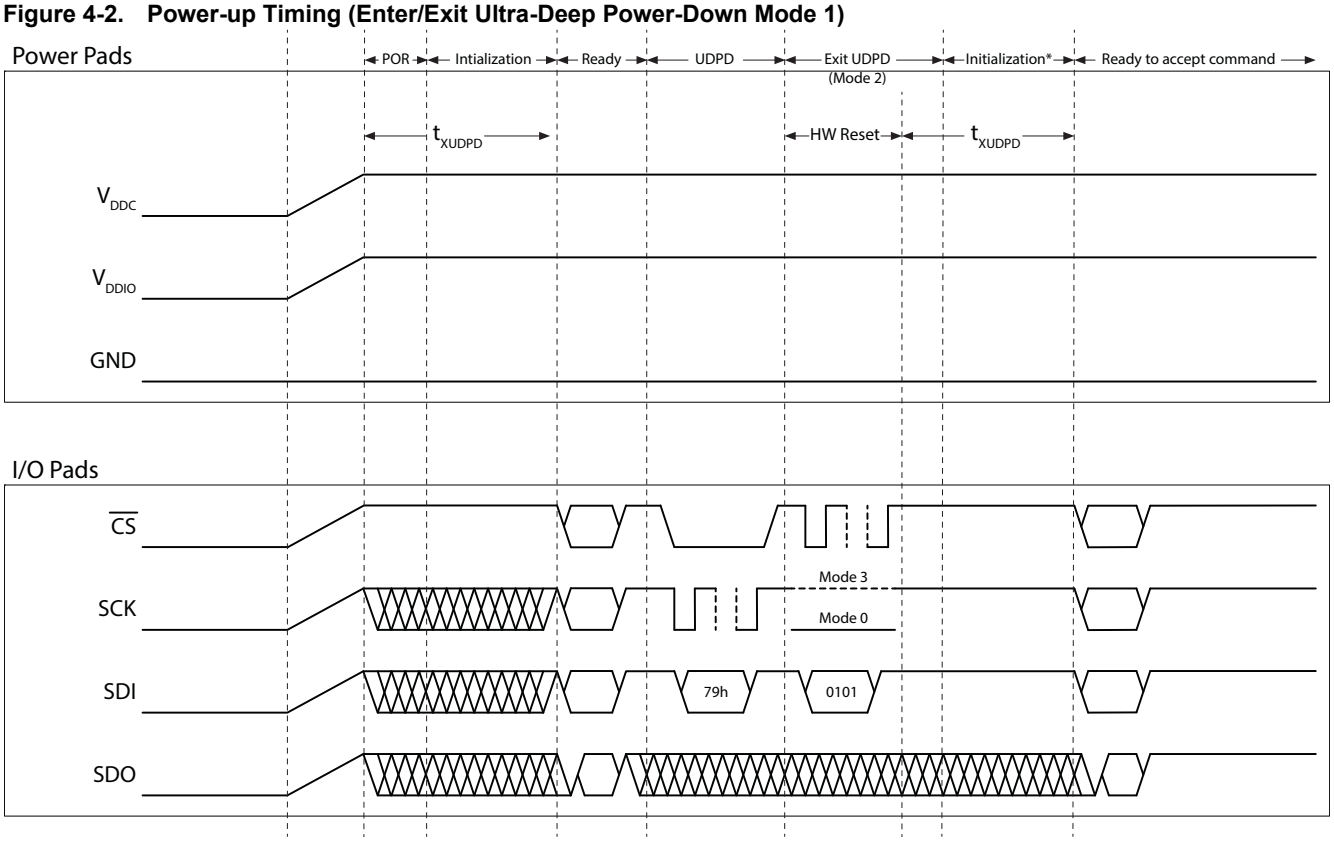
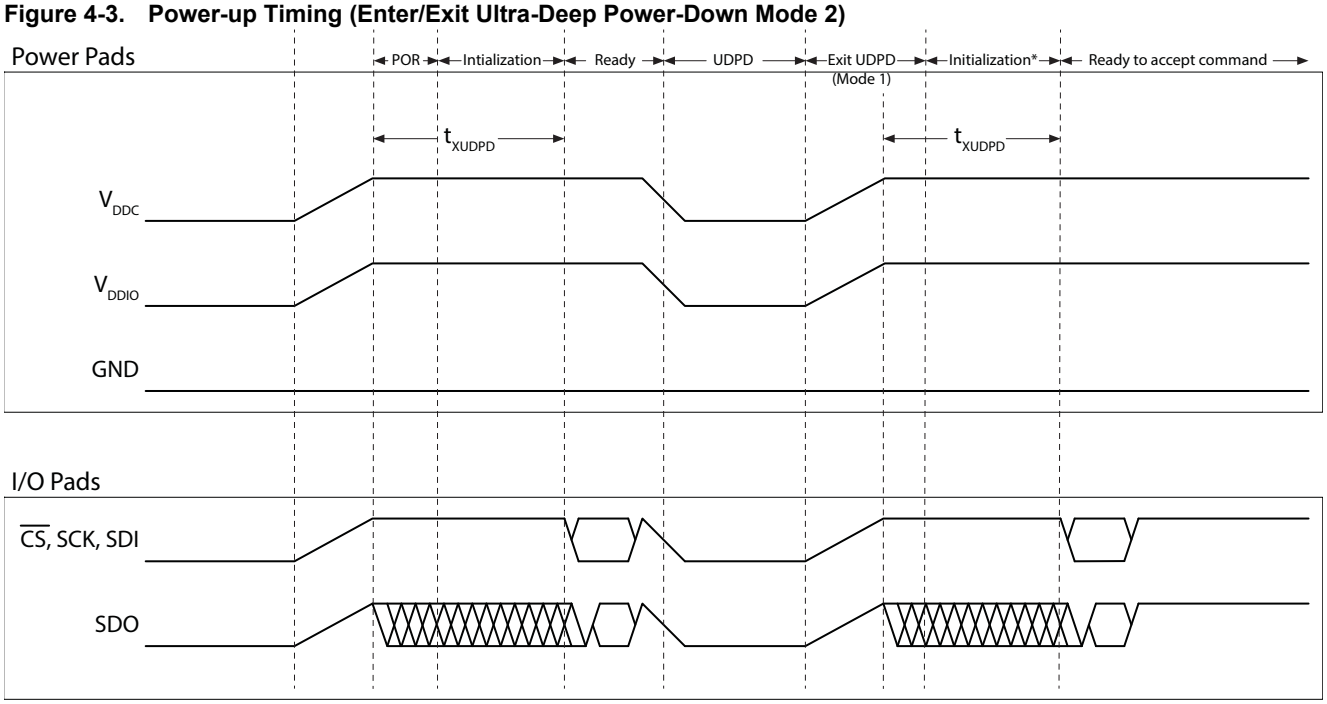


Figure 4-2. Power-up Timing (Enter/Exit Ultra-Deep Power-Down Mode 1)



Note: V_{DDIO} and V_{DDC} must be powered up together. In order to READ or WRITE both voltages are required.

Figure 4-3. Power-up Timing (Enter/Exit Ultra-Deep Power-Down Mode 2)



5. Pin Descriptions and Pin-out

Table 5-1. Pin Descriptions

Mnemonic	Pin Number	Pin Name	Description
$\overline{CS}$	1	Chip Select	Making $\overline{CS}$ low activates the internal circuitry for device operation. Making $\overline{CS}$ high deselects the device and switches into standby mode to reduce power. When the device is not selected ($\overline{CS}$ high), data is not accepted via the Serial Data Input pin (SDI) and the Serial Data Output pin (SDO) remains in a high-impedance state. To minimize power consumption, the master should ensure that this pin always has a valid logic level.
SDO	2	Serial Data Out	Sends read data or status on the falling edge of SCK.
V_{DDC}	3	Core Power	Power Supply for digital controller and low voltage logic. A low ESR 100nF capacitor should be connected between each supply pin and GND.
GND	4	Ground	
SDI	5	Serial Data In	Device data input; accepts commands, addresses, and data on the rising edge of SCK. To minimize power consumption, the master should ensure that this pin always has a valid logic level.

Mnemonic	Pin Number	Pin Name	Description
SCK	6	Serial Clock	Provides timing for the SPI interface. SPI commands, addresses, and data are latched on the rising edge on the Serial Clock signal, and output data is shifted out on the falling edge of the Serial Clock signal. To minimize power consumption, the master should ensure that this pin always has a valid logic level.
V_{DDIO}	7	I/O and Write Power	I/O and Write Power Supply. A low ESR 100nF capacitor should be connected between each supply pin and GND (see Figure 5-2).
V_{DDIO}	8	I/O and Write Power	I/O and Write Power Supply. A low ESR 100nF capacitor should be connected between each supply pin and GND (see Figure 5-2).

Figure 5-1. Pinout (Top View)

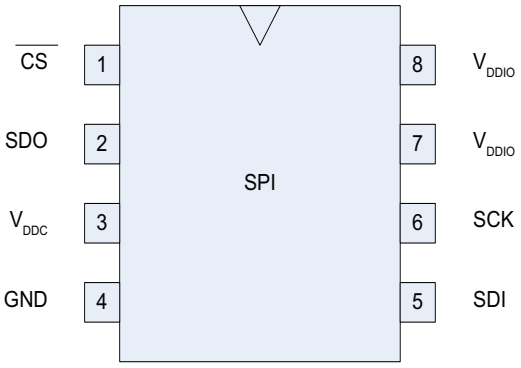
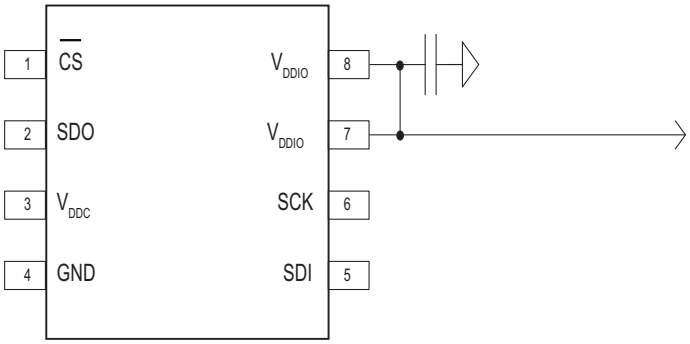


Figure 5-2. Suggested Signal Connection for Write Power Supply (Top View)

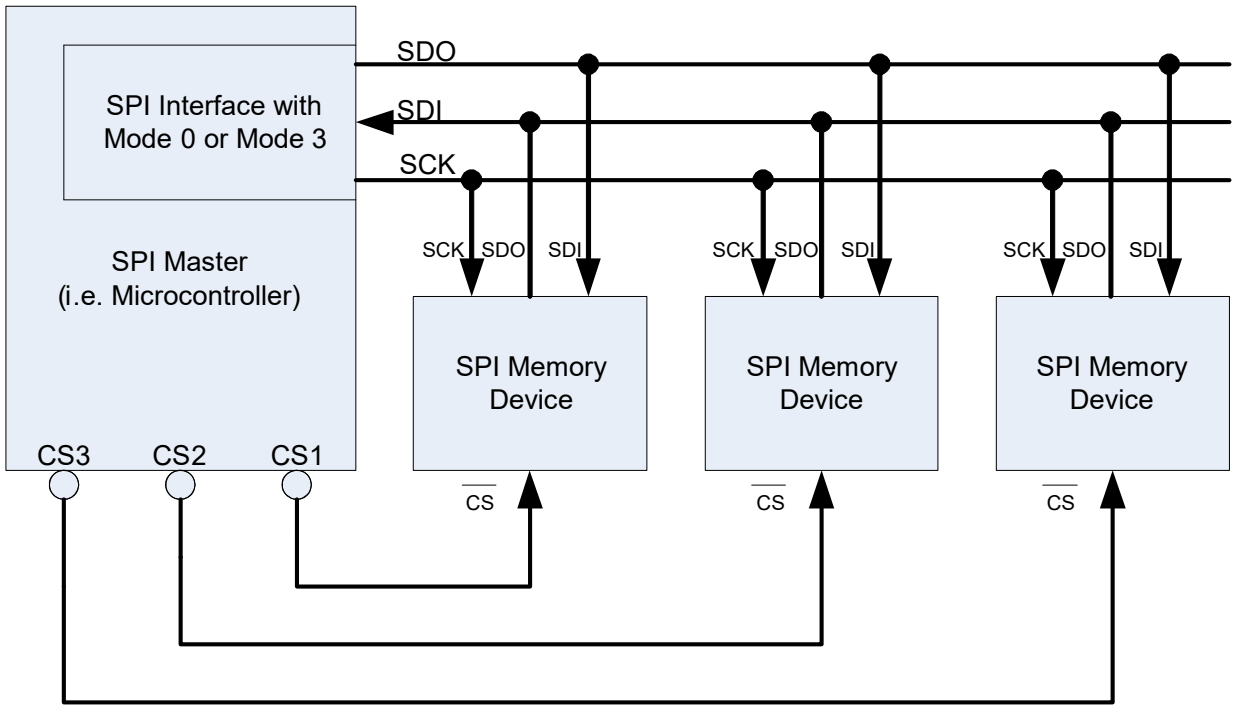


Note: The two V_{DDIO} supply signals must be tied together to supply write and I/O voltage

6. SPI Modes Description

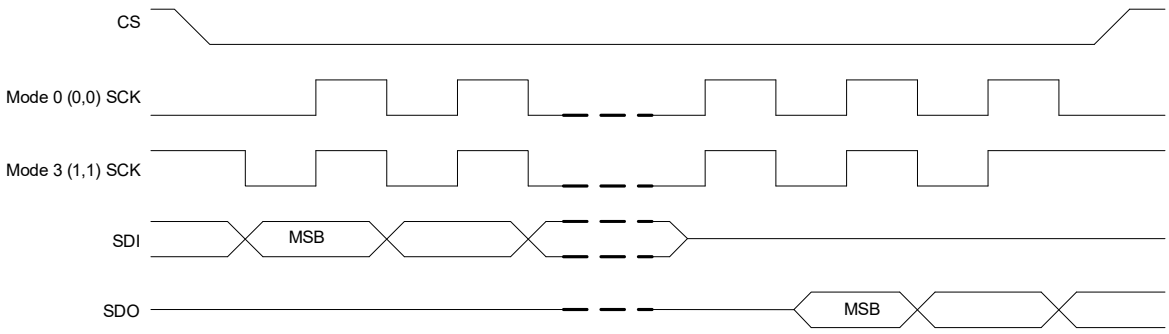
Multiple Adesto SPI devices can be connected onto a Serial Peripheral Interface (SPI) serial bus controlled by an SPI master, such as a microcontroller, as shown in Figure 6-1.

Figure 6-1. Connection Diagram, SPI Master and SPI Slaves



The Adesto RM333X Series supports two SPI modes: Mode 0 (0, 0) and Mode 3 (1, 1). The difference between these two modes is the clock polarity when the SPI master is in standby mode ($\overline{CS}$ high). In Mode 0, the Serial Clock (SCK) stays at 0 during standby. In Mode 3, the SCK stays at 1 during standby. An example sequence for the two SPI modes is shown in Figure 6-2. For both modes, input data (on SDI) is latched in on the rising edge of Serial Clock (SCK), and output data (SDO) is available beginning with the falling edge of Serial Clock (SCK).

Figure 6-2. SPI Modes



7. Registers

7.1 Instruction Register

The Adesto RM333X Series uses a single 8-bit instruction register. The instructions and their operation codes are listed in Table 7-1. All instructions, addresses, and data are transferred with the MSB first, and begin transferring with the first low-to-high SCK transition after the $\overline{CS}$ pin goes low.

Table 7-1. Device Operating Instructions

Instruction	Description	Operation Code	Address Cycles	Dummy Cycles	Data Cycles
WRSR	Write Status Register	01H	0	0	1
WR	Write data to memory array	02H	2	0	1 to 32
READ	Read data from memory array	03H	2	0	1 to ∞
WRDI	Write Disable	04H	0	0	0
RDSR	Read Status Register	05H	0	0	1 to ∞
WREN	Write Enable	06H	0	0	0
WRSR2	Write Status Register2	31H	0	0	1
UDPD	Ultra-Deep Power-Down	79H	0	0	0

7.2 Status Register Byte 1

The Adesto RM333X Series uses a 2-byte Status Register. The Write In Progress (WIP) and Write Enable (WEL) status of the device can be determined by reading the first byte of this register. The non-volatile configuration bits are also in the first byte. The Status Register can be read at any time, including during an internally self-timed write operation.

The Status Register Byte 1 format is shown in Table 7-2. The Status Register Byte 1 bit definitions are shown in Table 7-3.

Table 7-2. Status Register Byte 1 Format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SRWD	0	0	0	BP1	BP0	WEL	WIP

Table 7-3. Status Register Byte 1 Bit Definitions

Bit	Name	Description	R/W	Non-Volatile Bit
0	WIP	**Write In Progress** “0” indicates the device is ready “1” indicates that the program/erase cycle is in progress and the device is busy	R	No
1	WEL	**Write Enable Latch** “0” Indicates that the device is disabled “1” indicates that the device is enabled	R/W	No
2	BP0	Block Protection Bits. "0" indicates the specific blocks are not protected. "1" indicates that the specific blocks are protected.	R/W	Yes
3	BP1			
4	UDPD	**Ultra-Deep Power-Down Status.** Read as “0” if device is in Standby or in an active read/write operation, Read as “1” if device is in Ultra-Deep Power-Down. Reading this bit after power-up or after exiting Ultra-Deep Power-Down will indicate when the device is ready for operation.	R	No
5	N/A	Reserved. Read as “0”	N/A	No
6	N/A	Reserved. Read as “0”	N/A	No
7	SRWD	See Table 8-1.	R/W	Yes

7.3 Status Register Byte 2

The Adesto RM333X Series uses the second byte in the Status Register to hold volatile configuration bits. The Status Register Byte 2 format is shown in table Table 7-4. The Status Register Byte 2 bit definitions are shown in table Table 7-5.

Table 7-4. Status Register Byte 2 Format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	SLOWOSC	AUDPD

Table 7-5. Status Register Byte 2 Bit Definitions

Bit	Name	Description	R/W	Non-Volatile Bit
0	AUDPD	**Auto Ultra-Deep Power-Down Mode after Write Operation** “1” specifies that the device will enter the Ultra-Deep Power-Down mode after a Write operation is completed. “0” specifies that the device will enter the Standby mode after a Write operation is completed.	W	No
1	SLOWOSC	**Slow Oscillator During Write Operation** "1" specifies that during the self-times Write operation the device will periodically slow down on-chip oscillator. "0" specifies that during the self-times Write operation the device will not slow down on-chip oscillator	W	No
2	N/A	Reserved. Read as “0”	N/A	No

Bit	Name	Description	R/W	Non-Volatile Bit
3	N/A	Reserved. Read as “0”	N/A	No
4	N/A	Reserved. Read as “0”	N/A	No
5	N/A	Reserved. Read as “0”	N/A	No
6	N/A	Reserved. Read as “0”	N/A	No
7	N/A	Reserved. Read as “0”	N/A	No

8. Write Protection

The Adesto RM333X Series has two protection modes: Hardware write protection, and software write protection in the form of the SRWD, WEL, BP0, and BP1 bits in the Status Register.

8.1 Hardware Write Protection

There is one hardware write protection feature:

- All write instructions must have the appropriate number of clock cycles before $\overline{CS}$ goes high or the write instruction will be ignored.
- The Status Register Byte1 contains the BP[1:0] bits which are used to protect pre-defined regions in the Memory Array. The SRWD bit is used to prevent write access to the Status Register Byte1 to permanently set the Block Protection status. This is a non-volatile bit, and once the user sets it to 1, the Status Register Byte1 is permanently locked.

Table 8-1. Hardware Write Protection on Status Register

SRWD	Status Register
0	Writable. User can write to the Status Register Byte1.
1	Protected.Status Register Byte1 is locked.

8.2 Software Write Protection

There are two software write protection features:

- Before any program, erase, or write status register instruction, the Write Enable Latch (WEL) bit in the Status Register must be set to a one by execution of the Write Enable (WREN) instruction. If the WEL bit is not enabled, all program, erase, or write register instructions will be ignored.
- The Block Protection bits (BP0 and BP1) allow a part or the whole memory area to be write protected.

See Table 8-2.

Table 8-2. Block Write Protect Bits

BP1	BP0	Protected Region	RM333X Series	
			Protected Address	Protected Area Size
0	0	None	None	0

BP1	BP0	Protected Region	RM333X Series	
0	1	Top ¼	6000-7FFF	8K bytes
1	0	Top ½	4000-7FFF	16K bytes
1	1	All	0-7FFF	All

9. Reducing Energy Consumption

In normal operation, when the device is idle, ($\overline{CS}$ is high, no Write or Erase operation in progress), the device is in Standby Mode, waiting for the next command. To reduce device energy consumption, Ultra-Deep Power-Down modes may be used.

To minimize power consumption, the master should ensure that the SCK, SDI and CS pins always has a valid logic level, these pins should not be left floating when the device is in Standby or Ultra-Deep Power-Down modes.

9.1 Ultra-Deep Power-Down mode

The Ultra-Deep Power-Down mode allows the device to further reduce its energy consumption compared to the existing Standby mode by shutting down additional internal circuitry. The UDPD command (79H) is used to instruct the device to enter Ultra-Deep Power-Down mode (UDPD Mode 1). Alternately, for maximum power conservation, V_{DDC} and V_{DDIO} can be turned off externally (UDPD Mode 2).

To test if the device is in Ultra-Deep Power-Down (in UDPD mode 1) without risk of bringing it out of Ultra-Deep Power-Down mode, use the Read Status Register Byte 1 instruction. The UDPD bit in Status Register Byte 1 will be 1 (pulled high by the internal pull-up resistor) if the device is in Ultra-Deep Power-Down mode, 0 otherwise.

When V_{DDC} and V_{DDIO} are turned off (UDPD Mode 2), all commands including the Read Status Register commands will be ignored. Since all commands will be ignored, the mode can be used as an extra protection mechanism against inadvertent or unintentional program and erase operations.

9.2 Auto Ultra-Deep Power-Down Mode after Write Operation

The Auto Ultra-Deep Power-Down Mode after Write Operation allows the device to further reduce its energy consumption by automatically entering the Ultra-Deep Power-Down Mode after completing an internally timed Write operation. The operation can be any one of the commands WR (Write), or WRSR (Write Status Register). Note that the WRSR2 command does not cause the device to go into Ultra-Deep Power-Down Mode. (See Table 7-5 for Status Register Byte 2 definition).

9.3 Slow Oscillator During Write Operation

The Slow Oscillator During Write Operation mode allows the device to further reduce its average current consumption by periodically slowing down the internal oscillator. This creates a duty cycle effect with time periods of high activity followed by timer periods of low activity. While this operating mode will increase the effective Write time, the average current over this Write time will be lower compared to the mode without this feature.

9.4 Exit Ultra-Deep Power-Down mode

Only the Exit Ultra-Deep Power-Down signal sequences or power cycling described in Figure 4-2 and in Section 10.9 will bring the device out of the Ultra- Deep Power-Down mode.

10. Command Descriptions

10.1 WREN (Write Enable, 06h):

The device powers up with the Write Enable Latch set to zero. This means that no write or erase instructions can be executed until the Write Enable Latch is set using the Write Enable (WREN) instruction. The Write Enable Latch is also set to zero automatically after any non-read instruction. Therefore, all page programming instructions and erase instructions must be preceded by a Write Enable (WREN) instruction. The sequence for the Write Enable instruction is shown in Figure 10-1.

Figure 10-1. WREN Sequence (06h)

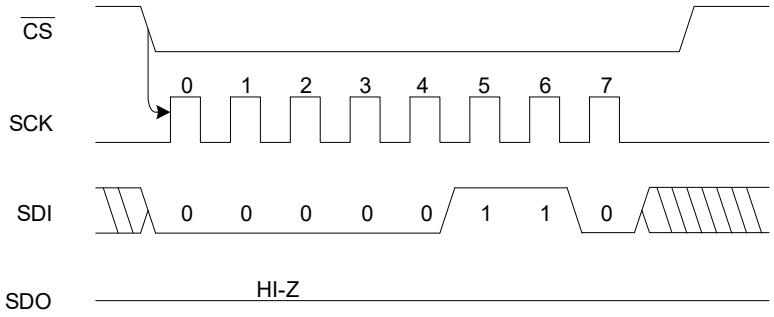


Table 10-1 is a list of actions that will automatically set the Write Enable Latch to zero when successfully executed. If an instruction is not successfully executed, for example if the $\overline{CS}$ pin is brought high before an integer multiple of 8 bits is clocked, the Write Enable Latch will not be reset.

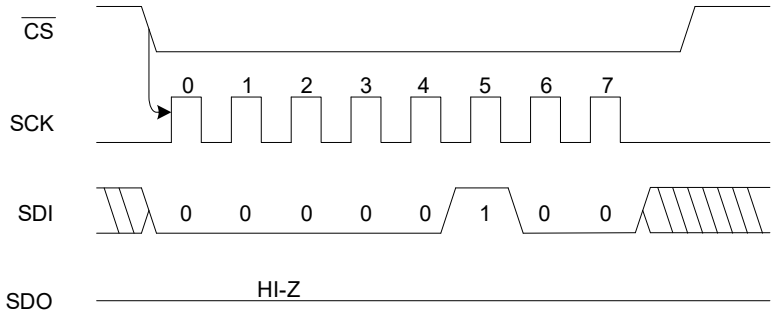
Table 10-1. Write Enable Latch to Zero

Instruction/Operation
Power-Up
WRDI (Write Disable)
WR (Write)
WRSR (Write Status Register)
WRSR2 (Write Status Register2)

10.2 WRDI (Write Disable, 04h):

To protect the device against inadvertent writes, the Write Disable instruction disables all write modes. Since the Write Enable Latch is automatically reset after each successful write instruction, it is not necessary to issue a WRDI instruction following a write instruction. The WRDI sequence is shown in Figure 10-2.

Figure 10-2. WRDI Sequence (04h)

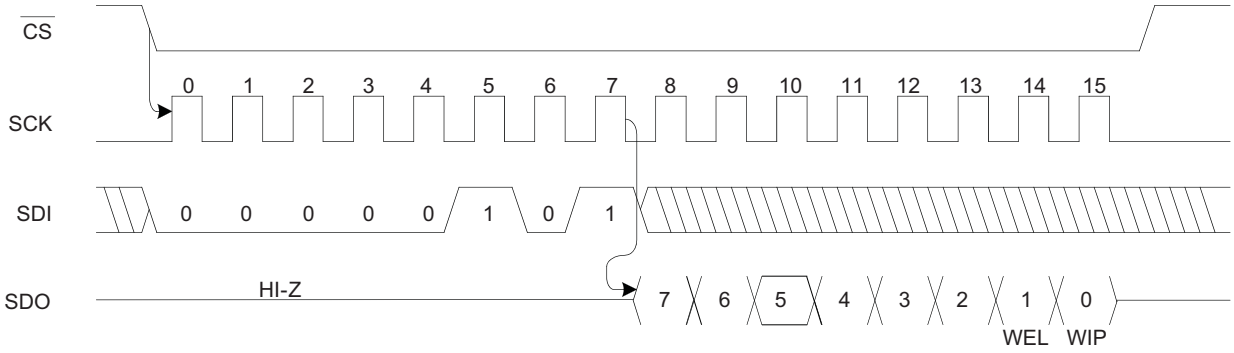


10.3 RDSR (Read Status Register Byte 1, 05h):

The Read Status Register Byte 1 instruction provides access to the Status Register and indication of write protection status of the memory.

Caution: The Write In Progress (WIP) and Write Enable Latch (WEL) indicate the status of the device. The RDSR sequence is shown in Figure 10-3.

Figure 10-3. RDSR Sequence (05h)

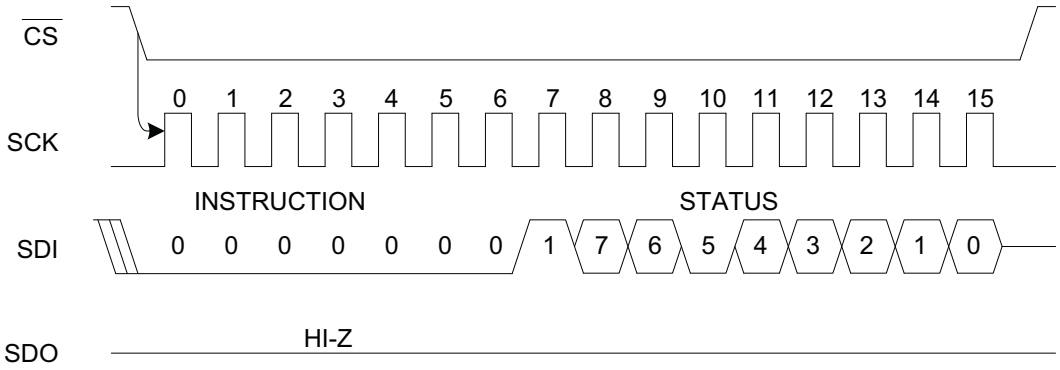


10.4 WRSR (Write Status Register Byte 1, 01h):

The Write Status Register (WRSR) instruction allows the user to select one of three levels of protection. The memory array can be block protected (see Table 8-2) or have no protection at all. The SRWD bit sets the write status of the Status Register (see Table 8-1).

Only the BP0, BP1 and SRWD bits are writable and are nonvolatile cells. The WRSR sequence is shown in Figure 10-4.

Figure 10-4. WRSR Sequence (01h)



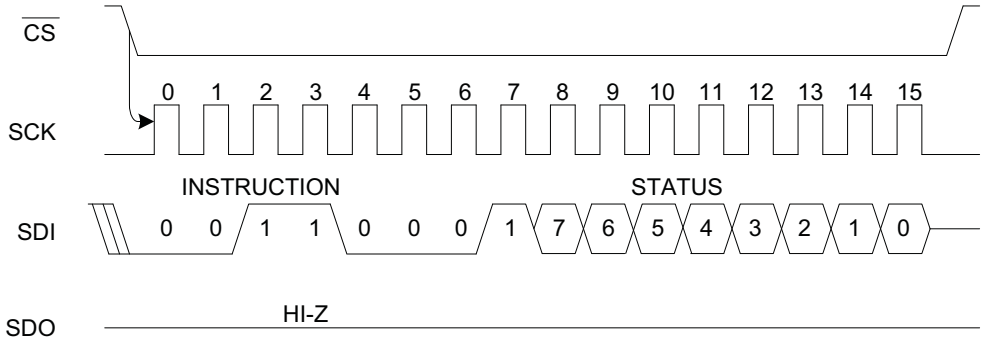
10.5 WRSR2 (Write Status Register Byte 2, 31h):

The Write Status Register Byte 2 (WRSR2) instruction allows the user to set or clear the SLOWOSC or AUDPD bits.

The user must set the WEL bit before issuing this command. Once the device accepts the WRSR2 command the WIP bit will be set to indicate that the device is busy. Once the device completes the operation, the WEL and WIP bits will be automatically cleared.

The WRSR sequence is shown in Figure 10-5.

Figure 10-5. WRSR2 Sequence (31h)



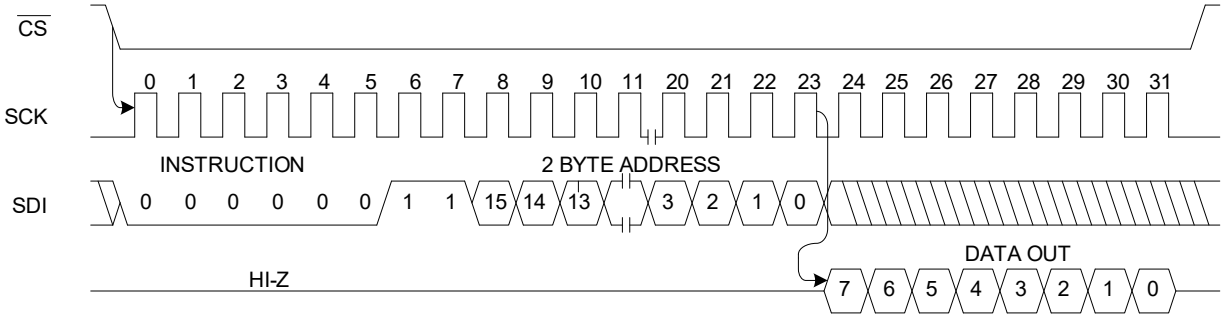
10.6 READ (Read Data, 03h):

Reading the Adesto RM333X Series via the Serial Data Output (SDO) pin requires the following sequence: First the $\overline{CS}$ line is pulled low to select the device; then the READ op-code is transmitted via the SDI line, followed by the address to be read (A15-A0). Although not all 16 address bits are used, a full 2 bytes of address must be transmitted to the device. For the 32-256Kb device, only address A0 to A14 are used; the rest are don't cares and must be set to “0”.

Once the read instruction and address have been sent, any further data on the SDI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SDO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the byte of data comes out. This completes the reading of one byte of data.

The READ sequence can be automatically continued by keeping the $\overline{CS}$ low. At the end of the first data byte the byte address is internally incremented and the next higher address data byte will be shifted out. When the highest address is reached, the address counter will roll over to the lowest address (00000), thus allowing the entire memory to be read in one continuous read cycle. The READ sequence is shown in Figure 10-6.

Figure 10-6. Single Byte READ Sequence (03h)



10.7 WR (Write Data, 02h):

Product	Density	Page Size (bytes)
RM3336	256Kbit	64
RM3335	128Kbit	64
RM3334	64Kbit	32
RM3333	32Kbit	32

The Write (WR) instruction allows bytes to be written to the memory. But first, the device must be write-enabled via the WREN instruction. The $\overline{CS}$ pin must be brought high after completion of the WREN instruction; then the $\overline{CS}$ pin can be brought back low to start the WR instruction. The $\overline{CS}$ pin going high at the end of the WR input sequence initiates the internal write cycle. During the internal write cycle, all commands except the RDSR instruction are ignored.
A WR instruction requires the following sequence: After the $\overline{CS}$ line is pulled low to select the device, the WR op-code is transmitted via the SDI line, followed by the byte address (A15-A0) and the data (D7-D0) to be written. For the 32-256Kb device, only address A0 to A14 are used; the rest are don't cares and must be set to “0”. The internal write cycle sequence will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.
The Write In Progress status of the device can be determined by initiating a Read Status Register (RDSR) instruction and monitoring the WIP bit. If the WIP bit (Bit 0) is a “1”, the write cycle is still in progress. If the WIP bit is “0”, the write cycle has ended. Only the RDSR instruction is enabled during the write cycle.

The Adesto RM333X Series is capable of 1-64 byte write operation (32 byte for 32Kbit and 64Kbit products, and 64 bytes for 128Kbit and 256Kbit products).

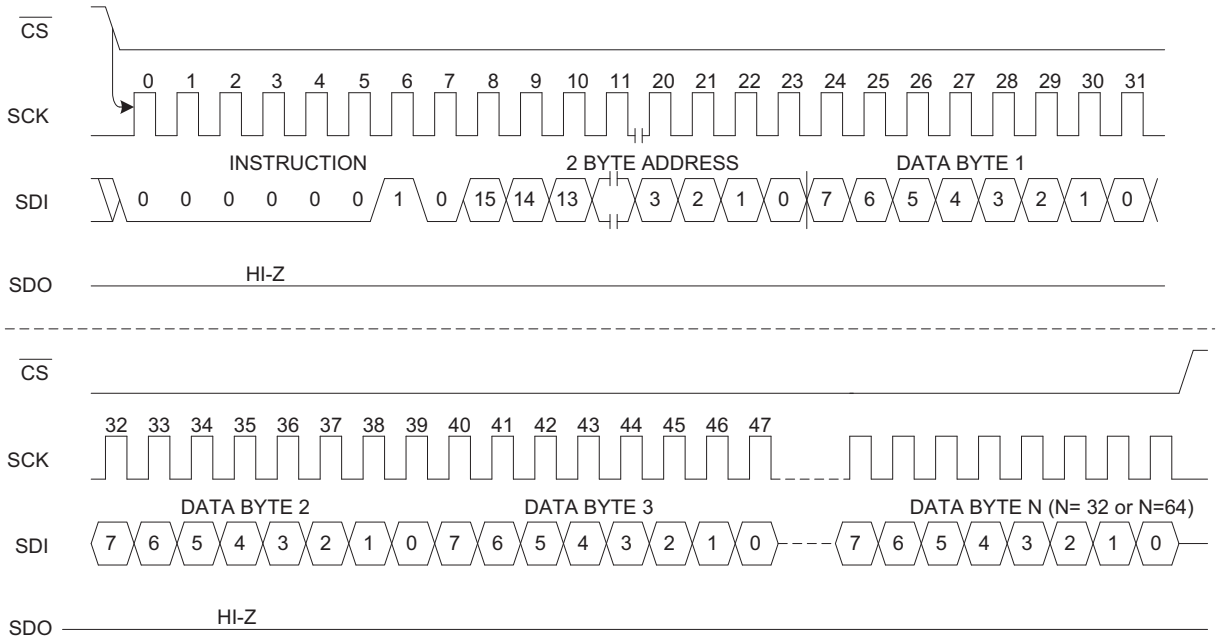
After each byte of data is received, the five low-order address bits (A4-A0) are internally incremented by one; the high-order bits of the address will remain constant. All transmitted data that goes beyond the end of the current page are written from the start address of the same page (from the address whose 5 least significant bits [A4-A0] are all zero). If more than 32 bytes are sent to the device, previously latched data are discarded and the last 32 data bytes are ensured to be written correctly within the same page. If less than 32 data bytes are sent to the device, they are correctly written at the requested addresses without having any effects on the other bytes of the same page.

For devices with the 64 byte page size, after each byte of data is received, the six low-order address bits (A5-A0) are internally incremented by one; the high-order bits of the address will remain constant. All transmitted data that goes beyond the end of the current page are written from the start address of the same page (from the address whose 6 least significant bits [A5-A0] are all zero). If more than 64 bytes are sent to the device, previously latched data are discarded and the last 64 data bytes are ensured to be written correctly within the same page. If less than 64 data bytes are sent to the device, they are correctly written at the requested addresses without having any effects on the other bytes of the same page.

The Adesto RM333X Series is automatically returned to the write disable state at the completion of a program cycle. The sequence for the WR command is shown in Figure 10-7. Note that the Multi-Byte Write operation is internally executed by sequentially writing the words in the Page Buffer.

NOTE: If the device is not write enabled (WREN) previous to the Write instruction, the device will ignore the write instruction and return to the standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to re initiate the serial communication.

Figure 10-7. WRITE Sequence (02h)



10.8 UDPD (Ultra-Deep Power-Down)

There are two different variations of Ultra-Deep Power-Down, UDPD mode 1 and UDPD mode 2. For UDPD mode 1, an SPI command is used to turn off the supply voltages internally on the chip. For UDPD mode 2, V_{DDC} and V_{DDIO} are turned off externally.

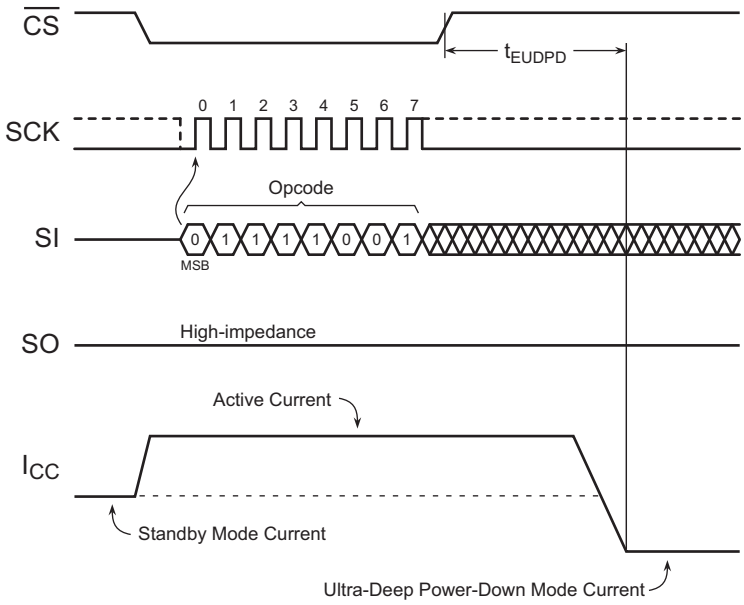
The Ultra-Deep Power-Down mode allows the device to further reduce its energy consumption compared to the existing Standby mode by shutting down additional internal circuitry. When the device is in the Ultra-Deep Power-Down mode (UDPD mode 2), all commands including the Read Status Register command will be ignored. Since all commands will be ignored, the mode can be used as an extra protection mechanism against inadvertent or unintentional program and erase operations.

10.8.1 UDPD mode 1

Entering the Ultra-Deep Power-Down mode 1 is accomplished by simply asserting the $\overline{CS}$ pin, clocking in the opcode 79h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the device will enter the Ultra-Deep Power-Down mode within the maximum time of $\mathbf{t_{EUDPD}}$.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation and return to the standby mode once the $\overline{CS}$ pin is deasserted. In addition, the device will default to the standby mode after a power cycle. The Ultra-Deep Power-Down command will be ignored if an internally self-timed operation such as a program or erase cycle is in progress. The sequence for UDPD is shown in Figure 10-8. See also Figure 4-2, Power-up Timing (Enter/Exit Ultra-Deep Power-Down Mode 1)

Figure 10-8. Ultra-Deep Power-Down (79h)



10.8.2 UDPD mode 2

In this mode, V_{DDC} and V_{DDIO} are turned off externally. Ideally both voltages should be turned off at the same time. If this is difficult to achieve, and there will be a time difference between the shutoff of the two voltages, the system designer should make sure that V_{DDIO} is turned off before V_{DDC} .

Similarly, when the device is turned on again, V_{DDIO} should be turned on before V_{DDC} if it is not possible to turn both on at the same time.

See Figure 4-3, Power-up Timing (Enter/Exit Ultra-Deep Power-Down Mode 2).

10.9 Exit Ultra-Deep Power-Down

To exit from the Ultra-Deep Power-Down mode, one of the following operations can be performed:

10.9.1 Exit Ultra-Deep Power-Down / Hardware Reset

Issue the Exit Ultra-Deep Power-Down / Hardware Reset sequence as described in Section 10.10, Hardware Reset.

10.9.2 Power Cycling

The device can also exit the Ultra-Deep Power Mode by power cycling the device. The system must wait for the device to return to the standby mode before normal command operations can be resumed. Upon recovery from Ultra-Deep Power-Down all internal registers will be at their Power-On default state.

10.10 Hardware Reset

The Exit Ultra-Deep Power-Down / Hardware Reset command sequence can be used to wakeup the device from Ultra-Deep Power-Down. This sequence can also be used to reset the device to its power on state without cycling power. It is in any case recommended to run a Hardware Reset command sequence after every time the device is powered up.

The reset sequence does not use the SCK pin. The SCK pin has to be held low (mode 0) or high (mode 3) through the entire reset sequence.This prevents any confusion with a command, as no command bits are transferred (clocked).

A reset is commanded when the data on the SDI pin is 0101 on four consecutive positive edges of the $\overline{CS}$ pin with no edge on the SCK pin throughout. This is a sequence where

1) $\overline{CS}$ is driven active low to select the device. This powers up the SPI slave.

2) Clock (SCK) remains stable in either a high or low state.

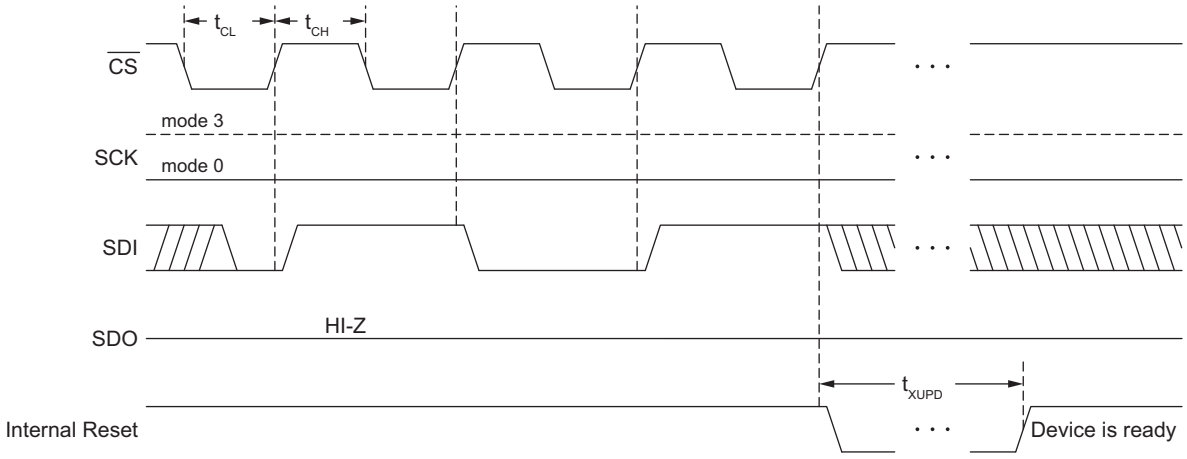
3) SDI is driven low by the bus master, simultaneously with $\overline{CS}$ going active low. No SPI bus slave drives SDI during $\overline{CS}$ low before a transition of SCK ie: slave streaming output active is not allowed until after the first edge of SCK.

4) $\overline{CS}$ is driven inactive. The slave captures the state of SI on the rising edge of $\overline{CS}$.

The above steps are repeated 4 times, each time alternating the state of SI.

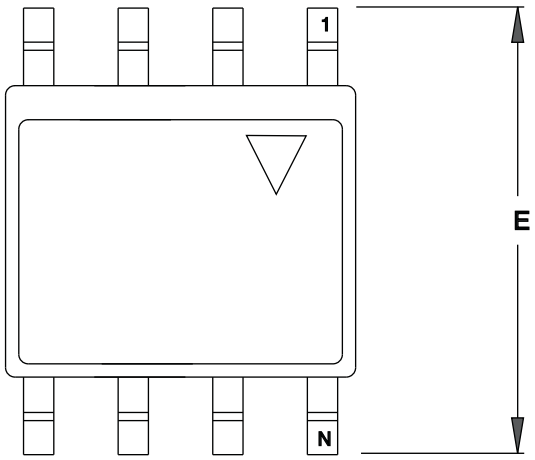
After the fourth $\overline{CS}$ pulse, the slave triggers its internal reset. SI is low on the first $\overline{CS}$, high on the second, low on the third, high on the fourth. This provides a 5h, unlike random noise. Any activity on SCK during this time will halt the sequence and a Reset will not be generated. Figure 10-9 below illustrates the timing for the Hardware Reset operation.

Figure 10-9. Hardware Reset

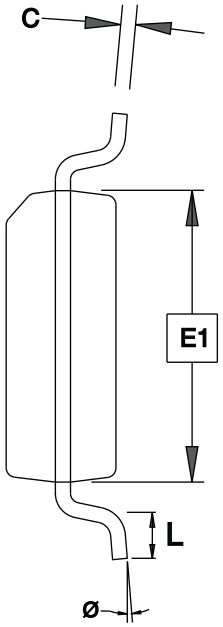


11. Package Information

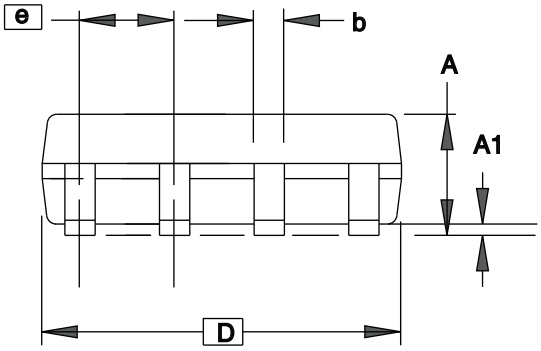
11.1 SN (JEDEC SOIC)



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

COMMON DIMENSIONS
(Unit of Measure = mm)

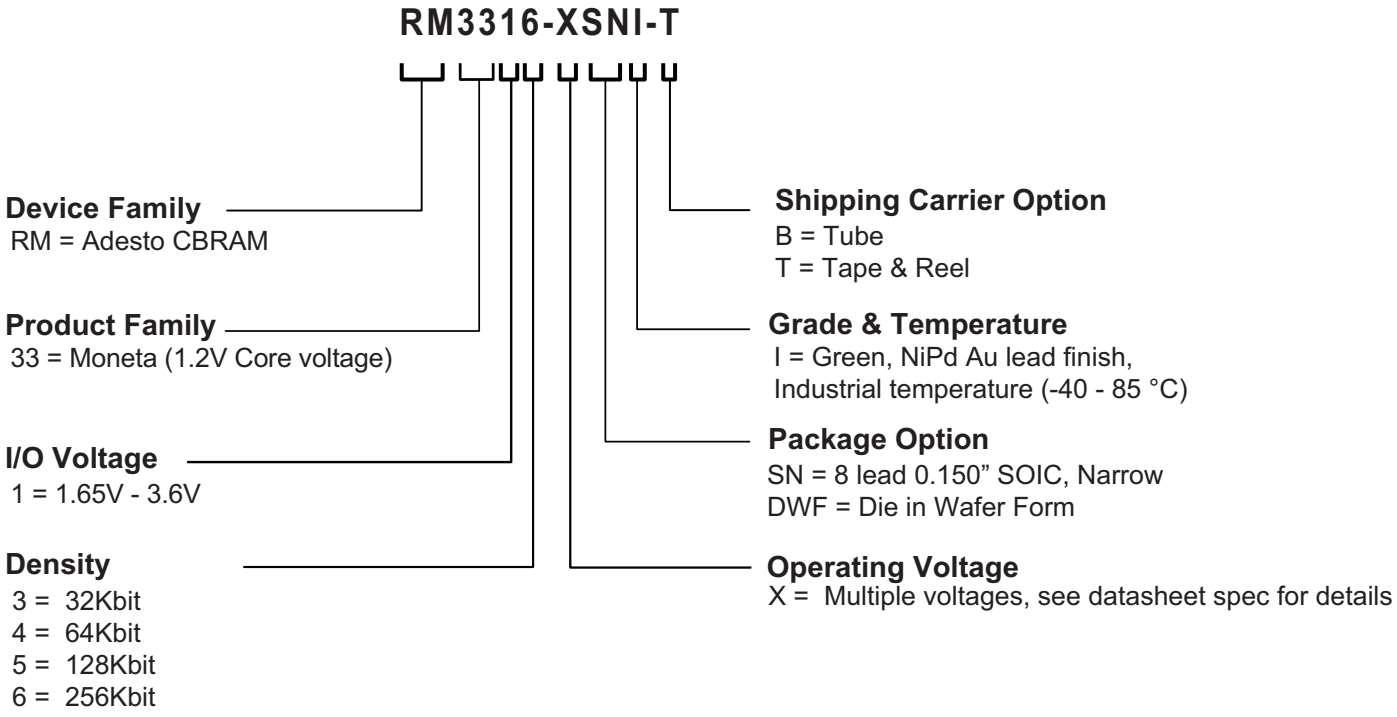
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
ø	0°	–	8°	

8/20/14

adesto™ TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	TITLE 8S1, 8-lead (0.150"Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	GPC SWB	DRAWING NO. 8S1	REV. G

12. Ordering Information

12.1 Ordering Detail



12.2 Ordering Codes

Ordering Code	Package	Density	Operating Voltage	f_{SCK}	Device Grade	Ship Carrier	Qty. Carrier
RM3336-XSNI-T	SN	256 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Reel	4000
RM3335-XSNI-T	SN	128 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Reel	4000
RM3334-XSNI-T	SN	64 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Reel	4000
RM3333-XSNI-T	SN	32 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Reel	4000
RM3336-X-DWF	DWF	256 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Wafer	Contact Adesto
RM3335-X-DWF	DWF	128 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Wafer	Contact Adesto
RM3334-X-DWF	DWF	64 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Wafer	Contact Adesto
RM3333-X-DWF	DWF	32 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Wafer	Contact Adesto

Package Type	
SN	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
DWF [1]	Die in Wafer Form (Known Good Die - KGD)

1. Contact Adesto for Wafer Die Map and other ordering information.

13. Revision History

Doc. Rev.	Date	Comments
RM333X-144A	7/2017	Initial document release.
RM333X-144B	11/2017	Added patent information.

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