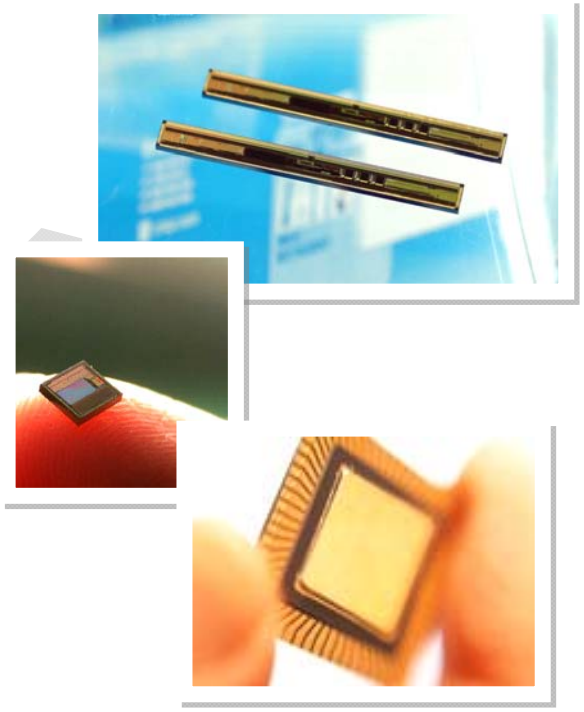
Raydium 瑞鼎科技股份有限公司
Raydium Semiconductor Corporation



RM68080 Data Sheet

Single Chip Driver with 262K color

for 240RGBx432 a-Si TFT LCD

Revision：0.4

Date：Dec 14, 2010

Revision History：

Revision	Description Of Change	Date
0.1	New creation	2010/5/27
0.2	Page 19: Modified the pin description of TEST1 -- TEST5 “Test pins (internal pull low). Connect to GND or leave these pins as open.” ➔ “Test pins. Connect to GND or leave these pins as open. Page 19: Add pad description for VMON	2010/5/31
0.3	Page 30: Move BC0 from D9 to D8 Page 75: Add recommended timing for RGBIF	2010/11/24
0.4	Page 11 – 13: Modified the truncated pad coordination	2010/12/14

Table of Content

1. General Description

The RM68080 is a single-chip liquid crystal controller driver LSI for a-Si TFT panel, comprising 233,280 bytes RAM for a maximum 240 RGB x 432 dots graphics display, source driver, gate driver and power supply circuit. For efficient data transfer, the RM68080 supports high-speed interface via 8-/9-/16-/18-bit ports as system interface to the microcomputer and high-speed RAM write function. As moving picture interface, the RM68080 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and DB17-0).

Also, the RM68080 incorporates step-up circuit and voltage follower circuit to generate TFT liquid crystal panel drive voltages.

The RM68080's power management functions such as 8-color display and power operation mode such as deep standby mode make this LSI a perfect driver for the medium or small sized portable products with color display systems such as digital cellular phones or hand-held devices with outstanding battery consistency.

2. Features

- A single-chip controller driver incorporating a gate circuit and a power supply circuit for a maximum 240 RGB x 432 dots graphics display on amorphous TFT panel in 262k colors
- System interface
  1. High-speed interface via 8-, 9-, 16-, 18-bit parallel ports
  2. Clock synchronous serial interface
- Moving picture display interface
  1. 16-, 18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  2. VSYNC interface (System interface + VSYNC)
- High-speed RAM write function
- Window address function to specify a rectangular area writing data in the internal RAM
- Write data within a rectangular area in the internal RAM via moving picture interface
- Reduce data transfer repeat by specifying the area in the RAM to rewrite data
- Support displaying still picture data in RAM area while displaying moving pictures simultaneously
- Abundant color display and drawing functions
  1. Programmable γ-correction function for 262k-color display
  2. Partial display function
- Low power consumption architecture (allowing direct input of interface I/O power supply)
  1. Deep standby mode
  2. 8-color display function
  3. Input power supply voltages: IOVCC = 1.65V~3.3V (interface I/O power supply)
     VCI = 2.5V~3.3V (liquid crystal analog circuit power supply)
     VCC = 2.5V~3.3V (logic circuit power supply)
- Incorporates a liquid crystal drive power supply circuit

1. Source driver liquid crystal drive/VCOM power supply: DDVDH-GND = 4.5V ~ 6.0V

   VCL-GND = -2.0V ~ -3.0V

   VCI-VCL ≦ 6.0V

2. Gate drive power supply: VGH-GND = 10.0V ~ 19.8V

   VGL-GND = -4.5V ~ -13.5V

   VGH-VGL ≦ 30.0V

3. VCOM drive (VCOM power supply): VCOMH = (VCI+0.2)V ~ (DDVDH-0.2)V

   VCOML = (VCL+0.2) V ~ 0V

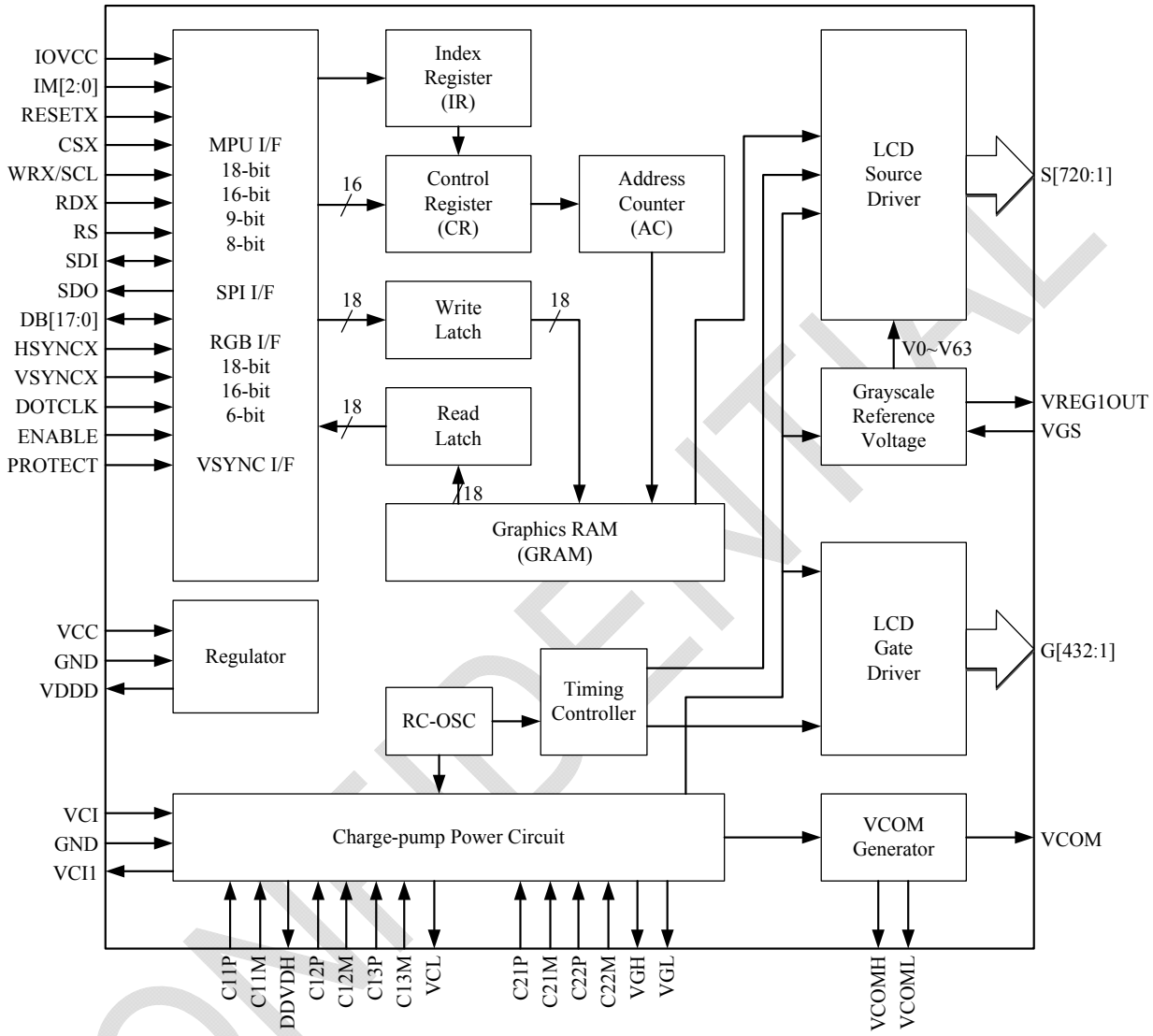
   VCOMH-VCOML amplitude = 6.0V (max.)

- Liquid crystal power supply startup sequencer
- TFT storage capacitance: Cst only (common VCOM formula)
- 233,280-byte internal RAM
- Internal 720-channel source driver and 432-channel gate driver
- Single-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate
- Internal reference voltage: to generate VREG1OUT

Table 1 Power Supply Specifications

No.	Item		RM68080
1	TFT data lines		720 output
2	TFT gate lines		432 output
3	TFT display storage capacitance		Cst only (Common VCOM)
4	Liquid crystal drive output	S1~S720	V0~V63 grayscales
		G1~G320	VGH-VGL
		VCOM	Change VCOMH-VCOML amplitude with electronic volume Change VCOMH with electronic volume
5	Input voltage	IOVCC (interface voltage)	1.65V~3.30V Power supply to IM0/ID, IM1-2, RESETX, DB17-0, RDX, SDI, SDO, WR/SCL, RS, CSX, VSYNCX, HSYNCX, DOTCLK, ENABLE, FMARK. Connect to VCC and VCI on the FPC when the electrical potentials are the same.
		VCI (liquid crystal drive power supply voltage)	2.50V~3.30V Connect to IOVCC and VCI on the FPC when the electrical potentials are the same.
		VCC (logic circuit power)	2.50V~3.30V Connect to IOVCC and VCC on the FPC when the electrical potentials are the same.
6	Liquid crystal drive voltages	DDVDH	4.5V ~ 6.0V
		VGH	10.0V ~ 18.0V
		VGL	-4.5V ~ -13.5V
		VGH-VGL	Max. 28.0V
		VCL	-1.9V ~ -3.3V
		VCI-VCL	Max. 6.0V
7	Internal step-up circuits	DDVDH	VCI1x2
		VGH	VCI1x5, x6
		VGL	VCI1x-3, -4, -5
		VCL	VCI1x-1

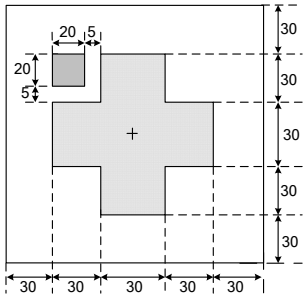
3. Block Diagram



4. Pin Diagram

Alignment Marks

A1



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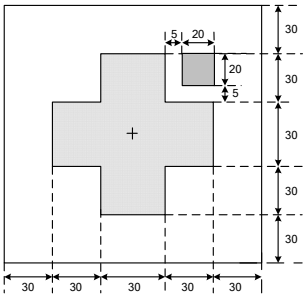
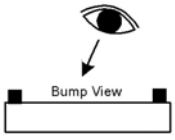
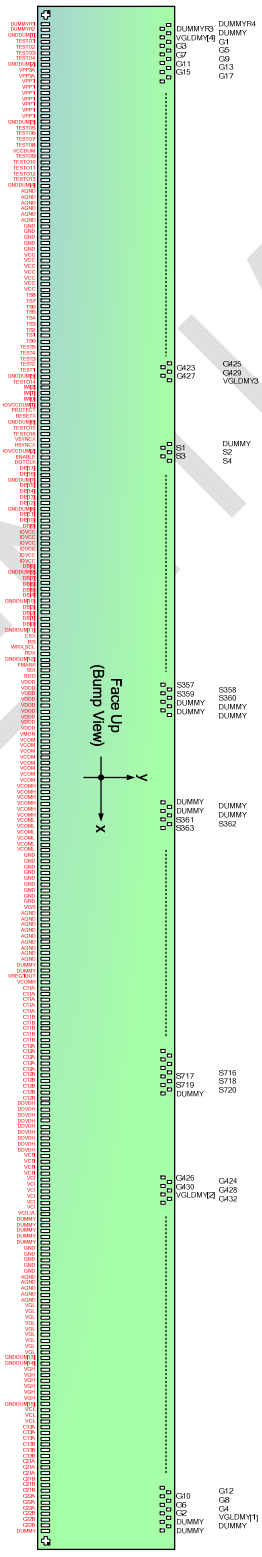


Unit: um





- Chip size: 19.03 mm x 0.80 mm (Include sealing and scribe line)
- Chip thickness: 280 um (typ.)
- PAD coordinates: PAD center
- PAD coordinates origin: Chip center
- Au bump size

4.1.1 15um x 100um: Output Pads to Panel

4.1.2 50um x 90um: Input Pads

- Au bump pitch: See PAD coordinates table
- Au bump height: 12um (typ.)
- Alignment mark

Alignment mark shape	X	Y
Type A	-9381.0	-246
	9381.0	-246

Pad Coordinate (Unit: um)

No	Name	X	Y
1	DUMMYR1	-9135	-286.5
2	DUMMYR2	-9065	-286.5
3	GNDDUM[1]	-8995	-286.5
4	TESTO1	-8925	-286.5
5	TESTO2	-8855	-286.5
6	TESTO3	-8785	-286.5
7	TESTO4	-8715	-286.5
8	GNDDUM[2]	-8645	-286.5
9	VPP3A	-8575	-286.5
10	VPP3A	-8505	-286.5
11	VPP1	-8435	-286.5
12	VPP1	-8365	-286.5
13	VPP1	-8295	-286.5
14	VPP1	-8225	-286.5
15	VPP1	-8155	-286.5
16	VPP1	-8085	-286.5
17	VPP1	-8015	-286.5
18	GNDDUM[3]	-7945	-286.5
19	TESTO5	-7875	-286.5
20	TESTO6	-7805	-286.5
21	TESTO7	-7735	-286.5
22	TESTO8	-7665	-286.5
23	VCCDUM	-7595	-286.5
24	TESTO9	-7525	-286.5
25	TESTO10	-7455	-286.5
26	TESTO11	-7385	-286.5
27	TESTO12	-7315	-286.5
28	TESTO13	-7245	-286.5
29	GNDDUM[4]	-7175	-286.5
30	AGND	-7105	-286.5
31	AGND	-7035	-286.5
32	AGND	-6965	-286.5
33	AGND	-6895	-286.5
34	AGND	-6825	-286.5
35	AGND	-6755	-286.5
36	GND	-6685	-286.5
37	GND	-6615	-286.5
38	GND	-6545	-286.5
39	GND	-6475	-286.5
40	GND	-6405	-286.5
41	VCC	-6335	-286.5
42	VCC	-6265	-286.5
43	VCC	-6195	-286.5
44	VCC	-6125	-286.5
45	VCC	-6055	-286.5
46	VCC	-5985	-286.5
47	VCC	-5915	-286.5
48	TS8	-5845	-286.5
49	TS7	-5775	-286.5
50	TS6	-5705	-286.5
51	TS5	-5635	-286.5
52	TS4	-5565	-286.5
53	TS3	-5495	-286.5
54	TS2	-5425	-286.5
55	TS1	-5355	-286.5
56	TS0	-5285	-286.5
57	TEST5	-5215	-286.5
58	TEST4	-5145	-286.5
59	TEST3	-5075	-286.5
60	TEST2	-5005	-286.5
61	TEST1	-4935	-286.5
62	GNDDUM[5]	-4865	-286.5
63	TESTO14	-4795	-286.5
64	IM[2]	-4725	-286.5
65	IM[1]	-4655	-286.5
66	IM[0]	-4585	-286.5
67	IOVCCDUM[1]	-4515	-286.5
68	PROTECT	-4445	-286.5
69	RESETX	-4375	-286.5
70	GNDDUM[6]	-4305	-286.5
71	TESTO15	-4235	-286.5
72	TESTO16	-4165	-286.5
73	VSYNCX	-4095	-286.5
74	HSYNCX	-4025	-286.5
75	IOVCCDUM[2]	-3955	-286.5
76	ENABLE	-3885	-286.5
77	DOTCLK	-3815	-286.5
78	DB[17]	-3745	-286.5
79	DB[16]	-3675	-286.5
80	GNDDUM[7]	-3605	-286.5
81	DB[15]	-3535	-286.5
82	DB[14]	-3465	-286.5
83	DB[13]	-3395	-286.5
84	DB[12]	-3325	-286.5
85	GNDDUM[8]	-3255	-286.5
86	DB[11]	-3185	-286.5
87	DB[10]	-3115	-286.5
88	DB[9]	-3045	-286.5
89	IOVCC	-2975	-286.5
90	IOVCC	-2905	-286.5
91	IOVCC	-2835	-286.5
92	IOVCC	-2765	-286.5
93	IOVCC	-2695	-286.5
94	IOVCC	-2625	-286.5
95	DB[8]	-2555	-286.5
96	GNDDUM[9]	-2485	-286.5
97	DB[7]	-2415	-286.5
98	DB[6]	-2345	-286.5
99	DB[5]	-2275	-286.5
100	DB[4]	-2205	-286.5
101	GNDDUM[10]	-2135	-286.5
102	DB[3]	-2065	-286.5
103	DB[2]	-1995	-286.5
104	DB[1]	-1925	-286.5
105	DB[0]	-1855	-286.5
106	GNDDUM[11]	-1785	-286.5
107	CSX	-1715	-286.5
108	RS	-1645	-286.5
109	WRX_SCL	-1575	-286.5
110	RDX	-1505	-286.5
111	GNDDUM[12]	-1435	-286.5
112	FMARK	-1365	-286.5
113	SDI	-1295	-286.5
114	SDO	-1225	-286.5
115	VDDD	-1155	-286.5
116	VDDD	-1085	-286.5
117	VDDD	-1015	-286.5
118	VDDD	-945	-286.5
119	VDDD	-875	-286.5
120	VDDD	-805	-286.5
121	VDDD	-735	-286.5
122	VDDD	-665	-286.5
123	VDDD	-595	-286.5
124	VMON	-525	-286.5
125	VCOM	-455	-286.5
126	VCOM	-385	-286.5
127	VCOM	-315	-286.5
128	VCOM	-245	-286.5
129	VCOM	-175	-286.5
130	VCOM	-105	-286.5
131	VCOM	-35	-286.5
132	VCOM	35	-286.5
133	VCOMH	105	-286.5
134	VCOMH	175	-286.5
135	VCOMH	245	-286.5
136	VCOMH	315	-286.5
137	VCOMH	385	-286.5
138	VCOMH	455	-286.5
139	VCOML	525	-286.5
140	VCOML	595	-286.5
141	VCOML	665	-286.5
142	VCOML	735	-286.5
143	VCOML	805	-286.5
144	VCOML	875	-286.5
145	GND	945	-286.5
146	GND	1015	-286.5
147	GND	1085	-286.5
148	GND	1155	-286.5
149	GND	1225	-286.5
150	GND	1295	-286.5
151	GND	1365	-286.5
152	GND	1435	-286.5
153	GND	1505	-286.5
154	VGS	1575	-286.5
155	AGND	1645	-286.5
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164	DUMMY	2275	-286.5
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166	VREG1OUT	2415	-286.5
167	VCOMR	2485	-286.5
168	C11A	2555	-286.5
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176	C11B	3115	-286.5
177	C11B	3185	-286.5
178	C12A	3255	-286.5
179	C12A	3325	-286.5
180	C12A	3395	-286.5
181	C12A	3465	-286.5
182	C12A	3535	-286.5
183	C12B	3605	-286.5
184	C12B	3675	-286.5
185	C12B	3745	-286.5
186	C12B	3815	-286.5
187	C12B	3885	-286.5
188	DDVDH	3955	-286.5
189	DDVDH	4025	-286.5
190	DDVDH	4095	-286.5
191	DDVDH	4165	-286.5
192	DDVDH	4235	-286.5
193	DDVDH	4305	-286.5
194	DDVDH	4375	-286.5
195	DDVDH	4445	-286.5
196	DDVDH	4515	-286.5
197	VCI1	4585	-286.5
198	VCI1	4655	-286.5
199	VCI1	4725	-286.5
200	VCI1	4795	-286.5
201	VCI	4865	-286.5
202	VCI	4935	-286.5
203	VCI	5005	-286.5
204	VCI	5075	-286.5
205	VCI	5145	-286.5
206	VCI	5215	-286.5
207	VCILVL	5285	-286.5
208	DUMMY	5355	-286.5
209	DUMMY	5425	-286.5
210	DUMMY	5495	-286.5
211	DUMMY	5565	-286.5
212	DUMMY	5635	-286.5
213	GND	5705	-286.5
214	GND	5775	-286.5
215	GND	5845	-286.5
216	GND	5915	-286.5
217	GND	5985	-286.5
218	AGND	6055	-286.5
219	AGND	6125	-286.5
220	AGND	6195	-286.5
221	AGND	6265	-286.5
222	AGND	6335	-286.5
223	VGL	6405	-286.5
224	VGL	6475	-286.5
225	VGL	6545	-286.5
226	VGL	6615	-286.5
227	VGL	6685	-286.5
228	VGL	6755	-286.5
229	VGL	6825	-286.5
230	VGL	6895	-286.5
231	VGL	6965	-286.5
232	GNDDUM[13]	7035	-286.5
233	GNDDUM[14]	7105	-286.5
234	VGH	7175	-286.5
235	VGH	7245	-286.5
236	VGH	7315	-286.5
237	VGH	7385	-286.5
238	VGH	7455	-286.5
239	VGH	7525	-286.5
240	GNDDUM[15]	7595	-286.5

No	Name	X	Y
241	VCL	7665	-286.5
242	VCL	7735	-286.5
243	VCL	7805	-286.5
244	C13A	7875	-286.5
245	C13A	7945	-286.5
246	C13A	8015	-286.5
247	C13B	8085	-286.5
248	C13B	8155	-286.5
249	C13B	8225	-286.5
250	C21A	8295	-286.5
251	C21A	8365	-286.5
252	C21A	8435	-286.5
253	C21B	8505	-286.5
254	C21B	8575	-286.5
255	C21B	8645	-286.5
256	C22A	8715	-286.5
257	C22A	8785	-286.5
258	C22A	8855	-286.5
259	C22B	8925	-286.5
260	C22B	8995	-286.5
261	C22B	9065	-286.5
262	DUMMY	9135	-286.5
263	DUMMY	9397.5	171
264	DUMMY	9382.5	290
265	DUMMY	9367.5	171
266	VGLDMY[1]	9352.5	290
267	G2	9337.5	171
268	G4	9322.5	290
269	G6	9307.5	171
270	G8	9292.5	290
271	G10	9277.5	171
272	G12	9262.5	290
273	G14	9247.5	171
274	G16	9232.5	290
275	G18	9217.5	171
276	G20	9202.5	290
277	G22	9187.5	171
278	G24	9172.5	290
279	G26	9157.5	171
280	G28	9142.5	290
281	G30	9127.5	171
282	G32	9112.5	290
283	G34	9097.5	171
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288	G44	9022.5	290
289	G46	9007.5	171
290	G48	8992.5	290
291	G50	8977.5	171
292	G52	8962.5	290
293	G54	8947.5	171
294	G56	8932.5	290
295	G58	8917.5	171
296	G60	8902.5	290
297	G62	8887.5	171
298	G64	8872.5	290
299	G66	8857.5	171
300	G68	8842.5	290
301	G70	8827.5	171
302	G72	8812.5	290
303	G74	8797.5	171
304	G76	8782.5	290
305	G78	8767.5	171
306	G80	8752.5	290
307	G82	8737.5	171
308	G84	8722.5	290
309	G86	8707.5	171
310	G88	8692.5	290
311	G90	8677.5	171
312	G92	8662.5	290
313	G94	8647.5	171
314	G96	8632.5	290
315	G98	8617.5	171
316	G100	8602.5	290
317	G102	8587.5	171
318	G104	8572.5	290
319	G106	8557.5	171
320	G108	8542.5	290
321	G110	8527.5	171
322	G112	8512.5	290
323	G114	8497.5	171
324	G116	8482.5	290
325	G118	8467.5	171
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327	G122	8437.5	171
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329	G126	8407.5	171
330	G128	8392.5	290
331	G130	8377.5	171
332	G132	8362.5	290
333	G134	8347.5	171
334	G136	8332.5	290
335	G138	8317.5	171
336	G140	8302.5	290
337	G142	8287.5	171
338	G144	8272.5	290
339	G146	8257.5	171
340	G148	8242.5	290
341	G150	8227.5	171
342	G152	8212.5	290
343	G154	8197.5	171
344	G156	8182.5	290
345	G158	8167.5	171
346	G160	8152.5	290
347	G162	8137.5	171
348	G164	8122.5	290
349	G166	8107.5	171
350	G168	8092.5	290
351	G170	8077.5	171
352	G172	8062.5	290
353	G174	8047.5	171
354	G176	8032.5	290
355	G178	8017.5	171
356	G180	8002.5	290
357	G182	7987.5	171
358	G184	7972.5	290
359	G186	7957.5	171
360	G188	7942.5	290
361	G190	7927.5	171
362	G192	7912.5	290
363	G194	7897.5	171
364	G196	7882.5	290
365	G198	7867.5	171
366	G200	7852.5	290
367	G202	7837.5	171
368	G204	7822.5	290
369	G206	7807.5	171
370	G208	7792.5	290
371	G210	7777.5	171
372	G212	7762.5	290
373	G214	7747.5	171
374	G216	7732.5	290
375	G218	7717.5	171
376	G220	7702.5	290
377	G222	7687.5	171
378	G224	7672.5	290
379	G226	7657.5	171
380	G228	7642.5	290
381	G230	7627.5	171
382	G232	7612.5	290
383	G234	7597.5	171
384	G236	7582.5	290
385	G238	7567.5	171
386	G240	7552.5	290
387	G242	7537.5	171
388	G244	7522.5	290
389	G246	7507.5	171
390	G248	7492.5	290
391	G250	7477.5	171
392	G252	7462.5	290
393	G254	7447.5	171
394	G256	7432.5	290
395	G258	7417.5	171
396	G260	7402.5	290
397	G262	7387.5	171
398	G264	7372.5	290
399	G266	7357.5	171
400	G268	7342.5	290
401	G270	7327.5	171
402	G272	7312.5	290
403	G274	7297.5	171
404	G276	7282.5	290
405	G278	7267.5	171
406	G280	7252.5	290
407	G282	7237.5	171
408	G284	7222.5	290
409	G286	7207.5	171
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411	G290	7177.5	171
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437	G342	6787.5	171
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465	G398	6367.5	171
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467	G402	6337.5	171
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469	G406	6307.5	171
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727	S478	2242.5	290
728	S477	2227.5	171
729	S476	2212.5	290
730	S475	2197.5	171
731	S474	2182.5	290
732	S473	2167.5	171
733	S472	2152.5	290
734	S471	2137.5	171
735	S470	2122.5	290
736	S469	2107.5	171
737	S468	2092.5	290
738	S467	2077.5	171
739	S466	2062.5	290
740	S465	2047.5	171
741	S464	2032.5	290
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743	S462	2002.5	290
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756	S449	1807.5	171
757	S448	1792.5	290
758	S447	1777.5	171
759	S446	1762.5	290
760	S445	1747.5	171
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762	S443	1717.5	171
763	S442	1702.5	290
764	S441	1687.5	171
765	S440	1672.5	290
766	S439	1657.5	171
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768	S437	1627.5	171
769	S436	1612.5	290
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775	S430	1522.5	290
776	S429	1507.5	171
777	S428	1492.5	290
778	S427	1477.5	171
779	S426	1462.5	290
780	S425	1447.5	171

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794	S411	1237.5	171
795	S410	1222.5	290
796	S409	1207.5	171
797	S408	1192.5	290
798	S407	1177.5	171
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810	S395	997.5	171
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813	S392	952.5	290
814	S391	937.5	171
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817	S388	892.5	290
818	S387	877.5	171
819	S386	862.5	290
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821	S384	832.5	290
822	S383	817.5	171
823	S382	802.5	290
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826	S379	757.5	171
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847	DUMMY	442.5	290
848	DUMMY	427.5	171
849	DUMMY	-427.5	290
850	DUMMY	-442.5	171
851	DUMMY	-457.5	290
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855	S358	-517.5	290
856	S357	-532.5	171
857	S356	-547.5	290
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862	S351	-622.5	171
863	S350	-637.5	290
864	S349	-652.5	171
865	S348	-667.5	290
866	S347	-682.5	171
867	S346	-697.5	290
868	S345	-712.5	171
869	S344	-727.5	290
870	S343	-742.5	171
871	S342	-757.5	290
872	S341	-772.5	171
873	S340	-787.5	290
874	S339	-802.5	171
875	S338	-817.5	290
876	S337	-832.5	171
877	S336	-847.5	290
878	S335	-862.5	171
879	S334	-877.5	290
880	S333	-892.5	171
881	S332	-907.5	290
882	S331	-922.5	171
883	S330	-937.5	290
884	S329	-952.5	171
885	S328	-967.5	290
886	S327	-982.5	171
887	S326	-997.5	290
888	S325	-1012.5	171
889	S324	-1027.5	290
890	S323	-1042.5	171
891	S322	-1057.5	290
892	S321	-1072.5	171
893	S320	-1087.5	290
894	S319	-1102.5	171
895	S318	-1117.5	290
896	S317	-1132.5	171
897	S316	-1147.5	290
898	S315	-1162.5	171
899	S314	-1177.5	290
900	S313	-1192.5	171

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906	S307	-1282.5	171
907	S306	-1297.5	290
908	S305	-1312.5	171
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915	S298	-1417.5	290
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937	S276	-1747.5	290
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939	S274	-1777.5	290
940	S273	-1792.5	171
941	S272	-1807.5	290
942	S271	-1822.5	171
943	S270	-1837.5	290
944	S269	-1852.5	171
945	S268	-1867.5	290
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955	S258	-2017.5	290
956	S257	-2032.5	171
957	S256	-2047.5	290
958	S255	-2062.5	171
959	S254	-2077.5	290
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966	S247	-2182.5	171
967	S246	-2197.5	290
968	S245	-2212.5	171
969	S244	-2227.5	290
970	S243	-2242.5	171
971	S242	-2257.5	290
972	S241	-2272.5	171
973	S240	-2287.5	290
974	S239	-2302.5	171
975	S238	-2317.5	290
976	S237	-2332.5	171
977	S236	-2347.5	290
978	S235	-2362.5	171
979	S234	-2377.5	290
980	S233	-2392.5	171
981	S232	-2407.5	290
982	S231	-2422.5	171
983	S230	-2437.5	290
984	S229	-2452.5	171
985	S228	-2467.5	290
986	S227	-2482.5	171
987	S226	-2497.5	290
988	S225	-2512.5	171
989	S224	-2527.5	290
990	S223	-2542.5	171
991	S222	-2557.5	290
992	S221	-2572.5	171
993	S220	-2587.5	290
994	S219	-2602.5	171
995	S218	-2617.5	290
996	S217	-2632.5	171
997	S216	-2647.5	290
998	S215	-2662.5	171
999	S214	-2677.5	290
1000	S213	-2692.5	171
1001	S212	-2707.5	290
1002	S211	-2722.5	171
1003	S210	-2737.5	290
1004	S209	-2752.5	171
1005	S208	-2767.5	290
1006	S207	-2782.5	171
1007	S206	-2797.5	290
1008	S205	-2812.5	171
1009	S204	-2827.5	290
1010	S203	-2842.5	171
1011	S202	-2857.5	290
1012	S201	-2872.5	171
1013	S200	-2887.5	290
1014	S199	-2902.5	171
1015	S198	-2917.5	290
1016	S197	-2932.5	171
1017	S196	-2947.5	290
1018	S195	-2962.5	171
1019	S194	-2977.5	290
1020	S193	-2992.5	171
1021	S192	-3007.5	290
1022	S191	-3022.5	171
1023	S190	-3037.5	290
1024	S189	-3052.5	171
1025	S188	-3067.5	290
1026	S187	-3082.5	171
1027	S186	-3097.5	290
1028	S185	-3112.5	171
1029	S184	-3127.5	290
1030	S183	-3142.5	171
1031	S182	-3157.5	290
1032	S181	-3172.5	171
1033	S180	-3187.5	290
1034	S179	-3202.5	171
1035	S178	-3217.5	290
1036	S177	-3232.5	171
1037	S176	-3247.5	290
1038	S175	-3262.5	171
1039	S174	-3277.5	290
1040	S173	-3292.5	171
1041	S172	-3307.5	290
1042	S171	-3322.5	171
1043	S170	-3337.5	290
1044	S169	-3352.5	171
1045	S168	-3367.5	290
1046	S167	-3382.5	171
1047	S166	-3397.5	290
1048	S165	-3412.5	171
1049	S164	-3427.5	290
1050	S163	-3442.5	171
1051	S162	-3457.5	290
1052	S161	-3472.5	171
1053	S160	-3487.5	290
1054	S159	-3502.5	171
1055	S158	-3517.5	290
1056	S157	-3532.5	171
1057	S156	-3547.5	290
1058	S155	-3562.5	171
1059	S154	-3577.5	290
1060	S153	-3592.5	171
1061	S152	-3607.5	290
1062	S151	-3622.5	171
1063	S150	-3637.5	290
1064	S149	-3652.5	171
1065	S148	-3667.5	290
1066	S147	-3682.5	171
1067	S146	-3697.5	290
1068	S145	-3712.5	171
1069	S144	-3727.5	290
1070	S143	-3742.5	171
1071	S142	-3757.5	290
1072	S141	-3772.5	171
1073	S140	-3787.5	290
1074	S139	-3802.5	171
1075	S138	-3817.5	290
1076	S137	-3832.5	171
1077	S136	-3847.5	290
1078	S135	-3862.5	171
1079	S134	-3877.5	290
1080	S133	-3892.5	171
1081	S132	-3907.5	290
1082	S131	-3922.5	171
1083	S130	-3937.5	290
1084	S129	-3952.5	171
1085	S128	-3967.5	290
1086	S127	-3982.5	171
1087	S126	-3997.5	290
1088	S125	-4012.5	171
1089	S124	-4027.5	290
1090	S123	-4042.5	171
1091	S122	-4057.5	290
1092	S121	-4072.5	171
1093	S120	-4087.5	290
1094	S119	-4102.5	171
1095	S118	-4117.5	290
1096	S117	-4132.5	171
1097	S116	-4147.5	290
1098	S115	-4162.5	171
1099	S114	-4177.5	290
1100	S113	-4192.5	171
1101	S112	-4207.5	290
1102	S111	-4222.5	171
1103	S110	-4237.5	290
1104	S109	-4252.5	171
1105	S108	-4267.5	290
1106	S107	-4282.5	171
1107	S106	-4297.5	290
1108	S105	-4312.5	171
1109	S104	-4327.5	290
1110	S103	-4342.5	171
1111	S102	-4357.5	290
1112	S101	-4372.5	171
1113	S100	-4387.5	290
1114	S99	-4402.5	171
1115	S98	-4417.5	290
1116	S97	-4432.5	171
1117	S96	-4447.5	290
1118	S95	-4462.5	171
1119	S94	-4477.5	290
1120	S93	-4492.5	171
1121	S92	-4507.5	290
1122	S91	-4522.5	171
1123	S90	-4537.5	290
1124	S89	-4552.5	171
1125	S88	-4567.5	290
1126	S87	-4582.5	171
1127	S86	-4597.5	290
1128	S85	-4612.5	171
1129	S84	-4627.5	290
1130	S83	-4642.5	171
1131	S82	-4657.5	290
1132	S81	-4672.5	171
1133	S80	-4687.5	290
1134	S79	-4702.5	171
1135	S78	-4717.5	290
1136	S77	-4732.5	171
1137	S76	-4747.5	290
1138	S75	-4762.5	171
1139	S74	-4777.5	290
1140	S73	-4792.5	171
1141	S72	-4807.5	290
1142	S71	-4822.5	171
1143	S70	-4837.5	290
1144	S69	-4852.5	171
1145	S68	-4867.5	290
1146	S67	-4882.5	171
1147	S66	-4897.5	290
1148	S65	-4912.5	171
1149	S64	-4927.5	290
1150	S63	-4942.5	171
1151	S62	-4957.5	290
1152	S61	-4972.5	171
1153	S60	-4987.5	290
1154	S59	-5002.5	171
1155	S58	-5017.5	290
1156	S57	-5032.5	171
1157	S56	-5047.5	290
1158	S55	-5062.5	171
1159	S54	-5077.5	290
1160	S53	-5092.5	171
1161	S52	-5107.5	290
1162	S51	-5122.5	171
1163	S50	-5137.5	290
1164	S49	-5152.5	171
1165	S48	-5167.5	290
1166	S47	-5182.5	171
1167	S46	-5197.5	290
1168	S45	-5212.5	171
1169	S44	-5227.5	290
1170	S43	-5242.5	171
1171	S42	-5257.5	290
1172	S41	-5272.5	171
1173	S40	-5287.5	290
1174	S39	-5302.5	171
1175	S38	-5317.5	290
1176	S37	-5332.5	171
1177	S36	-5347.5	290
1178	S35	-5362.5	171
1179	S34	-5377.5	290
1180	S33	-5392.5	171
1181	S32	-5407.5	290
1182	S31	-5422.5	171
1183	S30	-5437.5	290
1184	S29	-5452.5	171
1185	S28	-5467.5	290
1186	S27	-5482.5	171
1187	S26	-5497.5	290
1188	S25	-5512.5	171
1189	S24	-5527.5	290
1190	S23	-5542.5	171
1191	S22	-5557.5	290
1192	S21	-5572.5	171
1193	S20	-5587.5	290
1194	S19	-5602.5	171
1195	S18	-5617.5	290
1196	S17	-5632.5	171
1197	S16	-5647.5	290
1198	S15	-5662.5	171
1199	S14	-5677.5	290
1200	S13	-5692.5	171

No	Name	X	Y
1201	S12	-5707.5	290
1202	S11	-5722.5	171
1203	S10	-5737.5	290
1204	S9	-5752.5	171
1205	S8	-5767.5	290
1206	S7	-5782.5	171
1207	S6	-5797.5	290
1208	S5	-5812.5	171
1209	S4	-5827.5	290
1210	S3	-5842.5	171
1211	S2	-5857.5	290
1212	S1	-5872.5	171
1213	DUMMY	-5887.5	290
1214	VGLDMY[3]	-6097.5	290
1215	G431	-6112.5	171
1216	G429	-6127.5	290
1217	G427	-6142.5	171
1218	G425	-6157.5	290
1219	G423	-6172.5	171
1220	G421	-6187.5	290
1221	G419	-6202.5	171
1222	G417	-6217.5	290
1223	G415	-6232.5	171
1224	G413	-6247.5	290
1225	G411	-6262.5	171
1226	G409	-6277.5	290
1227	G407	-6292.5	171
1228	G405	-6307.5	290
1229	G403	-6322.5	171
1230	G401	-6337.5	290
1231	G399	-6352.5	171
1232	G397	-6367.5	290
1233	G395	-6382.5	171
1234	G393	-6397.5	290
1235	G391	-6412.5	171
1236	G389	-6427.5	290
1237	G387	-6442.5	171
1238	G385	-6457.5	290
1239	G383	-6472.5	171
1240	G381	-6487.5	290
1241	G379	-6502.5	171
1242	G377	-6517.5	290
1243	G375	-6532.5	171
1244	G373	-6547.5	290
1245	G371	-6562.5	171
1246	G369	-6577.5	290
1247	G367	-6592.5	171
1248	G365	-6607.5	290
1249	G363	-6622.5	171
1250	G361	-6637.5	290
1251	G359	-6652.5	171
1252	G357	-6667.5	290
1253	G355	-6682.5	171
1254	G353	-6697.5	290
1255	G351	-6712.5	171
1256	G349	-6727.5	290
1257	G347	-6742.5	171
1258	G345	-6757.5	290
1259	G343	-6772.5	171
1260	G341	-6787.5	290
1261	G339	-6802.5	171
1262	G337	-6817.5	290
1263	G335	-6832.5	171
1264	G333	-6847.5	290
1265	G331	-6862.5	171
1266	G329	-6877.5	290
1267	G327	-6892.5	171
1268	G325	-6907.5	290
1269	G323	-6922.5	171
1270	G321	-6937.5	290
1271	G319	-6952.5	171
1272	G317	-6967.5	290
1273	G315	-6982.5	171
1274	G313	-6997.5	290
1275	G311	-7012.5	171
1276	G309	-7027.5	290
1277	G307	-7042.5	171
1278	G305	-7057.5	290
1279	G303	-7072.5	171
1280	G301	-7087.5	290
1281	G299	-7102.5	171
1282	G297	-7117.5	290
1283	G295	-7132.5	171
1284	G293	-7147.5	290
1285	G291	-7162.5	171
1286	G289	-7177.5	290
1287	G287	-7192.5	171
1288	G285	-7207.5	290
1289	G283	-7222.5	171
1290	G281	-7237.5	290
1291	G279	-7252.5	171
1292	G277	-7267.5	290
1293	G275	-7282.5	171
1294	G273	-7297.5	290
1295	G271	-7312.5	171
1296	G269	-7327.5	290
1297	G267	-7342.5	171
1298	G265	-7357.5	290
1299	G263	-7372.5	171
1300	G261	-7387.5	290
1301	G259	-7402.5	171
1302	G257	-7417.5	290
1303	G255	-7432.5	171
1304	G253	-7447.5	290
1305	G251	-7462.5	171
1306	G249	-7477.5	290
1307	G247	-7492.5	171
1308	G245	-7507.5	290
1309	G243	-7522.5	171
1310	G241	-7537.5	290
1311	G239	-7552.5	171
1312	G237	-7567.5	290
1313	G235	-7582.5	171
1314	G233	-7597.5	290
1315	G231	-7612.5	171
1316	G229	-7627.5	290
1317	G227	-7642.5	171
1318	G225	-7657.5	290
1319	G223	-7672.5	171
1320	G221	-7687.5	290
1321	G219	-7702.5	171
1322	G217	-7717.5	290
1323	G215	-7732.5	171
1324	G213	-7747.5	290
1325	G211	-7762.5	171
1326	G209	-7777.5	290
1327	G207	-7792.5	171
1328	G205	-7807.5	290
1329	G203	-7822.5	171
1330	G201	-7837.5	290
1331	G199	-7852.5	171
1332	G197	-7867.5	290
1333	G195	-7882.5	171
1334	G193	-7897.5	290
1335	G191	-7912.5	171
1336	G189	-7927.5	290
1337	G187	-7942.5	171
1338	G185	-7957.5	290
1339	G183	-7972.5	171
1340	G181	-7987.5	290
1341	G179	-8002.5	171
1342	G177	-8017.5	290
1343	G175	-8032.5	171
1344	G173	-8047.5	290
1345	G171	-8062.5	171
1346	G169	-8077.5	290
1347	G167	-8092.5	171
1348	G165	-8107.5	290
1349	G163	-8122.5	171
1350	G161	-8137.5	290
1351	G159	-8152.5	171
1352	G157	-8167.5	290
1353	G155	-8182.5	171
1354	G153	-8197.5	290
1355	G151	-8212.5	171
1356	G149	-8227.5	290
1357	G147	-8242.5	171
1358	G145	-8257.5	290
1359	G143	-8272.5	171
1360	G141	-8287.5	290
1361	G139	-8302.5	171
1362	G137	-8317.5	290
1363	G135	-8332.5	171
1364	G133	-8347.5	290
1365	G131	-8362.5	171
1366	G129	-8377.5	290
1367	G127	-8392.5	171
1368	G125	-8407.5	290
1369	G123	-8422.5	171
1370	G121	-8437.5	290
1371	G119	-8452.5	171
1372	G117	-8467.5	290
1373	G115	-8482.5	171
1374	G113	-8497.5	290
1375	G111	-8512.5	171
1376	G109	-8527.5	290
1377	G107	-8542.5	171
1378	G105	-8557.5	290
1379	G103	-8572.5	171
1380	G101	-8587.5	290
1381	G99	-8602.5	171
1382	G97	-8617.5	290
1383	G95	-8632.5	171
1384	G93	-8647.5	290
1385	G91	-8662.5	171
1386	G89	-8677.5	290
1387	G87	-8692.5	171
1388	G85	-8707.5	290
1389	G83	-8722.5	171
1390	G81	-8737.5	290
1391	G79	-8752.5	171
1392	G77	-8767.5	290
1393	G75	-8782.5	171
1394	G73	-8797.5	290
1395	G71	-8812.5	171
1396	G69	-8827.5	290
1397	G67	-8842.5	171
1398	G65	-8857.5	290
1399	G63	-8872.5	171
1400	G61	-8887.5	290
1401	G59	-8902.5	171
1402	G57	-8917.5	290
1403	G55	-8932.5	171
1404	G53	-8947.5	290
1405	G51	-8962.5	171
1406	G49	-8977.5	290
1407	G47	-8992.5	171
1408	G45	-9007.5	290
1409	G43	-9022.5	171
1410	G41	-9037.5	290
1411	G39	-9052.5	171
1412	G37	-9067.5	290
1413	G35	-9082.5	171
1414	G33	-9097.5	290
1415	G31	-9112.5	171
1416	G29	-9127.5	290
1417	G27	-9142.5	171
1418	G25	-9157.5	290
1419	G23	-9172.5	171
1420	G21	-9187.5	290
1421	G19	-9202.5	171
1422	G17	-9217.5	290
1423	G15	-9232.5	171
1424	G13	-9247.5	290
1425	G11	-9262.5	171
1426	G9	-9277.5	290
1427	G7	-9292.5	171
1428	G5	-9307.5	290
1429	G3	-9322.5	171
1430	G1	-9337.5	290
1431	VGLDMY[4]	-9352.5	171
1432	DUMMY	-9367.5	290
1433	DUMMYR3	-9382.5	171
1434	DUMMYR4	-9397.5	290

5. Pin Function

Table 2 Interface

<table>
<tr><th>Signal</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>IM2-1,
IM0/ID</td><td>I</td><td>GND or
IOVCC</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0 /ID</th><th>Interface Mode</th><th>DB Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td></tr>
<tr><td>1</td><td>0</td><td>(ID)</td><td>Clock synchronous serial interface</td><td>SDI, SDO</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>Setting disabled</td><td>-</td></tr>
</table></td><td>-</td></tr>
<tr><td>CSX</td><td>I</td><td>MPU</td><td>Chip select signal. Amplitude: IOVCC-GND
Low: the RM68080 is selected and accessible
High: the RM68080 is not selected and not accessible.</td><td>GND</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal. Amplitude: IOVCC-GND
Low: select Index or status register
High: select control register
Fix to either IOVCC or GND when not in use</td><td>IOVCC</td></tr>
<tr><td>WRX_SCL</td><td>I</td><td>MPU</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when nWR is low. Synchronous clock signal (SCL) in serial interface operation.
Amplitude: IOVCC-GND</td><td>IOVCC</td></tr>
<tr><td>RDX</td><td>I</td><td>MPU</td><td>Read strobe signal in 80-system bus interface operation and enables read operation when RDX is low.
Amplitude: IOVCC-GND</td><td>IOVCC</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>Serial data input (SDI) pin in serial interface operation. The data is inputted and latched on the rising edge of the SCL signal.
Amplitude: IOVCC-GND</td><td>GND or
IOVCC</td></tr>
<tr><td>SDO</td><td>O</td><td>MPU</td><td>Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal.
Amplitude: IOVCC-GND</td><td>Open</td></tr>
<tr><td>DB0-DB17</td><td>I/O</td><td>MPU</td><td>18-bit parallel bi-directional data bus for 80-system interface operation. Amplitude: IOVCC-GND.</td><td>GND or
IOVCC</td></tr>
</table>

			8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-DB1 are used. 18-bit I/F: DB17-DB0 are used. 18-bit parallel bi-directional data bus for RGB interface operation. Amplitude: IOVCC-GND. 16-bit I/F: DB17-DB13 and DB11-DB1 are used. 18-bit I/F: DB17-DB0 are used. Unused pins must be fixed to GND level.	
ENABLE	I	MPU	Data enable signal for RGB interface operation. Amplitude: IOVCC-GND. Low: accessible (select) High: Not accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit.	GND or IOVCC
VSYNCX	I	MPU	Frame synchronous signal for RGB interface operation.. Amplitude: IOVCC-GND. VSPL = “0”: Active low. VSPL = “1”: Active high.	GND or IOVCC
HSYNCX	I	MPU	Line synchronous signal for RGB interface operation. Amplitude: IOVCC-GND. HSPL = “0”: Active low. HSPL = “1”: Active high.	GND or IOVCC
DOTCLK	I	MPU	Dot clock signal for RGB interface operation. The data input timing is on the rising edge of DOTCLK. Amplitude: IOVCC-GND. DPL = “0”: Input data on the rising edge of DOTCLK DPL = “1”: Input data on the falling edge of DOTCLK	GND or IOVCC
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM. (Amplitude: IOVCC-GND).	Open

Table 3 Reset

Signal	I/O	Connect to	Function	When not in use
RESETX	I	MPU	Reset signal. Initializes the RM68080 when it is low. Make sure to execute a power-on reset when turning on power supply. (internal	GND or IOVCC

			pull high) Amplitude: IOVCC-GND.	
PROTECT	I	MPU	Reset protect signal. When PROTECT is fixed to GND, the hardware is disabled. (internal pull high) Low: Hardware reset is disabled High: Hardware reset is enabled	IOVCC

Table 4 Power supply

Signal	I/O	Connect to	Function	When not in use
AGND	I	Power supply	GND for the analog side: AGND = 0V.	-
GND	I	Power supply	GND for the digital side: GND = 0V.	-
VDD	O	Stabilizing Capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.	-
IOVCC	I	Power supply	Power supply to the interface pins: IM[2:0], RESETX, CSX, WRX, RDX, RS, DB17-0, VSYNCX, HSYNCX, DOTCLK, ENABLE, SCL, SDI, and SDO. IOVCC = 1.65V ~ 3.3V. VCI ≥ IOVCC. In case of COG, connect to VCI on the FPC if IOVCC=VCI, to prevent noise.	-
VCILVL	I	Reference power supply	Connect to an external power supply at the same level as VCI. In case of COG, connect to VCI on the FPC to prevent noise.	
VPP1	I	Power supply	Power supply for OTP	Open or AGND
VGLDMY1-4	O	Unused gate lines	Connect unused gate lines to fix the level at VGL	-

Table 5 Step-up circuit

Signal	I/O	Connect to	Function	When not in use
VCI	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.	-
VCC	I	Power supply	Power supply to the digital circuit. Connect to an external power supply of 2.5V ~ 3.3V.	-
VCI1	O	Stabilizing Capacitor	An internal reference voltage for the step-up circuit1. Make sure to set the VCI1 voltage so that the DDVDH, VGH and VGL voltages are set within the respective specification.	-
DDVDH	O	Stabilizing Capacitor	Power supply for the source driver liquid crystal drive unit and VCOM drive. DDVDH = 4.5V ~ 6.0V	-
VGH	O	Stabilizing Capacitor	Liquid crystal gate driver power supply.	-
VGL	O	Stabilizing Capacitor	Liquid crystal gate driver power supply.	-
VCL	O	Stabilizing Capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = 0.5V ~ -VCI	-
C11A, C11B C12A, C12B	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.	-
C13A, C13B C21A, C21B C22A, C22B	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.	-
VREG1 OUT	O	Stabilizing Capacitor	Output voltage generated from the reference voltage. The voltage level is set with the VRH bits. VREG1OUT is: (1) a source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 4.0 ~ (DDVDH – 0.5)V.	Open

Table 6 LCD drive

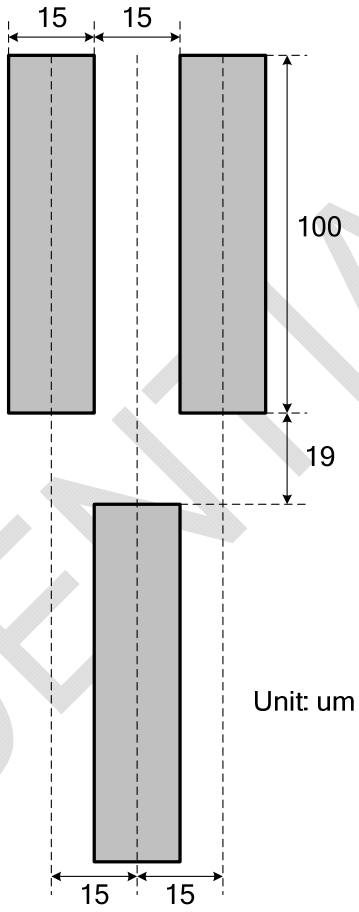
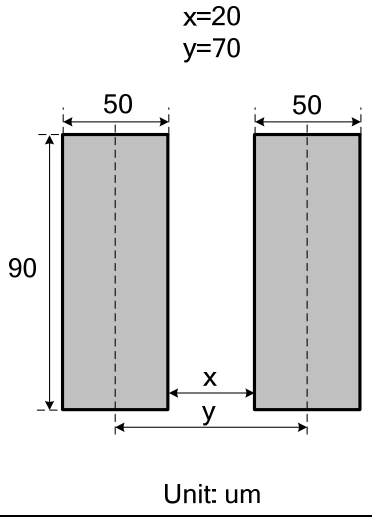
Signal	I/O	Connect to	Function	When not in use
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register.	Open
VCOMH	O	Stabilizing Capacitor	The High level of VCOM amplitude. The output level can be adjusted by either external resistor (VCOMR) or electronic volume. Connect to a stabilizing capacitor.	Open
VCOML	O	Stabilizing Capacitor	The Low level of VCOM amplitude. Adjust the VCOML level with the VDV bits. Make sure to connect to stabilizing capacitor.	Open
VCOMR	I	Variable resistor or open	Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND.	Open
VGS	I	GND or external resistor	Reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.	-
S1~S720	O	LCD	Liquid crystal application voltages. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is outputted from S1. When SS = 1, the data in the RAM address h00000 is outputted from S720.	Open
G1~G432	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level	Open

Table 7 Others (test, dummy pins)

Signal	I/O	Connect to	Function	When not in use
DUMMYR 1 – 4	-	-	DUMMYR1 – 4 are short circuited within the chip for COG contact resistance measurement.	
DUMMY			Dummy pad. Leave these pins as open.	
IOVCCDU M1 – 2	O	-	Connect unused interface and test pins to these pins on the glass to fix voltage levels. Leave open when not used.	-
GNDDUM 1 – 15	O	-		-

VCCDUM	O	-		-
TESTO 1 –16	O	Open	Test pins. Leave them open.	Open
TEST1 – 5	I	Open	Test pins. Connect to GND or leave these pins as open.	GND
TS0 – 4	I	Open	Test pins (internal pull low). Leave them open.	Open
TS5 – 8	O	Open	Test pins.	Open
VCOM	-	Open	Test pin.	Open

6. Bump Arrangement

Pad	Arrangement
Output pins **(No. 263--1434)**	
I/O Pads **(No. 1--262)**	

7. Function Description

7.1 System Interface

The RM68080 supports 80-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and a clock synchronous serial interface. The interface is selected by setting the IM2-0 pins.

The RM68080 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information about control register and internal GRAM. The WDR is the register to temporarily store data to be written to control register and internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the RM68080 performs the first read operation from the internal GRAM. Valid data is read out when the RM68080 performs the second and subsequent read operation.

The instruction execution time except that of starting oscillation takes 0 clock cycle to allow writing instructions consecutively.

Table 8 Register Selection (80-system 8/9/16/18-bit Parallel Interface)

WRX	RDX	RS	Function
0	1	0	Write index to IR
1	0	0	Setting disabled
0	1	1	Write to control register or internal GRAM via WDR
1	0	1	Read from internal GRAM and register via RDR

Table 9 Register Selection (Clock synchronous serial interface)

Start byte		
R/W	RS	Function
0	0	Write index to IR
1	0	Setting disabled
0	1	Write to control register or internal GRAM via WDR
1	1	Read from internal GRAM and register via RDR

Table 10 IM Bit Settings and System Interface

IM2	IM1	IM0	System interface	DB pins	RAM write data	Instruction write transfer
0	0	0	80-system 18-bit interface	DB17-0	Single transfer (18 bits)	Single transfer (16 bits)
0	0	1	80-system 9-bit interface	DB17-9	2 transfers (1st: 9 bits, 2nd: 9 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	0	80-system 16-bit interface	DB17-10, DB8-1	Single transfer (16 bits) 2 transfers (1st: 2 bits, 2nd: 16 bits) 2 transfers (1st: 16 bits, 2nd: 2 bits)	Single transfer (16 bits)
0	1	1	80-system 8-bit interface	DB17-10	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
1	0	*	Clock synchronous serial interface	(SDI, SDO)	2 transfers (1st: 8 bits, 2nd: 8 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
1	1	*	Setting disabled	-	-	-

7.2 External Display Interface (RGB, VSYNC interfaces)

The RM68080 supports RGB interface and VSYNC interface as the external interface to display moving picture. When the RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB17-0) is written in synchronization with these signals when the polarity of enable signal (ENABLE) allows write operation in order to prevent flicker while updating display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, which synchronizes the display operation with the VSYNC signal. The display data is written to the internal GRAM via system interface. When writing data via VSYNC interface, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display interface” section.

The RM68080 allows switching interface by instruction according to the still and/or moving pictures display required. Via the RGB interface, the RM68080 writes all display data to the internal GRAM in order to transfer data only when updating the data and thereby reduce the data transfer and power consumption for moving picture display.

7.3 Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register to set a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As the RM68080 writes data to the internal GRAM, the address in the AC is automatically increased or decreased one step. The window address function enables writing data only within the rectangular area specified in the GRAM.

7.4 Graphics RAM (GRAM)

GRAM is graphics RAM, which can store bit-pattern data of 233,280 (240RGB x 432 x18/8) bytes with 18 bits per pixel.

7.5 Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal driving voltages according to the grayscale data in the γ-correction registers to enable 262k-color display. For details, see the γ-Correction Register section.

7.6 Timing Generator

The timing generator produces timing signals for the operations of internal circuits such as the internal GRAM, source driver, etc. The timing signals for display operations such as RAM read operation and the timing signals for internal operations such as RAM access from the MPU are generated separately in order to avoid mutual interference.

7.7 Oscillator (OSC)

The RM68080 generates the RC oscillation clock by internal RC oscillator circuit. The frame rate is adjusted by the register setting.

7.8 Liquid Crystal Driver Circuit

The liquid crystal driver circuit of the RM68080 consists of a 720-output source driver (S1 ~ S720) and a 432-output gate driver (G1~G432). The display pattern data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the SS bit and the shift direction of gate output from the gate driver can be changed by setting the GS bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for each LCD module.

7.9 Internal Logic Power Supply Regulator

The internal logic power supply regulator generates internal logic power supply VDD.

8. GRAM Address Map and Read/Write

Table 11 GRAM address and display position on the panel (SS = 0, BGR = 0)

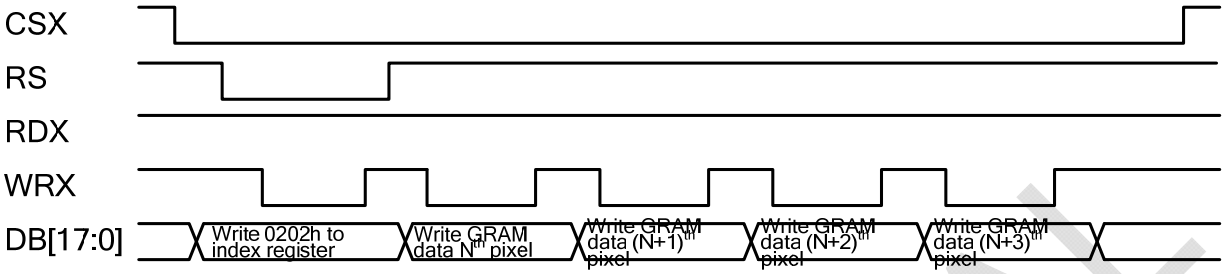
GS=0		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			.....	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G432	h00000			h00001			h00002			h00003			.....	h000EC			h000ED			h000EE			h000EF		
G2	G431	h00100			h00101			h00102			h00103			.....	h001EC			h001ED			h001EE			h001EF		
G3	G430	h00200			h00201			h00202			h00203			.....	h002EC			h002ED			h002EE			h002EF		
G4	G429	h00300			h00301			h00302			h00303			.....	h003EC			h003ED			h003EE			h003EF		
G5	G428	h00400			h00401			h00402			h00403			.....	h004EC			h004ED			h004EE			h004EF		
G6	G427	h00500			h00501			h00502			h00503			.....	h005EC			h005ED			h005EE			h005EF		
G7	G426	h00600			h00601			h00602			h00603			.....	h006EC			h006ED			h006EE			h006EF		
G8	G425	h00700			h00701			h00702			h00703			.....	h007EC			h007ED			h007EE			h007EF		
G9	G424	h00800			h00801			h00802			h00803			.....	h008EC			h008ED			h008EE			h008EF		
G10	G423	h00900			h00901			h00902			h00903			.....	h009EC			h009ED			h009EE			h009EF		
G11	G422	h00A00			h00A01			h00A02			h00A03			.....	h00AEC			h00AED			h00AEE			h00AEF		
G12	G421	h00B00			h00B01			h00B02			h00B03			.....	h00BEC			h00BED			h00BEE			h00BEF		
G13	G420	h00C00			h00C01			h00C02			h00C03			.....	h00CEC			h00CED			h00CEE			h00CEF		
G14	G419	h00D00			h00D01			h00D02			h00D03			.....	h00DEC			h00DED			h00DEE			h00DEF		
G15	G418	h00E00			h00E01			h00E02			h00E03			.....	h00EEC			h00EED			h00EEE			h00EEF		
G16	G417	h00F00			h00F01			h00F02			h00F03			.....	h00FEC			h00FED			h00FEE			h00FEF		
G17	G416	h01000			h01001			h01002			h01003			.....	h010EC			h010ED			h010EE			h010EF		
G18	G415	h01100			h01101			h01102			h01103			.....	h011EC			h011ED			h011EE			h011EF		
G19	G414	h01200			h01201			h01202			h01203			.....	h012EC			h012ED			h012EE			h012EF		
G20	G413	h01300			h01301			h01302			h01303			.....	h013EC			h013ED			h013EE			h013EF		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮			⋮		
G417	G16	h13000			h13001			h13002			h13003			.....	h130EC			h130ED			h130EE			h130EF		
G418	G15	h13100			h13101			h13102			h13103			.....	h131EC			h131ED			h131EE			h131EF		
G419	G14	h13200			h13201			h13202			h13203			.....	h132EC			h132ED			h132EE			h132EF		
G420	G13	h13300			h13301			h13302			h13303			.....	h133EC			h133ED			h133EE			h133EF		
G421	G12	h13400			h13401			h13402			h13403			.....	h134EC			h134ED			h134EE			h134EF		
G422	G11	h13500			h13501			h13502			h13503			.....	h135EC			h135ED			h135EE			h135EF		
G423	G10	h13600			h13601			h13602			h13603			.....	h136EC			h136ED			h136EE			h136EF		
G424	G9	h13700			h13701			h13702			h13703			.....	h137EC			h137ED			h137EE			h137EF		
G425	G8	h13800			h13801			h13802			h13803			.....	h138EC			h138ED			h138EE			h138EF		
G426	G7	h13900			h13901			h13902			h13903			.....	h139EC			h139ED			h139EE			h139EF		
G427	G6	h13A00			h13A01			h13A02			h13A03			.....	h13AEC			h13AED			h13AEE			h13AEF		
G428	G5	h13B00			h13B01			h13B02			h13B03			.....	h13BEC			h13BED			h13BEE			h13BEF		
G429	G4	h13C00			h13C01			h13C02			h13C03			.....	h13CEC			h13CED			h13CEE			h13CEF		
G430	G3	h13D00			h13D01			h13D02			h13D03			.....	h13DEC			h13DED			h13DEE			h13DEF		
G431	G2	h13E00			h13E01			h13E02			h13E03			.....	h13EEC			h13EED			h13EEE			h13EEF		
G432	G1	h13F00			h13F01			h13F02			h13F03			.....	h13FEC			h13FED			h13FEE			h13FEF		

Table 12 GRAM address and display position on the panel (SS = 1, BGR = 1)

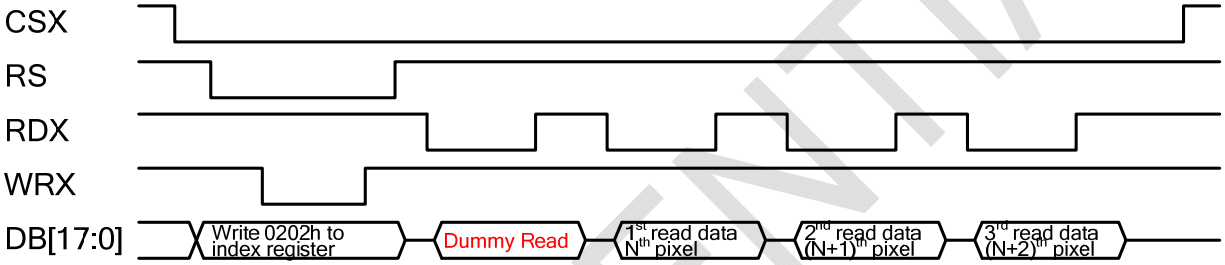
GS=0		S720 S719 S718	S717 S716 S715	S714 S713 S712	S711 S710 S709	.....	S12 S11 S10	S9 S8 S7	S6 S5 S4	S3 S2 S1
GS=0	GS=1	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]	.....	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]
G1	G432	h00000	h00001	h00002	h00003	.....	h000EC	h000ED	h000EE	h000EF
G2	G431	h00100	h00101	h00102	h00103	.....	h001EC	h001ED	h001EE	h001EF
G3	G430	h00200	h00201	h00202	h00203	.....	h002EC	h002ED	h002EE	h002EF
G4	G429	h00300	h00301	h00302	h00303	.....	h003EC	h003ED	h003EE	h003EF
G5	G428	h00400	h00401	h00402	h00403	.....	h004EC	h004ED	h004EE	h004EF
G6	G427	h00500	h00501	h00502	h00503	.....	h005EC	h005ED	h005EE	h005EF
G7	G426	h00600	h00601	h00602	h00603	.....	h006EC	h006ED	h006EE	h006EF
G8	G425	h00700	h00701	h00702	h00703	.....	h007EC	h007ED	h007EE	h007EF
G9	G424	h00800	h00801	h00802	h00803	.....	h008EC	h008ED	h008EE	h008EF
G10	G423	h00900	h00901	h00902	h00903	.....	h009EC	h009ED	h009EE	h009EF
G11	G422	h00A00	h00A01	h00A02	h00A03	.....	h00AEC	h00AED	h00AEE	h00AEF
G12	G421	h00B00	h00B01	h00B02	h00B03	.....	h00BEC	h00BED	h00BEE	h00BEF
G13	G420	h00C00	h00C01	h00C02	h00C03	.....	h00CEC	h00CED	h00CEE	h00CEF
G14	G419	h00D00	h00D01	h00D02	h00D03	.....	h00DEC	h00DED	h00DEE	h00DEF
G15	G418	h00E00	h00E01	h00E02	h00E03	.....	h00EEC	h00EED	h00EEE	h00EEF
G16	G417	h00F00	h00F01	h00F02	h00F03	.....	h00FEC	h00FED	h00FEE	h00FEF
G17	G416	h01000	h01001	h01002	h01003	.....	h010EC	h010ED	h010EE	h010EF
G18	G415	h01100	h01101	h01102	h01103	.....	h011EC	h011ED	h011EE	h011EF
G19	G414	h01200	h01201	h01202	h01203	.....	h012EC	h012ED	h012EE	h012EF
G20	G413	h01300	h01301	h01302	h01303	.....	h013EC	h013ED	h013EE	h013EF
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
G417	G16	h13000	h13001	h13002	h13003	.....	h130EC	h130ED	h130EE	h130EF
G418	G15	h13100	h13101	h13102	h13103	.....	h131EC	h131ED	h131EE	h131EF
G419	G14	h13200	h13201	h13202	h13203	.....	h132EC	h132ED	h132EE	h132EF
G420	G13	h13300	h13301	h13302	h13303	.....	h133EC	h133ED	h133EE	h133EF
G421	G12	h13400	h13401	h13402	h13403	.....	h134EC	h134ED	h134EE	h134EF
G422	G11	h13500	h13501	h13502	h13503	.....	h135EC	h135ED	h135EE	h135EF
G423	G10	h13600	h13601	h13602	h13603	.....	h136EC	h136ED	h136EE	h136EF
G424	G9	h13700	h13701	h13702	h13703	.....	h137EC	h137ED	h137EE	h137EF
G425	G8	h13800	h13801	h13802	h13803	.....	h138EC	h138ED	h138EE	h138EF
G426	G7	h13900	h13901	h13902	h13903	.....	h139EC	h139ED	h139EE	h139EF
G427	G6	h13A00	h13A01	h13A02	h13A03	.....	h13AEC	h13AED	h13AEE	h13AEF
G428	G5	h13B00	h13B01	h13B02	h13B03	.....	h13BEC	h13BED	h13BEE	h13BEF
G429	G4	h13C00	h13C01	h13C02	h13C03	.....	h13CEC	h13CED	h13CEE	h13CEF
G430	G3	h13D00	h13D01	h13D02	h13D03	.....	h13DEC	h13DED	h13DEE	h13DEF
G431	G2	h13E00	h13E01	h13E02	h13E03	.....	h13EEC	h13EED	h13EEE	h13EEF
G432	G1	h13F00	h13F01	h13F02	h13F03	.....	h13FEC	h13FED	h13FEE	h13FEF

i80 18/16bit System Bus Interface Timing

(a) Write to GRAM

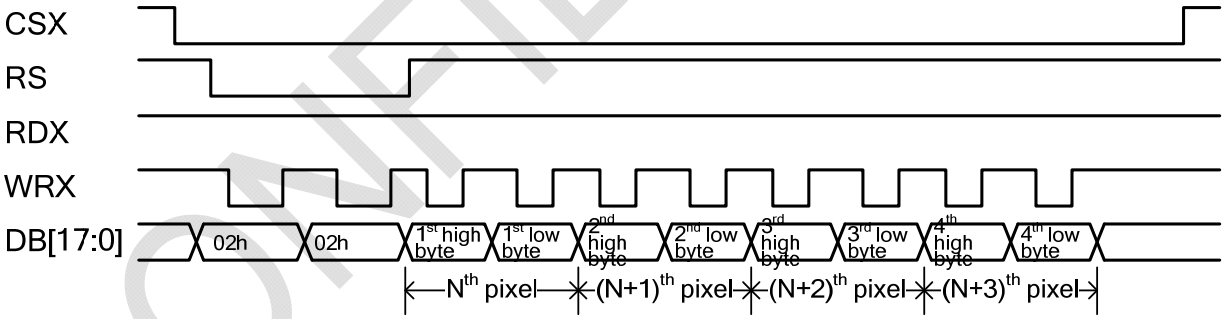


(b) Read from GRAM

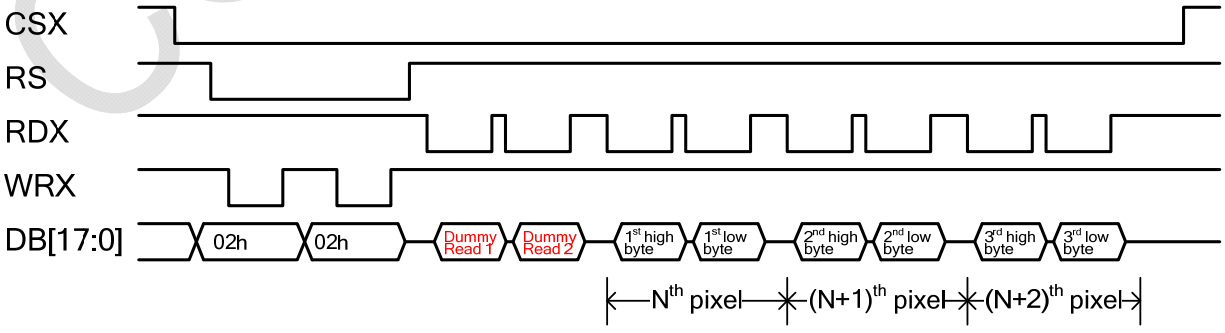


i80 9/8bit System Bus Interface Timing

(a) Write to GRAM



(b) Read from GRAM



9. Instruction

9.1 Outline

The RM68080 adopts 18-bit bus architecture in order to interface to high-performance microcomputer in high speed. All the functional blocks of RM68080 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (RDX/WRX) and data bus D17-0 are used to read/write the instructions and data of RM68080. When accessing the RM68080's internal RAM, data is processed in units of 18 bits. The following are the categories of instruction in RM68080.

1. Specify the index of register
2. Display control
3. Power management control
4. Set internal GRAM address
5. Transfer data to and from the internal GRAM
6. Window address control
7. γ -correction
8. Panel display control

The internal GRAM address is updated automatically as data is written to the internal GRAM, which, in combination with the window address function, contributes to minimizing data transfer and thereby lessens the loading on the microcomputer. The RM68080 writes instructions consecutively by executing the instruction within the cycle when it is written, meanwhile, there is no instruction execution time required.

9.2 Instruction Data Format

The data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface. For more details, please refer to section of "System Interface".

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface.

9.3 Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	*	*	*	*	*	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index R000h to R7FFh of the control register or RAM control to be accessed using a binary number from “000_0000_0000” to “111_1111_1111”. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

9.4 ID code (R000h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RO	1	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0

The ID code “6808”h is outputted when this register is read.

9.5 Display control

9.5.1 Driver Output Control (R001h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shift from S1 to S720.

When SS = “1”, the source driver output shift from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, RGB dots are assigned one to one from S1 to S720.

When SS = “1” and BGR = “1”, RGB dots are assigned one to one from S720 to S1.

When changing the SS or BGR bits, RAM data must be rewritten.

SM: Controls the scan mode in combination with GS setting. See “Scan mode setting”.

9.5.2 LCD Driving Wave Control (R002h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	BC0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BC0: Selects the liquid crystal drive waveform VCOM..

BC0 = 0: frame inversion waveform is selected.

BC0 = 1: line inversion waveform is selected.

9.5.3 Entry Mode (R003h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I//D1	I/D0	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the RM68080 writes data to the internal GRAM.
AM = “0”, sets the horizontal direction.
AM = “1”, sets the vertical direction.
When making a window address area, the data is written only within the area in the direction determined by I/D[1:0] and AM.

I/D[1:0]: Either increments or decrements the address counter automatically as the data is written to the GRAM. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]).

ORG: Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data within the window address area using high-speed RAM write function. Also see Figure 3 and Figure 4.
ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.
ORG = 1: The origin address “h00000” is moved according to the I/D[1:0] setting.

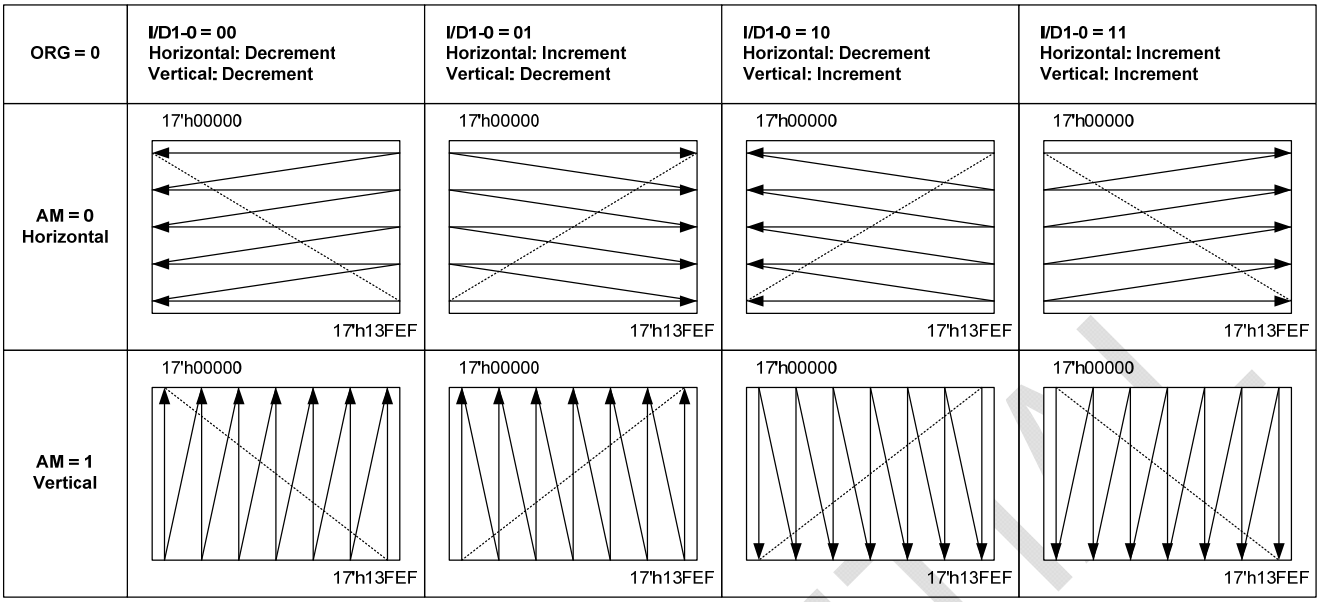


Figure 1 Automatic address update (ORG = 0, AM, ID)

Note: When writing data within the window address area with ORG = 0, any address within the window address area can be designated as the starting point of RAM write operation.

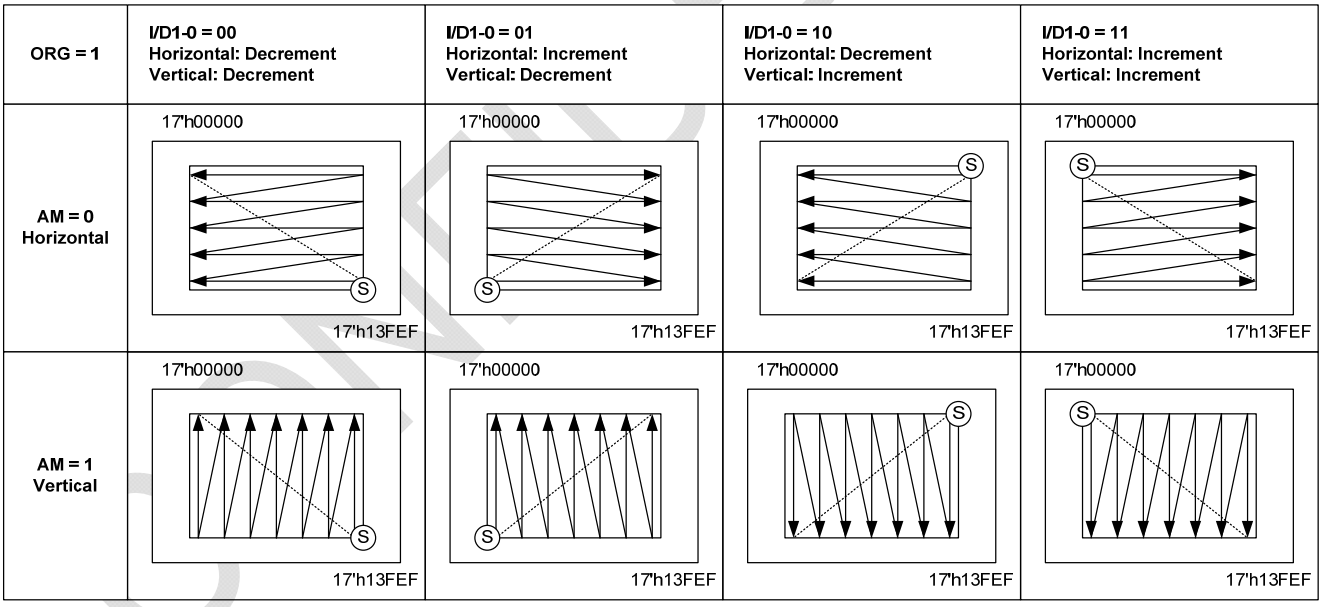


Figure 2 Automatic address update (ORG = 1, AM, ID)

Note: 1. When ORG = 1, make sure to set the address “h00000” in the RAM address set registers (R210h, R21h). Setting other addresses is inhibited. 2. When ORG = 1, the starting point of writing data within the window address area can be set at either corner of the window address area (“S” in circle in the above figure).

BGR: Reverse the order from RGB to BGR in writing 18-bit pixel data in the GRAM.

BGR = 0: Write data in the order of RGB to the GRAM.

BGR = 1: Reverse the order from RGB to BGR in writing data to the GRAM.

BGR = 0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR = 1

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

DFM: In combination with the TRI setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface.

TRI: Selects the format to transfer data bits via 16-bit or 8-bit interface.

In 16-bit bus interface operation,

TRI = 0: 16-bit RAM data is transferred in one transfer.

TRI = 1: 18-bit RAM data is transferred in two transfers.

In 8-bit interface operation,

TRI = 0: 16-bit RAM data is transferred in two transfers.

TRI = 1: 18-bit RAM data is transferred in three transfers.

In SPI interface operation,

TRI = 0: 16-bit RAM data is transferred in two transfers.

TRI = 1: 18-bit RAM data is transferred in three transfers.

9.5.4 Display Control 1 (R007h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	PTDE	0	0	0	BASEE	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The RM68080 drives liquid crystal with non-lit display level or drives only partial image display areas.

BASEE = 1: A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

PTDE: PTDE is the display enable bit of partial image.

When PTDE = 0, the partial image is turned off and only base image is displayed on the screen.

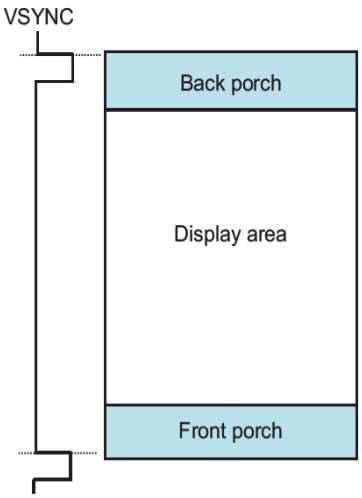
When PTDE = 1, the partial image is displayed on the screen. In this case, turn off the base image by setting BASEE = 0.

9.5.5 Display Control 2 (R008h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	BP7	BP6	BP5	BP4	BP3	BP2	BP1	BP0
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP [7:0] / BP [7:0]: Sets the number of lines for a front porch period / back porch period (a blank period following the end of display / (a blank period made before the beginning of display).
In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

FP[7:0] BP[7:0]	Front Porch period (Line periods)	Back Porch period (Line periods)
8'h00	Setting disabled	Setting disabled
8'h01	Setting disabled	Setting disabled
8'h02	Setting disabled	2 lines
8'h03	3 lines	3 lines
8'h04	4 lines	4 lines
8'h05	5 lines	5 lines
8'h06	6 lines	6 lines
8'h07	7 lines	7 lines
8'h08	8 lines	8 lines
8'h09	9 lines	9 lines
8'h0A	10 lines	10 lines
…	…	…
8'h7F	127 lines	127 lines
8'h80	128 lines	128 lines
8'h81	Setting disabled	Setting disabled
…	…	…
8'hFF	Setting disabled	Setting disabled



Note : The output timing to the LCD panel is delayed by two line periods from the synchronous signal (VSYNC) input timing.

9.5.6 Display Control 3 (R009h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	PTV	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

ISC [3:0]: Set the scan cycle when setting PTG[1:0]="10" to selects interval scan. The scan cycle is defined by from 0 to 31 as table below. The polarity is inverted in the same timing every interval scan cycle.

ISC[3:0]	Scan cycle	Time for interval when (f_{FLM}) = 60Hz
4'h0	0 frames	17 ms
4'h1	3 frames	50 ms
4'h2	5 frames	84 ms
4'h3	7 frames	117 ms
4'h4	9 frames	150 ms
4'h5	11 frames	184 ms
4'h6	13 frames	217 ms
4'h7	15 frames	251 ms
4'h8	17 frames	284 ms
4'h9	19 frames	317 ms
4'hA	21 frames	351 ms
4'hB	23 frames	384 ms
4'hC	25 frames	418 ms
4'hD	27 frames	451 ms
4'hE	29 frames	484 ms
4'hF	31 frames	517 ms

PTG[1:0]: Sets the scan mode in non-display area. The scan mode selected by PTG[1:0] bits is applied in the non-display area when the base image is turned off and the non-display area other than the first and second partial display areas.

PTG1	PTG0	Gate in non-display area	Source in non-display area	VCOM output
0	0	Normal scan	PTS[2:0] setting	PTS[2:0] setting
0	1	Setting disabled	-	-
1	0	Interval scan	PTS[2:0] setting	PTS[2:0] setting
1	1	Setting disabled	-	-

PTS[2:0]: Sets the source output level in non-display area drive period. When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63.

PTS[1:0]	NDL	Gate Scan		Gate not Scan	
		SD	VCOM	SD	VCOM
2'b00	0	Min voltage difference		Min voltage difference	
2'b01		Min voltage difference.		Min voltage difference	
2'b10		GND	GND	GND	GND
2'b11		Hz	Hz	Hz	Hz
2'b00	1	Max voltage difference		Max voltage difference	
2'b01		Max voltage difference		Max voltage difference	
2'b10		GND	GND	GND	GND
2'b11		Hz	Hz	Hz	Hz

PTV: When displaying a partial image, the VCOM waveform control for non-lit area

PTV	VCOM operation waveform in non-lit area
0	Follow the BC setting
1	Frame inversion

9.5.7 Eight Color Control (R00Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	COL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

COL: When COL = 1, the RM68080 displays in 8-colors with low power consumption.

COL	Display color
0	262,144
1	8

9.5.8 External Display Interface Control 1 (R00Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	0	RIM
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM: Sets the interface format in RGB interface.

RIM	RGB interface operation	Display color
0	18-bit RGB interface (1 transfer/pixel) via DB17-0	262,144
1	16-bit RGB interface (1 transfer/pixel) via DB17-13 and DB11-1	65,536

Note: Instruction bits are set via system interface.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNCX interface operation mode is prohibited.

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting disabled

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

RM	RAM Access Interface
0	System interface / VSYNC interface
1	RGB interface

ENC[2:0]: Sets the RAM write cycle via RGB interface.

ENC[2:0]	RAM Write Cycle (frame periods)
3'h0	1 frame
3'h1	2 frames
3'h2	3 frames
3'h3	4 frames
3'h4	5 frames
3'h5	6 frames
3'h6	7 frames
3'h7	8 frames

9.5.9 External Display Interface Control 2 (R00Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of DOTCLK pin.

DPL = 0: input data on the rising edge of DOTCLK

DPL = 1: input data on the falling edge of DOTCLK

EPL: Sets the signal polarity of ENABLE pin.

EPL = 0: writes data DB17-0 when ENABLE = "0" and disables data write operation when ENABLE = "1".

EPL = 1: writes data DB17-0 when ENABLE = "1" and disables data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of HSYNCX pin.

HSPL = 0: low active

HSPL = 1: high active

VSPL: Sets the signal polarity of VSYNCX pin.

VSPL = 0: low active

VSPL = 1: high active

9.6 Panel Interface Control Instruction

9.6.1 Panel Interface Control 1 (R010h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	RTNI5	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
Default		0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the RM68080's display operation is synchronized with internal clock.

DIVI[1:0]: Sets the division ratio of the internal clock frequency.

Frame Frequency Calculation

$$Frame\ frequency = \frac{fosc}{Clocks\ per\ line \times division\ ratio \times (line + BP + FP)}[Hz]$$

fosc : RC oscillation frequency

Line : Number of lines to drive the LCD (NL bits)

Division ratio : DIVI

Clocks per line : RTNI

DIVI[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

RTNI[5:0]	Clocks per line
6'h00~6'h0F	Setting inhibited
6'h10	16 clocks
6'h11	17 clocks
6'h12	18 clocks
6'h13	19 clocks
…	…
6'h3D	61 clocks
6'h3E	62 clocks
6'h3F	63 clocks

9.6.2 Panel Interface Control 2 (R011h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	SDTI[2]	SDTI[1]	SDTI[0]
Default		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

NOWI[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation synchronizing with the internal clock.

NOWI[2:0]	Non-overlap period
3'h0	Setting inhibited
3'h1	1 (internal clock)
3'h2	2
3'h3	3

NOWI[2:0]	Non-overlap period
3'h4	4
3'h5	5
3'h6	6
3'h7	7

Note: The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits.

SDTI[2:0]: Set the source output delay from the reference point. For the relationships between gate interface signals, see Liquid Crystal Panel Interface Timing.

SDTI[2:0]	Non-overlap period
3'h0	Setting inhibited
3'h1	1 (internal clock)
3'h2	2
3'h3	3

SDTI[2:0]	Non-overlap period
3'h4	4
3'h5	5
3'h6	6
3'h7	7

Note:

1. The number of clocks in the table setting is measured from the reference point
2. 1 clock = (internal oscillation clock period) x (division ratio)
3. The reference point is the falling edge of gate output

9.6.3 Panel Interface Control 5 (R014h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	PCDIVH [3]	PCDIVH [2]	PCDIVH [1]	PCDIVH [0]	PCDIVL [3]	PCDIVL [2]	PCDIVL [1]	PCDIVL [0]
Default		0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

PCDIVH[2:0], **PCDIVL[2:0]**: When DM=1 and RGB I/F is selected, display operation clock source come from DOTCLKD. PCDIVH and PCDIVL define division ration of DOTCLK to generate DOTCLKD.

PCDIVH is used to define number of DOTCLK in high period of DOTCLKD in units of one clock.

PCDIVL is used to define number of DOTCLK in low period of DOTCLKD in units of one clock.

Write PCDIVH and PCDIVL values so that the display timing is close to that of internal oscillation clock.

PCDIVH[2:0]	High period
3'h0	Setting inhibited
3'h1	1 (DOTCLK clock)
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	7

PCDIVL[2:0]	Low period
3'h0	Setting inhibited
3'h1	1 (DOTCLK clock)
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	7

9.6.4 Panel Interface Control 6 (R020h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DIVE[1:0]: Sets the division ratio of DOTCLK when RM68080 display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Note: Clock frequency for internal operation = DOTCLK / (DIVE x (PCDIVH + PCDIVL)).

9.6.5 Panel Interface Control 7 (R021h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	0	SDTE[2]	SDTE[1]	SDTE[0]
Default		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

NOWE[3:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

NOWE[3:0]	Non-overlap period
4'h0	Setting inhibited
4'h1	1 clock(s)
4'h2	2
4'h3	3
4'h4	4
4'h5	5
4'h6	6
4'h7	7

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH) [DOTCLK].

SDTE[2:0]: Set the source output delay from the reference point when display timing is synchronized with DOTCLK(DM = 2'h1). For the relationships between gate interface signals, see Liquid Crystal Panel Interface Timing.

SDTI[2:0]	Non-overlap period
3'h0	Setting inhibited
3'h1	1 (internal clock)
3'h2	2
3'h3	3

SDTI[2:0]	Non-overlap period
3'h4	4
3'h5	5
3'h6	6
3'h7	7

Note:

1. The number of clocks in the table setting is measured from the reference point
2. 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH) [DOTCLK]
3. The reference point is the falling edge of gate output

9.6.6 Frame Marker Control (R090h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	FMKM	FMI2	FMI1	FMI0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMKM: When FMKM = 1, the RM68080 starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits.

FMI[2]	FMI[1]	FMI[0]	FMARK output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is outputted at the start of back porch period for 1H period .
Make sure the setting restriction 9'h000 ≤ FMP ≤ BP+NL+FP.

FMP[8:0]	FMARK output position
9'h000	0
9'h001	1st line
9'h002	2nd line
…	…
9'h1BD	445rd line
9'h1BE	446th line
9'h1BF	447h line

9.7 Power Control

9.7.1 Power Control 1 (R100h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	BT2	BT1	BT0	0	0	AP1	AP0	0	DSTB	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AP[1:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[1:0] = 2'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	Electricity in LCD drive power supply amplifiers
3'h0	Halt operation
3'h1	0.50
3'h2	0.75
3'h3	1.00

Note: The values in the table represent the ratio of current in respective settings to the current when AP[1:0] = 2'h3.

BT[2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0			Setting inhibited	
3'h1	VCI1 x 2	-VCI1	VCI1 x 6	-VCI1 x 5
3'h2				-VCI1 x 4
3'h3				-VCI1 x 3
3'h4			Setting inhibited	
3'h5	VCI1 x 2	-VCI1	VCI1 x 5	-VCI1 x 5
3'h6				-VCI1 x 4
3'h7				-VCI1 x 3

Notes:

1. Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages.
2. Set the following voltages within the respective ranges:
   DDVDH = 6.0V (max.), VGH = 18.V (max.), VGL = -13.5 (max.), VGH-VGL = 28.0V (max.) and VCL = 3.0 (max.)

DSTB: When DSTB = 1, the RM68080 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not kept when the RM68080 enters the deep standby mode, and they would be reset automatically after exiting deep standby mode.

To exit deep standby mode, CSX pin needs to be toggled from low to high 6 times.

9.7.2 Power Control 2 (R101h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
Default		0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0

DC0[2:0] / DC1[2:0]: Selects the operating frequency of the step-up circuit 1 / step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC0[2:0]	Step-up circuit 1: step-up frequency (f_{DCDC1})
3'h0	halt step-up circuit 1
3'h1	fbclk
3'h2	fbclk /2
3'h3	fbclk /4
3'h4	fbclk /8
3'h5	fbclk /16
3'h6	fbclk /32
3'h7	fbclk

DC1[2:0]	Step-up circuit 2: step-up frequency (f_{DCDC2})
3'h0	halt step-up circuit 2
3'h1	fbclk /32
3'h2	fbclk /64
3'h3	fbclk /128
3'h4	fbclk /256
3'h5	fbclk /32
3'h6	fbclk /32
3'h7	fbclk /32

Note: Make sure the DC0, DC1 setting restriction: $f_{DCDC1} \geq f_{DCDC2}$. "fbclk" is a clock for boost circuit.

VC[2:0]: Sets the ratio factor of VCI to generate the reference voltages VCI1.

VC[2:0]	VCI1 Voltage
3'h0	Disabled
3'h1	VCILVL x 0.94
3'h2	VCILVL x 0.89
3'h3	Disabled
3'h4	Disabled
3'h5	VCILVL x 0.76
3'h6	Disabled
3'h7	VCI x 1.00

9.7.3 Power Control 3 (R102h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	VRH4	VRH3	VRH2	VRH1	VRH0	0	0	VCMR	0	0	PSON	PON	0	0	0	0
Default		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

VRH[4:0]: Sets the factor to generate VREG1OUT from VCI.

VRH[4:0]	VREG1OUT Voltage
5'h00 – 5'h0F	Setting inhibited
5'h10	Halt
5'h11	VCIR x 1.625
5'h12	VCIR x 1.650
5'h13	VCIR x 1.675
5'h14	VCIR x 1.700
5'h15	VCIR x 1.725
5'h16	VCIR x 1.750
5'h17	VCIR x 1.775
5'h18	VCIR x 1.800
5'h19	VCIR x 1.825
5'h1A	VCIR x 1.850
5'h1B	VCIR x 1.875
5'h1C	VCIR x 1.900
5'h1D	VCIR x 1.925
5'h1E	VCIR x 1.950
5'h1F	VCIR x 1.975

Notes:

1. Make sure the VC and VRH setting restrictions: VREG1OUT ≦ (DDVDH-0.5)V.
2. When VCI<2.5V, internal reference voltage will be same as VCI.

VCMR: Select the electrical potential of VCOMH is either set from external resistance (VCOMR pin) or internal electronic volume (VCM[4:0])

VCMR	VCOMH Electrical Potential setting
0	VCOMR (externally supplied)
1	Internal electronic volume

PSON, PON: Turn power supply on. PON and PSON must be set to 1 and start the internal power supply operation. Follow power supply sequence to set PON and PSON bits. (These two bits could be written only)

9.7.4 Power Control 4 (R103h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	VDV4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0]: Select the factor of VREG1OUT to set the amplitude of VCOM alternating voltage from 0.70 to 1.32 xVREG1OUT

VDV[4:0]	VCOM Amplitude	VDV[4:0]	VCOM Amplitude
5'h0	VREG1OUT x 0.70	5'h10	VREG1OUT x 1.02
5'h1	VREG1OUT x 0.72	5'h11	VREG1OUT x 1.04
5'h2	VREG1OUT x 0.74	5'h12	VREG1OUT x 1.06
5'h3	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.08
5'h4	VREG1OUT x 0.78	5'h14	VREG1OUT x 1.10
5'h5	VREG1OUT x 0.80	5'h15	VREG1OUT x 1.12
5'h6	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.14
5'h7	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.16
5'h8	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.18
5'h9	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.20
5'hA	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.22
5'hB	VREG1OUT x 0.92	5'h1B	VREG1OUT x 1.24
5'hC	VREG1OUT x 0.94	5'h1C	VREG1OUT x 1.26
5'hD	VREG1OUT x 0.96	5'h1D	VREG1OUT x 1.28
5'hE	VREG1OUT x 0.98	5'h1E	VREG1OUT x 1.30
5'hF	VREG1OUT x 1.00	5'h1F	VREG1OUT x 1.32

Note:

1. Set VDV[4:0] so that VCOM amplitude becomes 6.0V or less
2. Set VCOML (VCOMH-VCOM amplitude) less than or equals to 0V

9.8 RAM Access Instruction

9.8.1 RAM Address Set (Horizontal Address) (R200h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.8.2 RAM Address Set (Vertical Address) (R201h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the RM68080 writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note: In RGB interface operation (RM = "1"), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

AD[16:0]	GRAM Data Setting
17'h00000 ~ 17'h000EF	Bitmap data on the 1st line
17'h00100 ~ 17'h001EF	Bitmap data on the 2nd line
17'h00200 ~ 17'h002EF	Bitmap data on the 3rd line
17'h00300 ~ 17'h003EF	Bitmap data on the 4th line
17'h00400 ~ 17'h004EF	Bitmap data on the 5th line
..	..
17'h1AC00 ~ 17'h1ACEF	Bitmap data on the 429th line
17'h1AD00 ~ 17'h1ADEF	Bitmap data on the 430th line
17'h1AE00 ~ 17'h1AEEF	Bitmap data on the 431st line
17'h1AF00 ~ 17'h1AFEF	Bitmap data on the 432nd line

9.8.3 Write Data to GRAM (R202h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data WD[17:0] is transferred via different data bus in different interface operation.															

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

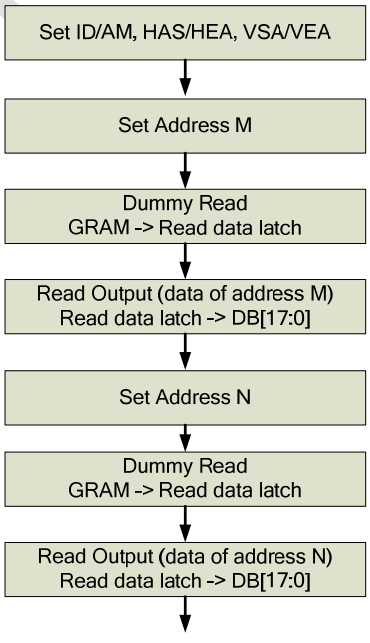
9.8.4 Read Data from GRAM (R202h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	RAM read data RD[17:0] is transferred via different data bus in different interface operation.															

Read 18-bit data from GRAM through the read data register (RDR).

When either 8-bit or 16-bit interface is selected, the LSBs of Rand B dot data are not read out.

Note: This register is disabled in RGB interface operation.

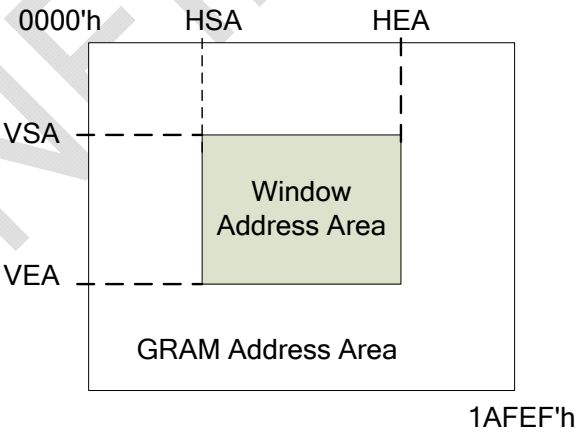


9.8.5 Window Address Write Control Instruction

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R210h	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R211h	W	1	0	0	0	0	0	0	0	0	HEA7	HSA6	HSA5	HEA4	HEA3	HEA2	HEA1	HEA0
R212h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R213h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VSA6	VSA5	VEA4	VEA3	VEA2	VEA1	VEA0
R210h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R211h			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R212h			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R213h			0	0	0	0	0	0	0	1	1	0	1	0	1	1	1	1

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HAS < HEA ≤ 8'hEF and 8'h01 ≤ HEA – HSA.

VSA[8:0], VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h1AF.



Note: The window address range must be within the GRAM address space.

9.9 Power Control 7 (R280h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	1	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	UID7	UID6	UID5	UID4	UID3	UID2	UID1	UID0
Default		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM [5:0]: Set internal VCOMH voltages.

VCM[5:0]	VCOMH Voltage
7'h00	VREG1OUT x 0.492
7'h01	VREG1OUT x 0.496
7'h02	VREG1OUT x 0.500
7'h03	VREG1OUT x 0.504
7'h04	VREG1OUT x 0.508
7'h05	VREG1OUT x 0.512
7'h06	VREG1OUT x 0.516
7'h07	VREG1OUT x 0.520
7'h08	VREG1OUT x 0.524
7'h09	VREG1OUT x 0.528
7'h0A	VREG1OUT x 0.532
7'h0B	VREG1OUT x 0.536
7'h0C	VREG1OUT x 0.540
7'h0D	VREG1OUT x 0.544
7'h0E	VREG1OUT x 0.548
7'h0F	VREG1OUT x 0.552
7'h10	VREG1OUT x 0.556
7'h11	VREG1OUT x 0.560
7'h12	VREG1OUT x 0.564
7'h13	VREG1OUT x 0.568
7'h14	VREG1OUT x 0.572
7'h15	VREG1OUT x 0.576
7'h16	VREG1OUT x 0.580
7'h17	VREG1OUT x 0.584
7'h18	VREG1OUT x 0.588
7'h19	VREG1OUT x 0.592
7'h1A	VREG1OUT x 0.596
7'h1B	VREG1OUT x 0.600
7'h1C	VREG1OUT x 0.604
7'h1D	VREG1OUT x 0.608
7'h1E	VREG1OUT x 0.612
7'h1F	VREG1OUT x 0.616
7'h20	VREG1OUT x 0.620
7'h21	VREG1OUT x 0.624
7'h22	VREG1OUT x 0.628
7'h23	VREG1OUT x 0.632
7'h24	VREG1OUT x 0.636
7'h25	VREG1OUT x 0.640
7'h26	VREG1OUT x 0.644
7'h27	VREG1OUT x 0.648
7'h28	VREG1OUT x 0.652
7'h29	VREG1OUT x 0.656
7'h2A	VREG1OUT x 0.660
7'h2B	VREG1OUT x 0.664

VCM[5:0]	VCOMH Voltage
7'h40	VREG1OUT x 0.748
7'h41	VREG1OUT x 0.752
7'h42	VREG1OUT x 0.756
7'h43	VREG1OUT x 0.760
7'h44	VREG1OUT x 0.764
7'h45	VREG1OUT x 0.768
7'h46	VREG1OUT x 0.772
7'h47	VREG1OUT x 0.776
7'h48	VREG1OUT x 0.780
7'h49	VREG1OUT x 0.784
7'h4A	VREG1OUT x 0.788
7'h4B	VREG1OUT x 0.792
7'h4C	VREG1OUT x 0.796
7'h4D	VREG1OUT x 0.800
7'h4E	VREG1OUT x 0.804
7'h4F	VREG1OUT x 0.808
7'h50	VREG1OUT x 0.812
7'h51	VREG1OUT x 0.816
7'h52	VREG1OUT x 0.820
7'h53	VREG1OUT x 0.824
7'h54	VREG1OUT x 0.828
7'h55	VREG1OUT x 0.832
7'h56	VREG1OUT x 0.836
7'h57	VREG1OUT x 0.840
7'h58	VREG1OUT x 0.844
7'h59	VREG1OUT x 0.848
7'h5A	VREG1OUT x 0.852
7'h5B	VREG1OUT x 0.856
7'h5C	VREG1OUT x 0.860
7'h5D	VREG1OUT x 0.864
7'h5E	VREG1OUT x 0.868
7'h5F	VREG1OUT x 0.872
7'h60	VREG1OUT x 0.876
7'h61	VREG1OUT x 0.880
7'h62	VREG1OUT x 0.884
7'h63	VREG1OUT x 0.888
7'h64	VREG1OUT x 0.892
7'h65	VREG1OUT x 0.896
7'h66	VREG1OUT x 0.900
7'h67	VREG1OUT x 0.904
7'h68	VREG1OUT x 0.908
7'h69	VREG1OUT x 0.912
7'h6A	VREG1OUT x 0.916
7'h6B	VREG1OUT x 0.920

7'h2C	VREG1OUT x 0.668	7'h6C	VREG1OUT x 0.924
7'h2D	VREG1OUT x 0.672	7'h6D	VREG1OUT x 0.928
7'h2E	VREG1OUT x 0.676	7'h6E	VREG1OUT x 0.932
7'h2F	VREG1OUT x 0.680	7'h6F	VREG1OUT x 0.936
7'h30	VREG1OUT x 0.684	7'h70	VREG1OUT x 0.940
7'h31	VREG1OUT x 0.688	7'h71	VREG1OUT x 0.944
7'h32	VREG1OUT x 0.692	7'h72	VREG1OUT x 0.948
7'h33	VREG1OUT x 0.696	7'h73	VREG1OUT x 0.952
7'h34	VREG1OUT x 0.700	7'h74	VREG1OUT x 0.956
7'h35	VREG1OUT x 0.704	7'h75	VREG1OUT x 0.960
7'h36	VREG1OUT x 0.708	7'h76	VREG1OUT x 0.964
7'h37	VREG1OUT x 0.712	7'h77	VREG1OUT x 0.968
7'h38	VREG1OUT x 0.716	7'h78	VREG1OUT x 0.972
7'h39	VREG1OUT x 0.720	7'h79	VREG1OUT x 0.976
7'h3A	VREG1OUT x 0.724	7'h7A	VREG1OUT x 0.980
7'h3B	VREG1OUT x 0.728	7'h7B	VREG1OUT x 0.984
7'h3C	VREG1OUT x 0.732	7'h7C	VREG1OUT x 0.988
7'h3D	VREG1OUT x 0.736	7'h7D	VREG1OUT x 0.992
7'h3E	VREG1OUT x 0.740	7'h7E	VREG1OUT x 0.996
7'h3F	VREG1OUT x 0.744	7'h7F	VREG1OUT x 1.000

UID[7:0]: User defined ID

9.10 γ Control

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R300h	W	1	0	0	0	PR0P01[4]	PR0P01[3]	PR0P01[2]	PR0P01[1]	PR0P01[0]	0	0	0	PR0P00[4]	PR0P00[3]	PR0P00[2]	PR0P00[1]	PR0P00[0]
R301h	W	1	PR0P04[3]	PR0P04[2]	PR0P04[1]	PR0P04[0]	PR0P03[3]	PR0P03[2]	PR0P03[1]	PR0P03[0]	0	0	0	PR0P02[4]	PR0P02[3]	PR0P02[2]	PR0P02[1]	PR0P02[0]
R302h	W	1	0	0	0	PR0P06[4]	PR0P06[3]	PR0P06[2]	PR0P06[1]	PR0P06[0]	0	0	0	0	PR0P05[3]	PR0P05[2]	PR0P05[1]	PR0P05[0]
R303h	W	1	0	0	0	PR0P08[4]	PR0P08[3]	PR0P08[2]	PR0P08[1]	PR0P08[0]	0	0	0	PR0P07[4]	PR0P07[3]	PR0P07[2]	PR0P07[1]	PR0P07[0]
R304h	W	1	0	0	PI0P3[1]	PI0P3[0]	0	0	PI0P2[1]	PI0P2[0]	0	0	PI0P1[1]	PI0P1[0]	0	0	PI0P0[1]	PI0P0[0]
R305h	W	1	0	0	0	PR0N01[4]	PR0N01[3]	PR0N01[2]	PR0N01[1]	PR0N01[0]	0	0	0	PR0N00[4]	PR0N00[3]	PR0N00[2]	PR0N00[1]	PR0N00[0]
R306h	W	1	PR0N04[3]	PR0N04[2]	PR0N04[1]	PR0N04[0]	PR0N03[3]	PR0N03[2]	PR0N03[1]	PR0N03[0]	0	0	0	PR0N02[4]	PR0N02[3]	PR0N02[2]	PR0N02[1]	PR0N02[0]
R307h	W	1	0	0	0	PR0N06[4]	PR0N06[3]	PR0N06[2]	PR0N06[1]	PR0N06[0]	0	0	0	0	PR0N05[3]	PR0N05[2]	PR0N05[1]	PR0N05[0]
R308h	W	1	0	0	0	PR0N08[4]	PR0N08[3]	PR0N08[2]	PR0N08[1]	PR0N08[0]	0	0	0	PR0N07[4]	PR0N07[3]	PR0N07[2]	PR0N07[1]	PR0N07[0]
R309h	W	1	0	0	PI0N3[1]	PI0N3[0]	0	0	PI0N2[1]	PI0N2[0]	0	0	PI0N1[1]	PI0N1[0]	0	0	PI0N0[1]	PI0N0[0]

PR0P00[4:0] Adjusts reference level for positive polarity output R0

PR0N00[4:0] Adjusts reference level for negative polarity output R0

PR0P01[4:0] Adjusts reference level for positive polarity output R1

PR0N01[4:0] Adjusts reference level for negative polarity output R1

PR0P02[4:0] Adjusts reference level for positive polarity output R2

PR0N02[4:0] Adjusts reference level for negative polarity output R2

PR0P03[3:0] Adjusts reference level for positive polarity output R3

PR0N03[3:0] Adjusts reference level for negative polarity output R3

PR0P04[3:0] Adjusts reference level for positive polarity output R4

PR0N04[3:0] Adjusts reference level for negative polarity output R4

PR0P05[3:0] Adjusts reference level for positive polarity output R5

PR0N05[3:0] Adjusts reference level for negative polarity output R5

PR0P06[4:0] Adjusts reference level for positive polarity output R6

PR0N06[4:0] Adjusts reference level for negative polarity output R6

PR0P07[4:0] Adjusts reference level for positive polarity output R7

PR0N07[4:0] Adjusts reference level for negative polarity output R7

PR0P08[4:0] Adjusts reference level for positive polarity output R8

PR0N08[4:0] Adjusts reference level for negative polarity output R8

PI0P0~1[1:0] Adjusts interpolation level for positive polarity output (V2~V7)

PI0N0~1[1:0] Adjusts interpolation level for negative polarity output (V2~V7)

PI0P2~3[1:0] Adjusts interpolation level for positive polarity output (V56~V61)

PI0N2~3[1:0] Adjusts interpolation level for negative polarity output (V56~V61)

Default values of all parameters are 0.

9.11 Base Image Display Control Instruction

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R400h	W	1	GS	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	0
R401h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
R404h	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
R400h	Default		0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
R401h			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R404h			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the RM68080 to display the same image from the same set of data whether the liquid crystal panel is normally black or white.

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	…	…	…
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	…	…	…
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the RM68080 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image
0	Fixed
1	Enable scrolling

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	Number of Lines
6’h00	Setting inhibited
6’h01	16 (lines)
6’h02	24
6’h03	32
6’h04	40
6’h05	48
6’h06	48
6’h07	56
6’h08	64
6’h09	72
6’h0A	80
6’h0B	88
6’h0C	96
6’h0D	104
6’h0E	112
6’h0F	120
6’h10	128
6’h11	136
6’h12	144
6’h13	152

NL[5:0]	Number of Lines
6’h14	160
6’h15	168
6’h16	176
6’h17	184
6’h18	192
6’h19	200
6’h1A	216
6’h1B	224
6’h1C	232
6’h1D	240
6’h1E	248
6’h1F	256
6’h20	264
6’h21	272
6’h22	280
6’h23	288
6’h24	296
6’h25	304
6’h26	312
6’h27	320

NL[5:0]	Number of Lines
6'h28	328
6'h29	336
6'h2A	344
6'h2B	352
6'h2C	360
6'h2D	368
6'h2E	376
6'h2F	384
6'h30	392
6'h31	400
6'h32	408
6'h33	416
6'h34	424
6'h35	432
Others	Setting inhibited

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

SCN[5:0]	Gate Line No (Scan start position)			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6’h00 ~ 6’h26	SCN*8+1	(SCN+NL+1)*8	SCN*16+1	(SCN+NL+1)*16-1
6’h27 ~ 6’h34	SCN*8+1	(SCN+NL+1)*8	(SCN-6’h27)*16+2	(SCN-6’h27+NL+1)*16
6’h35~6’h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

NDL: Sets the source output level in non-lit display area. NDL bit can keep the non-display area lit on.

NDL	Non-display area	
	Positive	Negative
0	V63	V0
1	V0	V63

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0]. Make sure VL[8:0] ≤ 320.

GS: Sets the direction of scan by the gate driver. Set GS bit in combination with SM and SS bits for the convenience of the display module configuration and the display direction.

9.12 Partial Display Control Instruction

9.12.1 Partial Image 1: Display Position (R500h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTDP[8]	PTDP[7]	PTDP[6]	PTDP[5]	PTDP[4]	PTDP[3]	PTDP[2]	PTDP[1]	PTDP[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.12.2 Partial Image 1: RAM Address (Start Line Address) (R501h), (End Line Address) (R502h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTSA[8]	PTSA[7]	PTSA[6]	PTSA[5]	PTSA[4]	PTSA[3]	PTSA[2]	PTSA[1]	PTSA[0]
W	1	0	0	0	0	0	0	0	PTEA[8]	PTEA[7]	PTEA[6]	PTEA[5]	PTEA[4]	PTEA[3]	PTEA[2]	PTEA[1]	PTEA[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP[8:0]: Sets the display position of partial image.

PTSA[8:0] and PTEA[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image. In setting, make sure that PTSA ≤ PTEA.

9.13 OTP VCM Control

9.13.1 OTP VCM Programming Control 1 (R6F0h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	ID_PGM_EN	VCM_PGM_EN	TE	CALB	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TE: OTP programming enable. When program OTP, must set this bit.

VCM_PGM_EN: VCM[6:0] programming enable. When program VCM[5:0], must set this bit and TE. The VCM[6:0] could be programmed three times.

ID_PGM_EN: UID[7:0] programming enable. When program UID[7:0], must set this bit and TE.

CALB: When CALB=1, all data in OTP is read out and written to internal registers. When finished, CALB is set to 0.

9.13.2OTP VCM Status and Enable (R6F1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0	VM_D 7	VM_D 6	VM_D 5	VM_D 4	VM_D 3	VM_D 2	VM_D 1	VM_D 0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

KEY[7:0]: OTP Programming key protection. Before writing OTP programming enable bits in R6F0h, it must write these bits with 0xA5 value first to make OTP programming successfully. If KEY[7:0] is not written with 0xA5, OTP programming will be fail. See OTP Programming flow.

VM_D[7:0]: OTP programming data for VCM[6:0] or UID[7:0].

10. Instruction List

No.	Register Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	*	*	*	*	*	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
000h	Driver Code Read	RO	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0
001h	Driver Output Control	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
002h	LCD Driving Wave Control	W	1	0	0	0	0	0	0	BC	0	0	0	0	0	0	0	0	0
003h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I//D1	I/D0	AM	0	0	0
007h	Display Control 1	W	1	0	0	0	PTDE	0	0	0	BASEE	0	0	0	0	0	0	0	0
008h	Display Control 2	W	1	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	BP7	BP6	BP5	BP4	BP3	BP2	BP1	BP0
009h	Display Control 3	W	1	0	0	0	0	PTV	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
00Bh	Eight Color Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	COL
00Ch	External Display Interface Control 1	W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	0	RIM
00Fh	External Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
010h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	RTNI5	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
011h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI [2]	NOWI [1]	NOW I[0]	0	0	0	0	0	SDTI[2]	SDTI[1]	SDTI[0]
014h	Panel Interface Control 5	W	1	0	0	0	0	0	0	0	0	PCDIVH [3]	PCDIVH [2]	PCDIVH [1]	PCDIVH [0]	PCDIVL [3]	PCDIVL [2]	PCDIVL [1]	PCDIVL [0]
020h	Panel Interface Control 6	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
021h	Panel Interface Control 7	W	1	0	0	0	0	NOWE [3]	NOWE [2]	NOWE [1]	NOWE [0]	0	0	0	0	0	SDTE [2]	SDTE [1]	SDTE [0]
090h	Frame Marker Control	W	1	FMKM	FMI2	FMI1	FMI0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
100h	Power Control 1	W	1	0	0	0	0	0	BT2	BT1	BT0	0	0	AP1	AP0	0	DSTB	0	0
101h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
102h	Power Control 3	W	1	VRH4	VRH3	VRH2	VRH1	VRH0	0	0	VCMR	0	0	PSON	PON	0	0	0	0
103h	Power Control 4	W	1	0	0	0	VDV4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	0	0	0	0	0	0

200h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
201h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
202h	Write Data to GRAM	RAM write data WD[17:0] / read data RD[17:0] is transferred via different data bus in different interface operation.																	
210h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
211h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HSA6	HSA5	HEA4	HEA3	HEA2	HEA1	HEA0
212h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
213h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VSA6	VSA5	VEA4	VEA3	VEA2	VEA1	VEA0
280h	Power Control 7	W	1	1	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	UID7	UID6	UID5	UID4	UID3	UID2	UID1	UID0
300h	Gamma Control 1	W	1	0	0	0	PR0P01[4]	PR0P01[3]	PR0P01[2]	PR0P01[1]	PR0P01[0]	0	0	0	PR0P00[4]	PR0P00[3]	PR0P00[2]	PR0P00[1]	PR0P00[0]
301h	Gamma Control 2	W	1	PR0P04[3]	PR0P04[2]	PR0P04[1]	PR0P04[0]	PR0P03[3]	PR0P03[2]	PR0P03[1]	PR0P03[0]	0	0	0	PR0P02[4]	PR0P02[3]	PR0P02[2]	PR0P02[1]	PR0P02[0]
302h	Gamma Control 3	W	1	0	0	0	PR0P06[4]	PR0P06[3]	PR0P06[2]	PR0P06[1]	PR0P06[0]	0	0	0	0	PR0P05[3]	PR0P05[2]	PR0P05[1]	PR0P05[0]
303h	Gamma Control 4	W	1	0	0	0	PR0P08[4]	PR0P08[3]	PR0P08[2]	PR0P08[1]	PR0P08[0]	0	0	0	PR0P07[4]	PR0P07[3]	PR0P07[2]	PR0P07[1]	PR0P07[0]
304h	Gamma Control 5	W	1	0	0	PI0P3[1]	PI0P3[0]	0	0	PI0P2[1]	PI0P2[0]	0	0	PI0P1[1]	PI0P1[0]	0	0	PI0P0[1]	PI0P0[0]
305h	Gamma Control 6	W	1	0	0	0	PR0N01[4]	PR0N01[3]	PR0N01[2]	PR0N01[1]	PR0N01[0]	0	0	0	PR0N00[4]	PR0N00[3]	PR0N00[2]	PR0N00[1]	PR0N00[0]
306h	Gamma Control 7	W	1	PR0N04[3]	PR0N04[2]	PR0N04[1]	PR0N04[0]	PR0N03[3]	PR0N03[2]	PR0N03[1]	PR0N03[0]	0	0	0	PR0N02[4]	PR0N02[3]	PR0N02[2]	PR0N02[1]	PR0N02[0]
307h	Gamma Control 8	W	1	0	0	0	PR0N06[4]	PR0N06[3]	PR0N06[2]	PR0N06[1]	PR0N06[0]	0	0	0	0	PR0N05[3]	PR0N05[2]	PR0N05[1]	PR0N05[0]
308h	Gamma Control 9	W	1	0	0	0	PR0N08[4]	PR0N08[3]	PR0N08[2]	PR0N08[1]	PR0N08[0]	0	0	0	PR0N07[4]	PR0N07[3]	PR0N07[2]	PR0N07[1]	PR0N07[0]
309h	Gamma Control 10	W	1	0	0	PI0N3[1]	PI0N3[0]	0	0	PI0N2[1]	PI0N2[0]	0	0	PI0N1[1]	PI0N1[0]	0	0	PI0N0[1]	PI0N0[0]
400h	Driver Output Control 2	W	1	GS	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	0
401h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
404h	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
500h	Partial Image Display Position	W	1	0	0	0	0	0	0	0	PTDP[8]	PTDP[7]	PTDP[6]	PTDP[5]	PTDP[4]	PTDP[3]	PTDP[2]	PTDP[1]	PTDP[0]
501h	Partial Image Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA[8]	PTSA[7]	PTSA[6]	PTSA[5]	PTSA[4]	PTSA[3]	PTSA[2]	PTSA[1]	PTSA[0]
502h	Partial Image Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA[8]	PTEA[7]	PTEA[6]	PTEA[5]	PTEA[4]	PTEA[3]	PTEA[2]	PTEA[1]	PTEA[0]

6F0h	OTP VCM Programming Control	W	1	0	0	0	0	0	0	ID_PGM_EN	VCM_PGM_EN	TE	CALB	0	0	0	0	0	0
6F1h	OTP VCM Status and Enable	W	1	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0	VM_D 7	VM_D 6	VM_D 5	VM_D 4	VM_D 3	VM_D 2	VM_D 1	VM_D 0

11. Interface and Data Format

The RM68080 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The RM68080 can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the RM68080 supports RGB interface and VSYNC interface, which enables data rewrite operation without flicker effect of the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNCX, HSYNCX, and DOTCLK. In synchronization with these signals, the RM68080 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the RM68080's GRAM so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the RAM area to write data for moving picture display, which enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The RM68080 operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register (R00Ch). When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes:

1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.

12. System Interface

The following are the kinds of system interfaces available with the RM68080. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

IM2	IM1	IM0	Interfacing Mode with MPU	DB pins	Colors
0	0	0	80-system 18-bit interface	DB17-0	262K
0	0	1	80-system 9-bit interface	DB17-9	262K
0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262K/65K
0	1	1	80-system 8-bit interface	DB17-10	262K/65K
1	0	ID	Clock synchronous serial interface	(SDI, SDO)	65K
1	1	*	Setting inhibited	-	-

12.1 80-system 18-bit Bus Interface

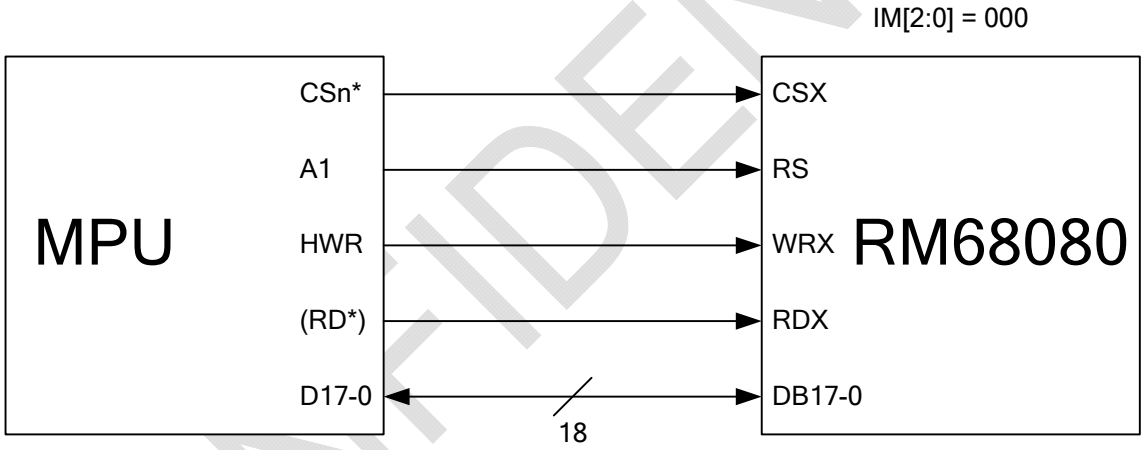


Figure 3 18-bit bus interface for 80-system

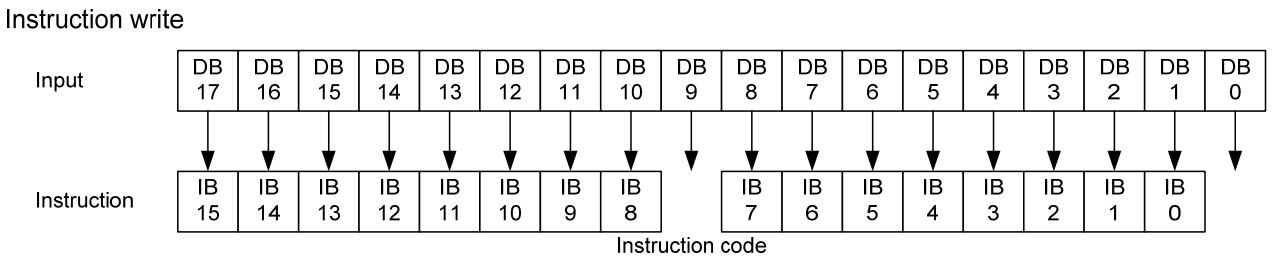


Figure 4 18-bit Interface Data Format (Instruction Write / Instruction Read)

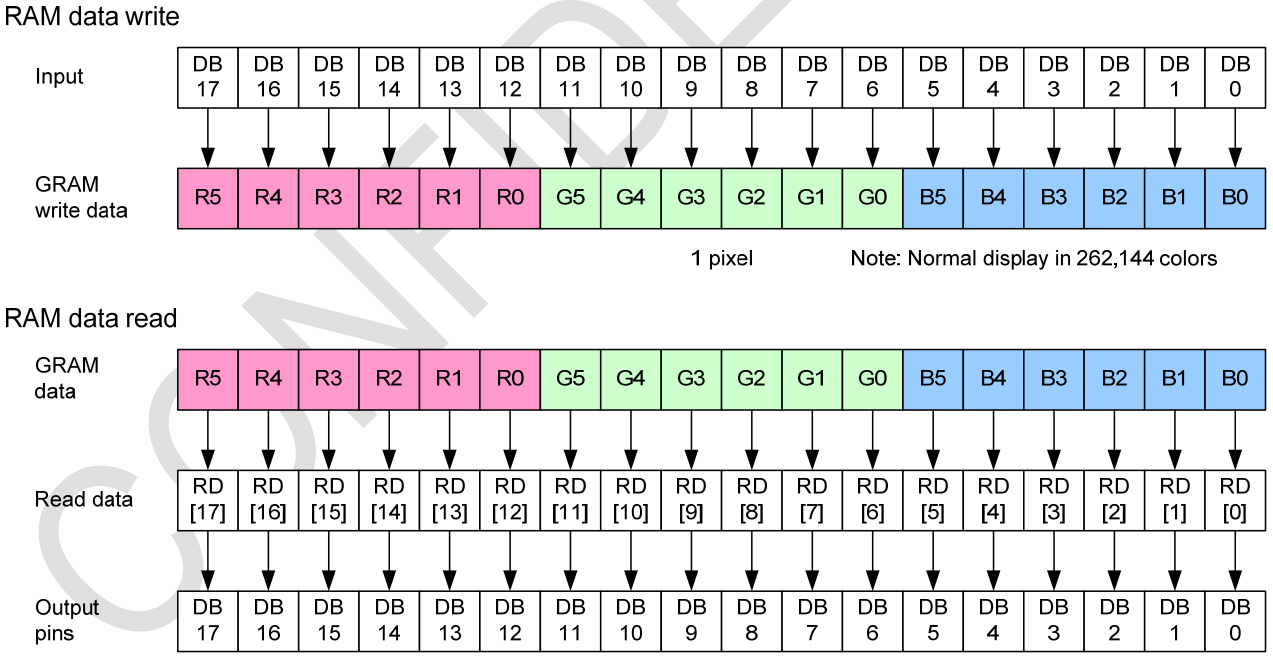


Figure 5 18-bit Interface Data Format (RAM Data Write / RAM Data Read)

12.2 80-system 16-bit Bus Interface

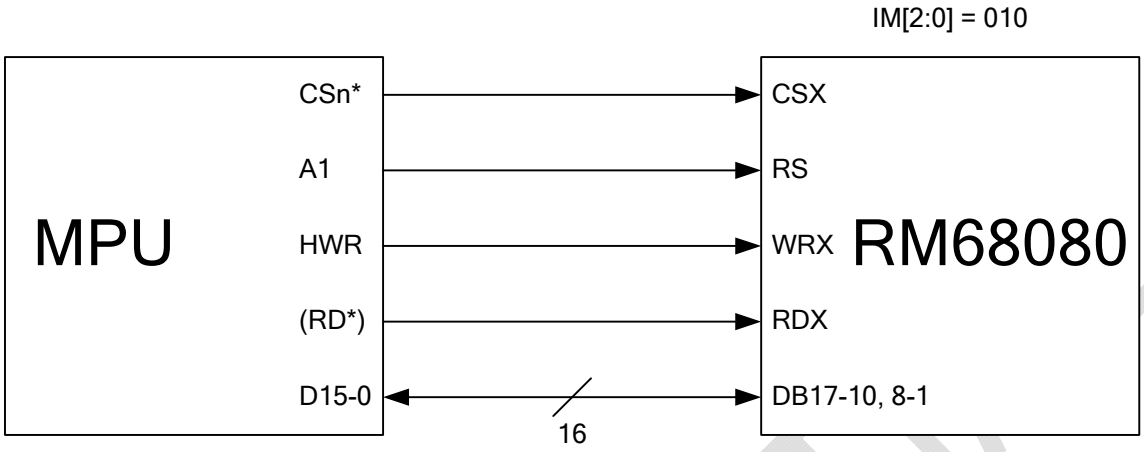


Figure 6 16-bit bus interface for 80-system

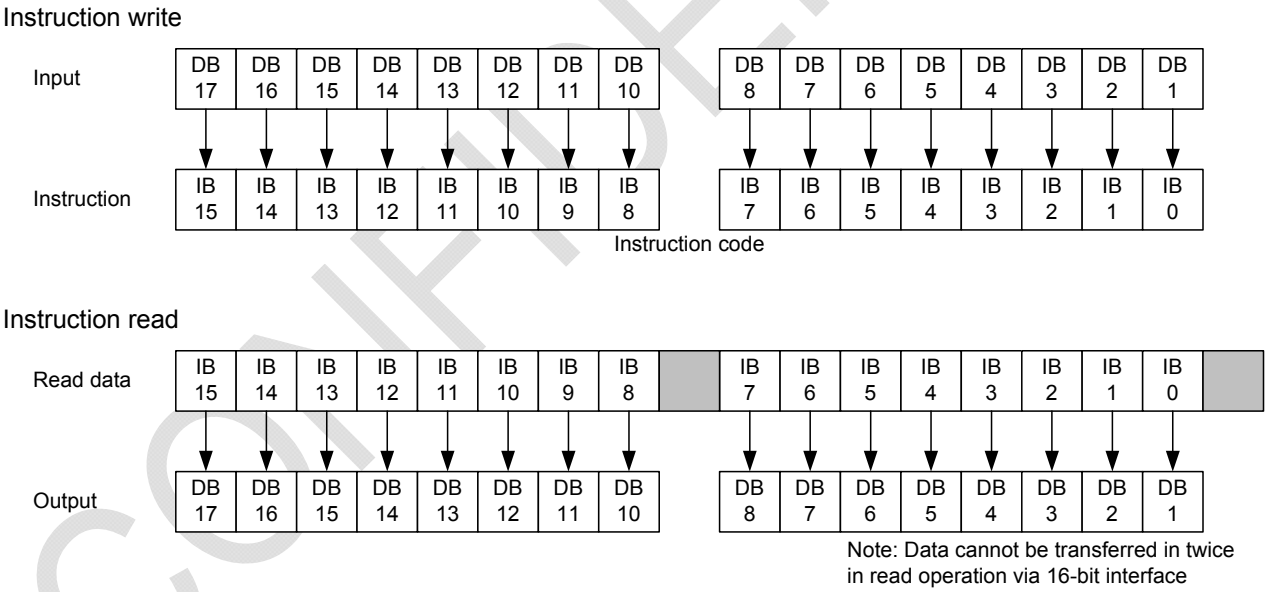
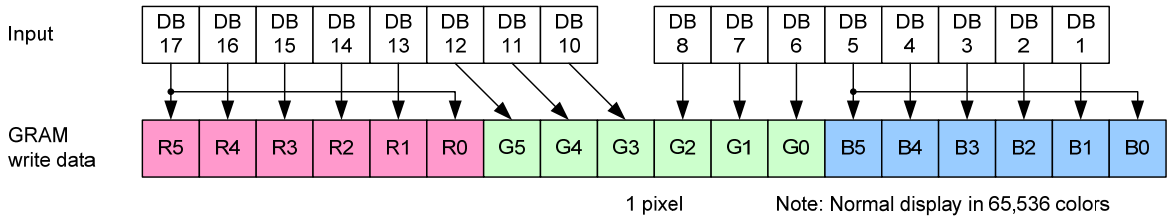
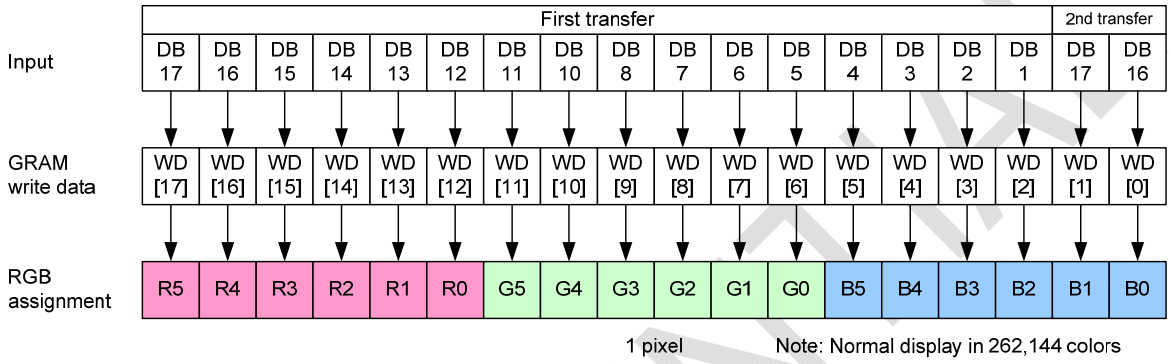


Figure 7 16-bit Interface Data Format (Instruction Write / Instruction Read)

RAM data write (single transfer mode: TRIREG = 0)



RAM data write (2 transfer mode: TRIREG = 1, DFM = 0)



RAM data write (2 transfer mode: TRIREG = 1, DFM = 1)

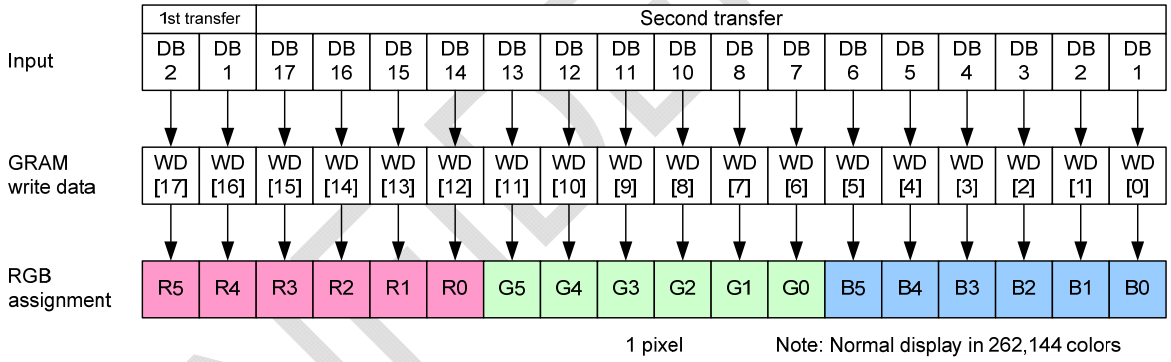


Figure 8 16-bit Interface Data Format (RAM data write)

RAM data read (single transfer: TRIREG = 0)

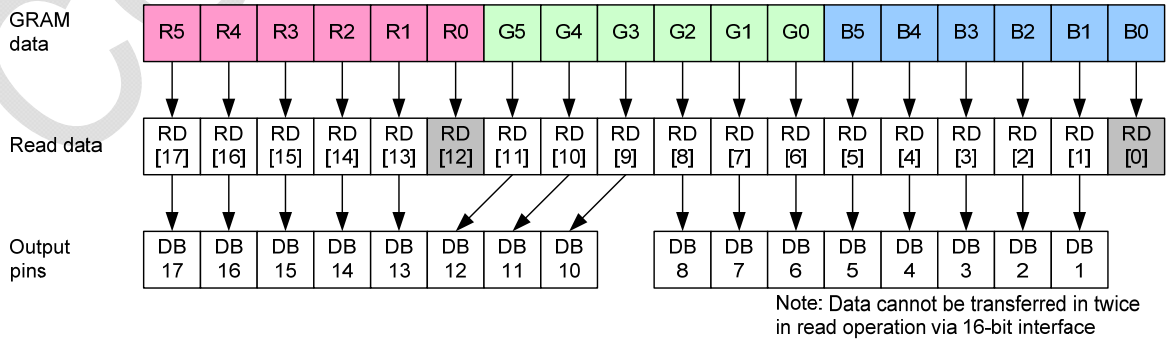


Figure 9 16-bit Interface Data Format (RAM data read)

12.3 80-system 9-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either IOVCC or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

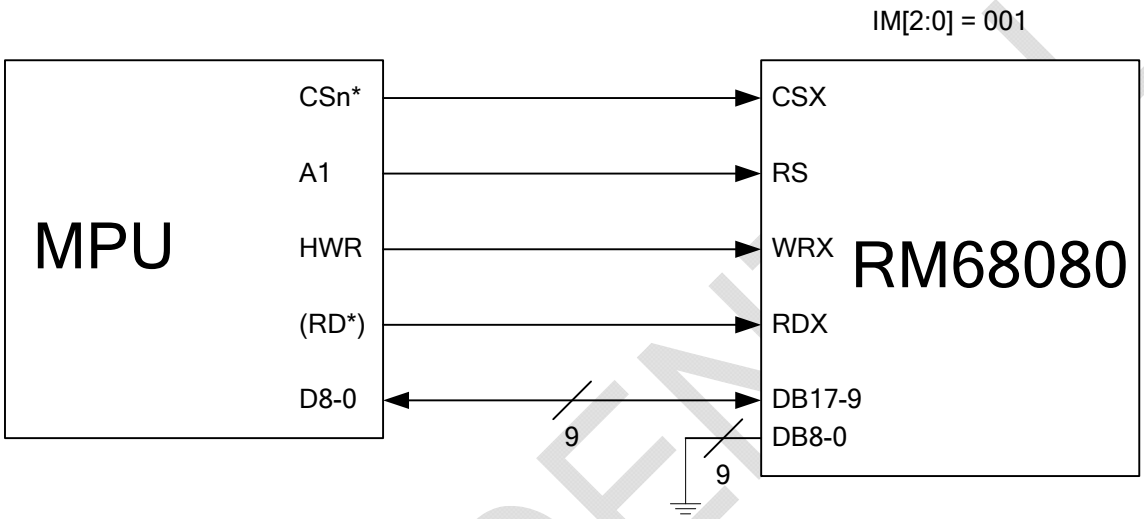


Figure 10 9-bit bus interface for 80-system

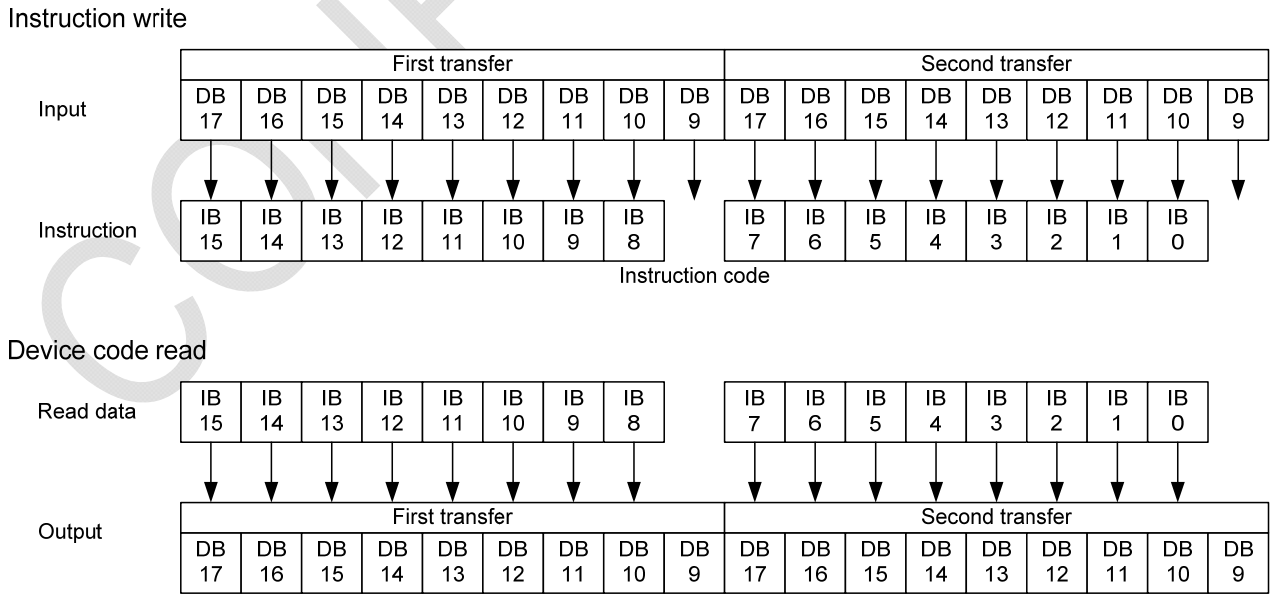
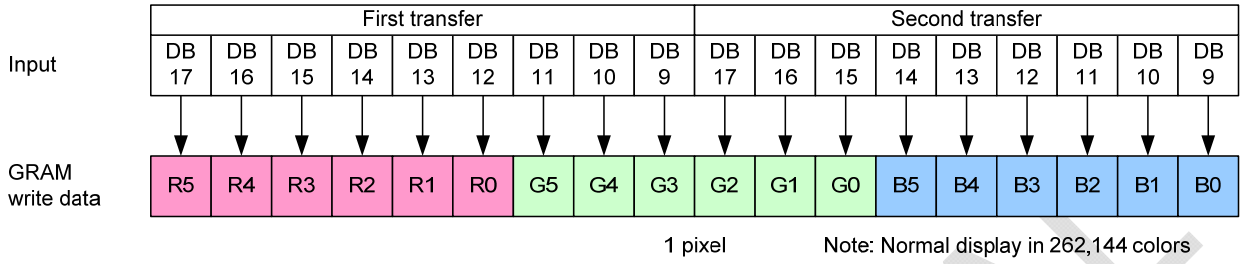


Figure 11 9-bit Interface Data Format (Instruction Write / Device Code Read)

RAM data write



RAM data read

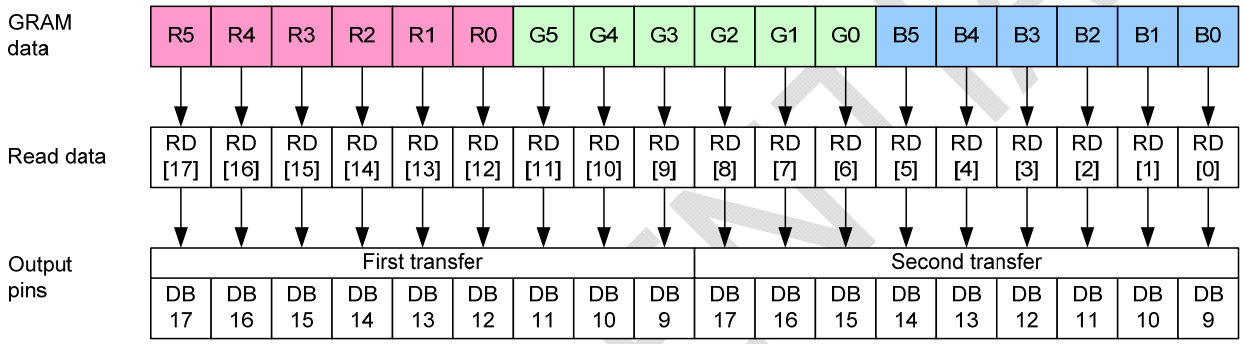


Figure 12 9-bit Interface Data Format (RAM Data Write / RAM Data Read)

12.4 80-system 8-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either IOVCC or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

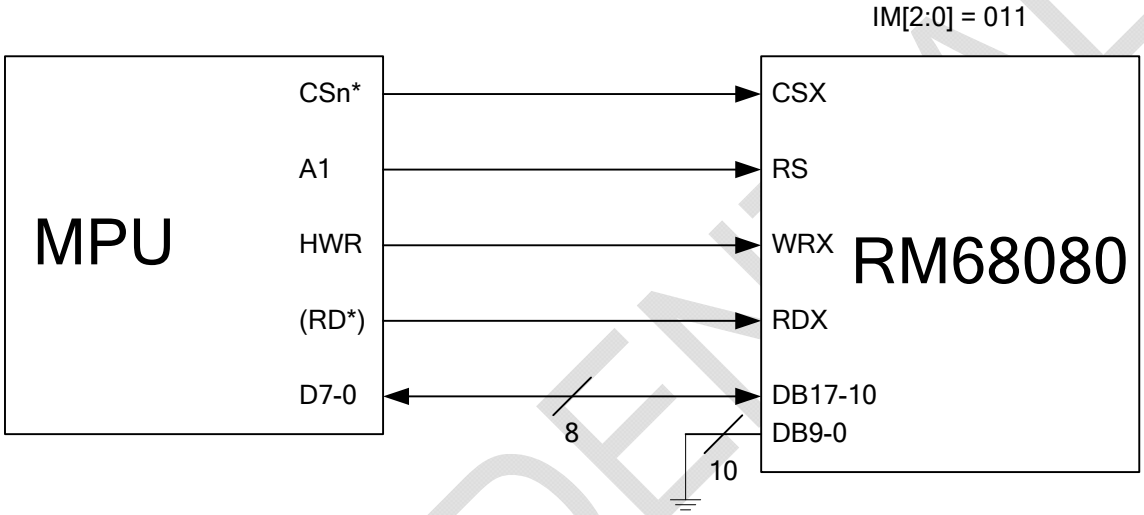


Figure 13 8-bit bus interface for 80-system

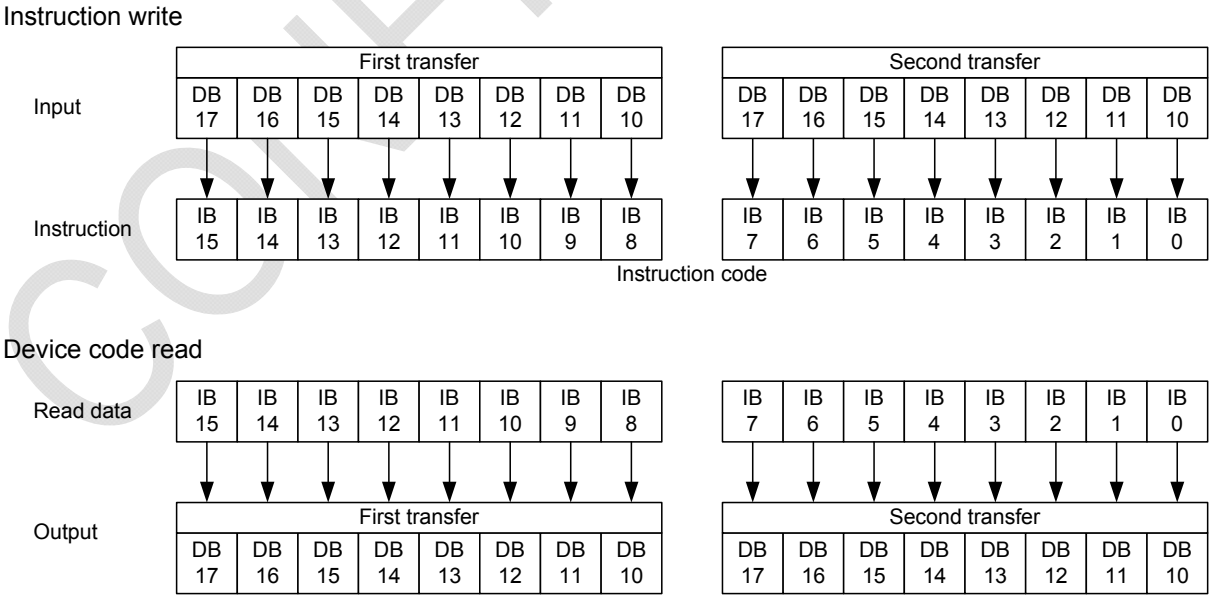
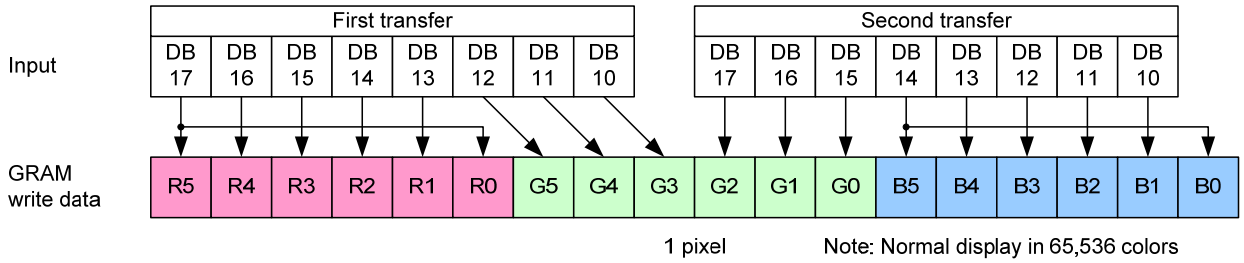
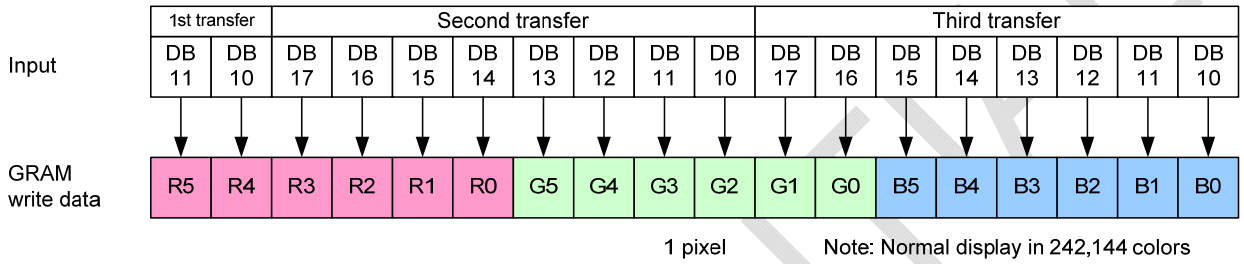


Figure 14 8-bit Interface Data Format (Instruction Write / Device Code Read)

RAM data write (2-transfer mode: TRIREG = 0)



RAM data write (3-transfer mode: TRIREG = 1, DFM = 0)



RAM data write (3-transfer mode: TRIREG = 1, DFM = 1)

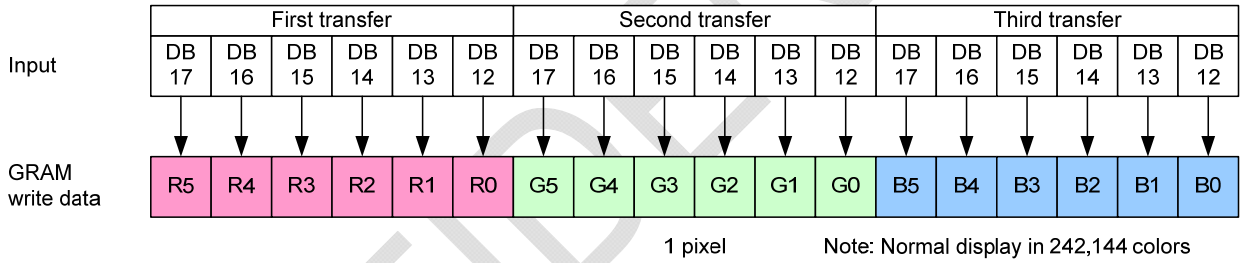


Figure 15 8-bit Interface Data Format (RAM Data Write)

RAM data read

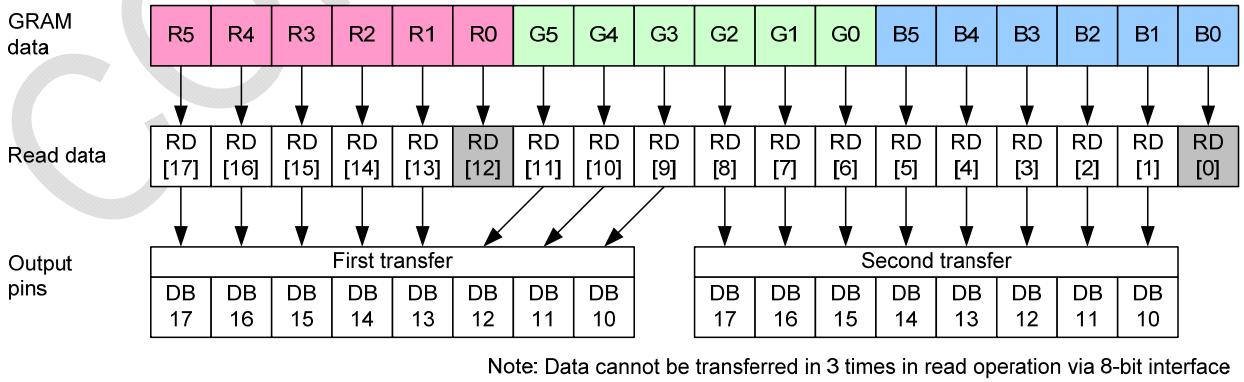
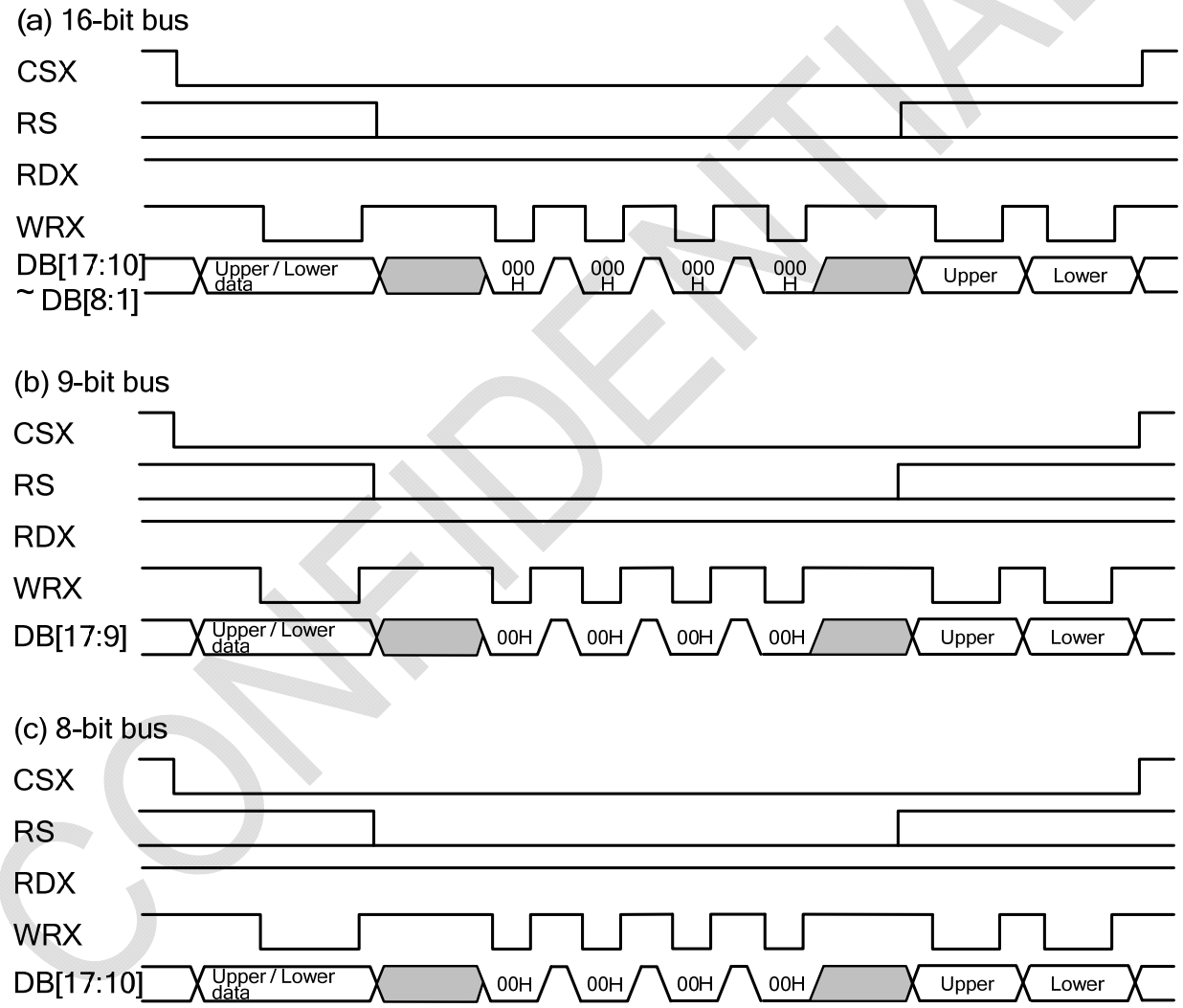


Figure 16 8-bit Interface Data Format (RAM Data Read)

12.5 Data Transfer Synchronization in 80-System

The RM68080 supports data transfer synchronization function to reset the counters for data transfers in 8-/9-/16-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H/000H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper part of the data. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Data Transfer Synchronization in i80-System



12.6 Serial Interface

The serial interface is selected by setting the IM2/1 pins to the IOVCC/GND levels, respectively. The data is transferred via chip select line (CSX), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVCC or GND level.

The SPI interface operation enables from the falling edge of CSX and ends of data transfer on the rising edge of CSX. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by RM68080.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, RM68080 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the RM68080 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Table 13 Start Byte Format

Transferred Bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: The ID bit is determined by setting the IM0/ID pin.

Table 14 Functions of RS, R/W bits

RS	R/W	Function
0	0	Set index register
0	1	Read a status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

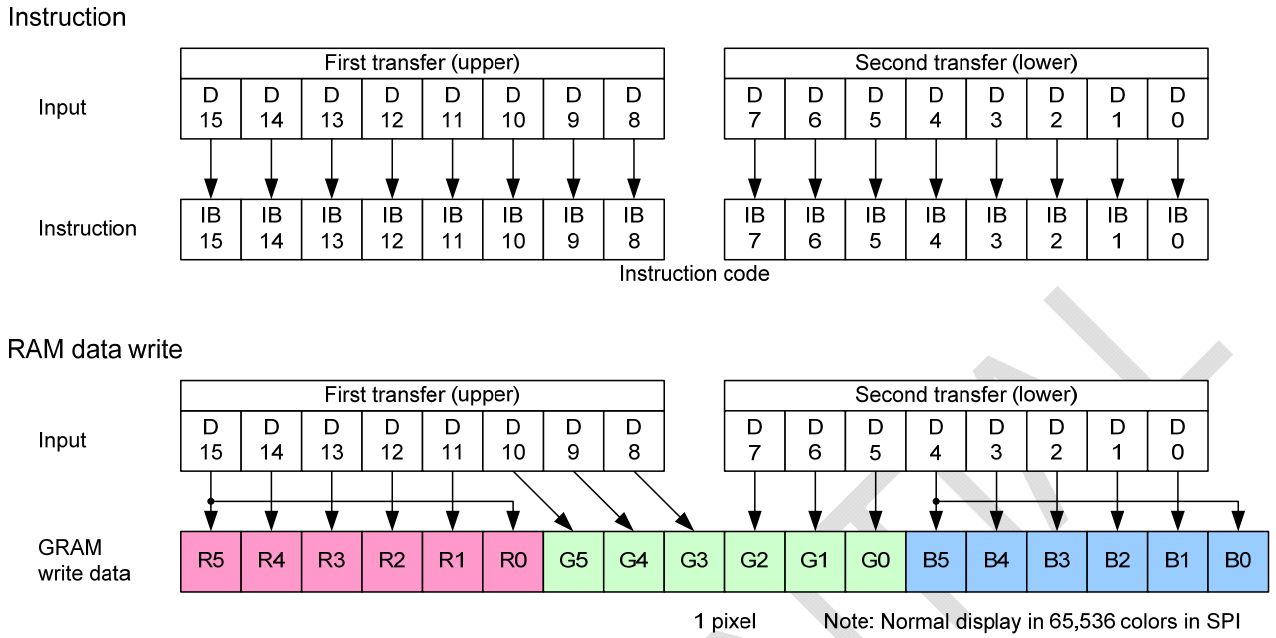
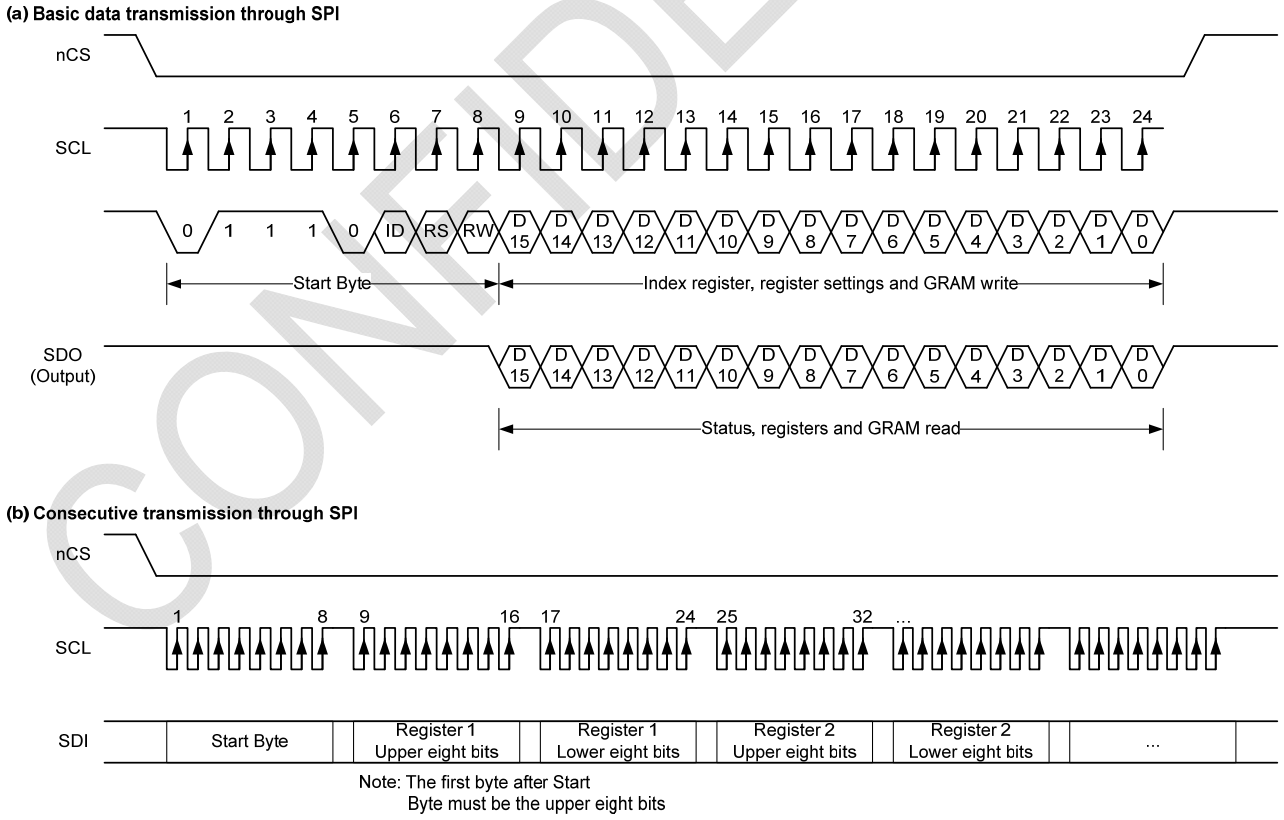
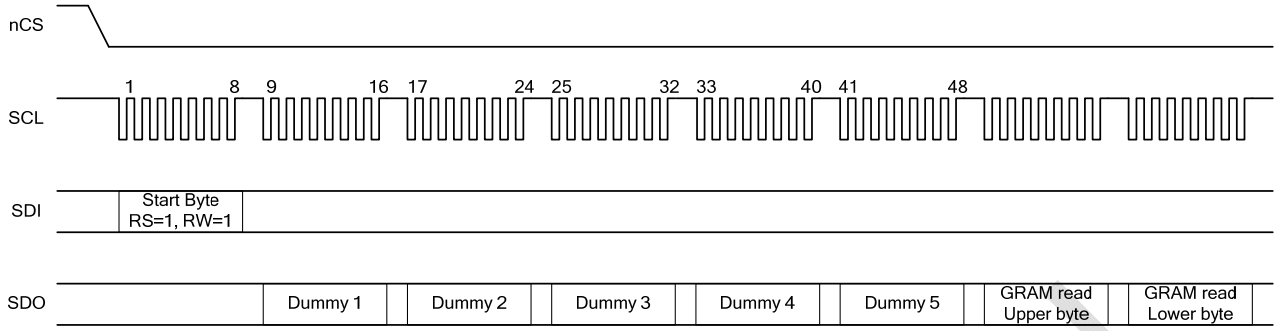


Figure 17 Serial Interface Data Format

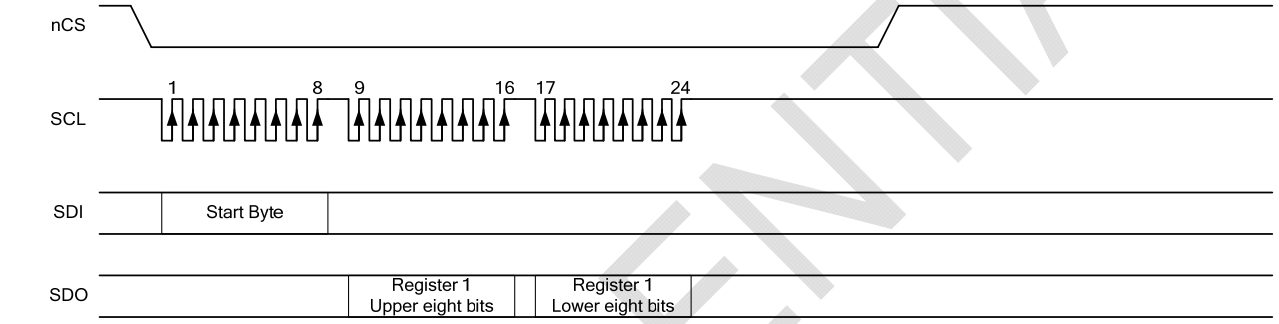


(c) GRAM data read transmission (TRI="0")



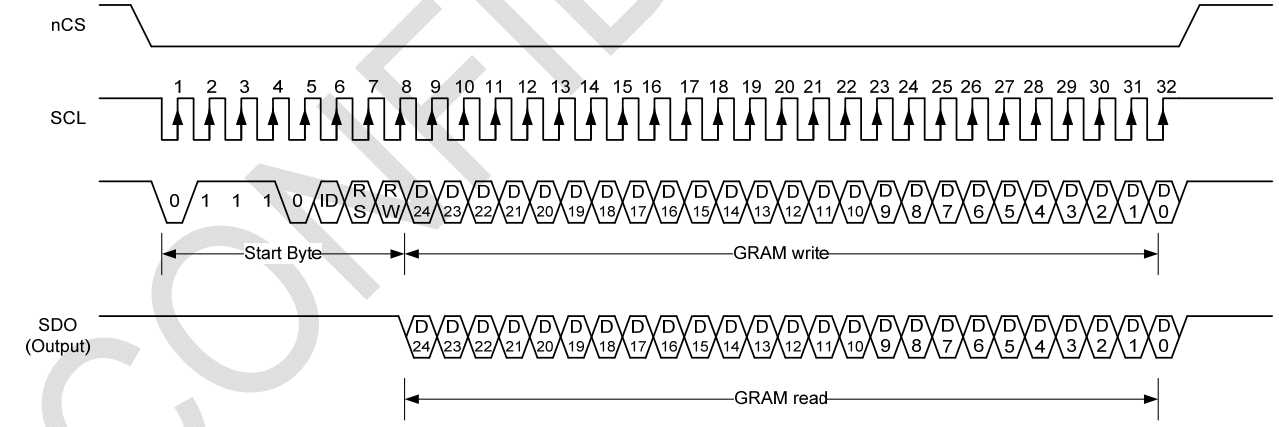
Note: Five bytes of dummy data are right after the Start Byte

(d) Status/register read transmission

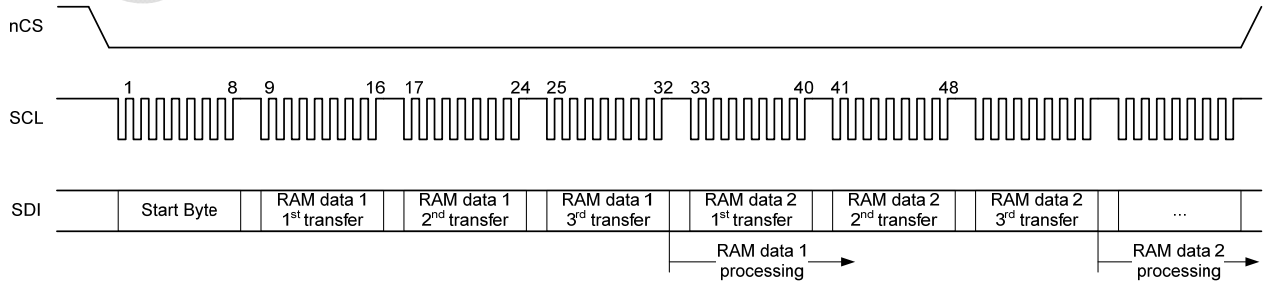


Note: Valid RAM data is read out right after the Start Byte

(e) Basic RAMdata transmission through SPI (TRI="1")



(f) GRAM data write transmission through SPI (TRI="1")



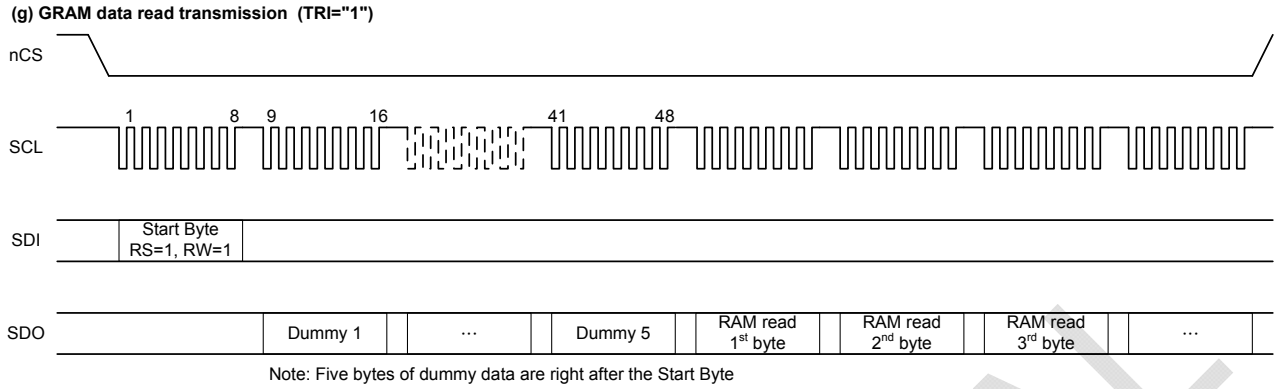


Figure 18 Data Transfer in Serial Interface

13. VSYNC Interface

RM68080 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNCX to display the moving picture with the system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.

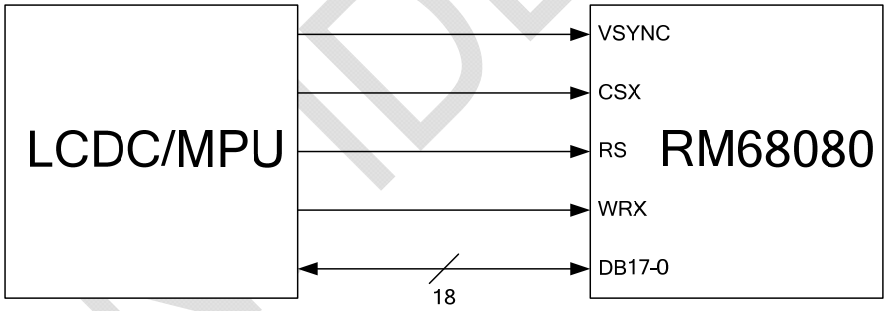


Figure 19 VSYNC Interface connection

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNCX input and the frame rate is determined by the pulse rate of VSYNCX signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

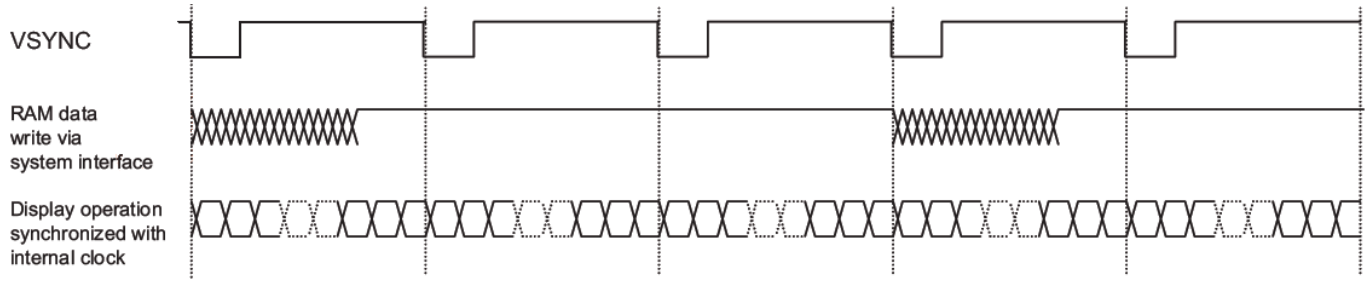


Figure 20 Moving Picture Data Transfers via VSYNC Interface

The VSYNCX interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$\text{Internal clock frequency (fosc)[Hz]} = \text{FrameRate} \times (\text{DisplayLines(NL)} + \text{FrontPorch(FP)} + \text{BackPorch(BP)}) \times \text{ClocksPerLine(RTN)} \times \text{variance}$$

$$\text{RAM Write Speed(min.)[Hz]} > \frac{240 \times \text{DisplayLines(NL)}}{(\text{FrintPorch(FP)} + \text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margins}) \times \text{ClocksPerLine(RTN)} \times \frac{1}{\text{fosc}}}$$

Note: When RAM write operation is not started right after the falling edge of VSYNCX, the time from the falling edge of VSYNCX until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Panel Size	240 RGB x 432 lines (NL = 6'h35: 432 lines)
Total number of lines (NL)	432 lines
Black/front porch	13/3 lines (BP = 8'h0D, FP = 8'h03)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz]

= 60 Hz x (432 + 3 + 13) lines x 23 clocks x 1.1 / 0.9 = 756 kHz

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz]

> 240 x 432 / {((13 + 3 + 432 -2) lines x 23 clocks) x 1/756 kHz} = 7.64 MHz

The above theoretical value is calculated based on the premise that the RM68080 starts to write data into

the internal GRAM on the falling edge of VSYNCX. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 7.71MHz or more will guarantee the completion of GRAM write operation before the RM68080 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes:

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNCX signal and the period of VSYNCX must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNCX cycle, i.e. after completing the display of the frame.
4. The partial display and vertical scroll functions are not available in VSYNC interface mode and set the AM bit to “0” to transfer display data.

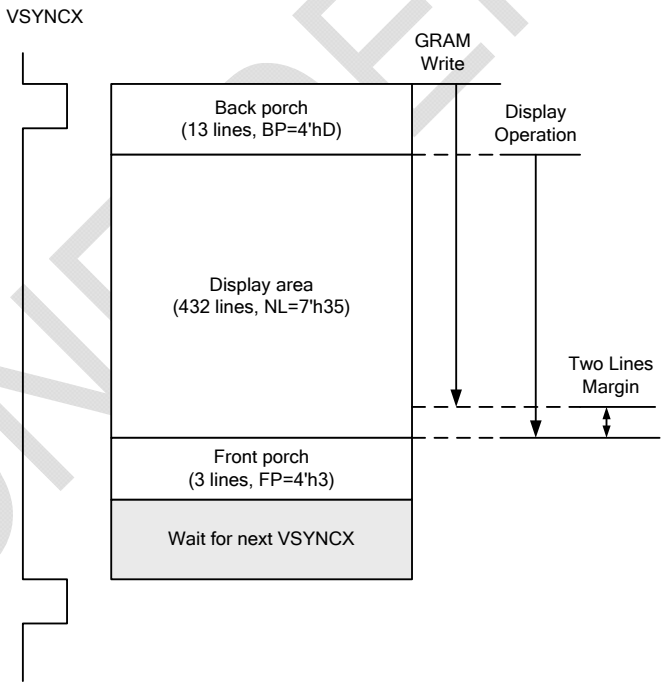


Figure 21 RAM Write Speed Margins

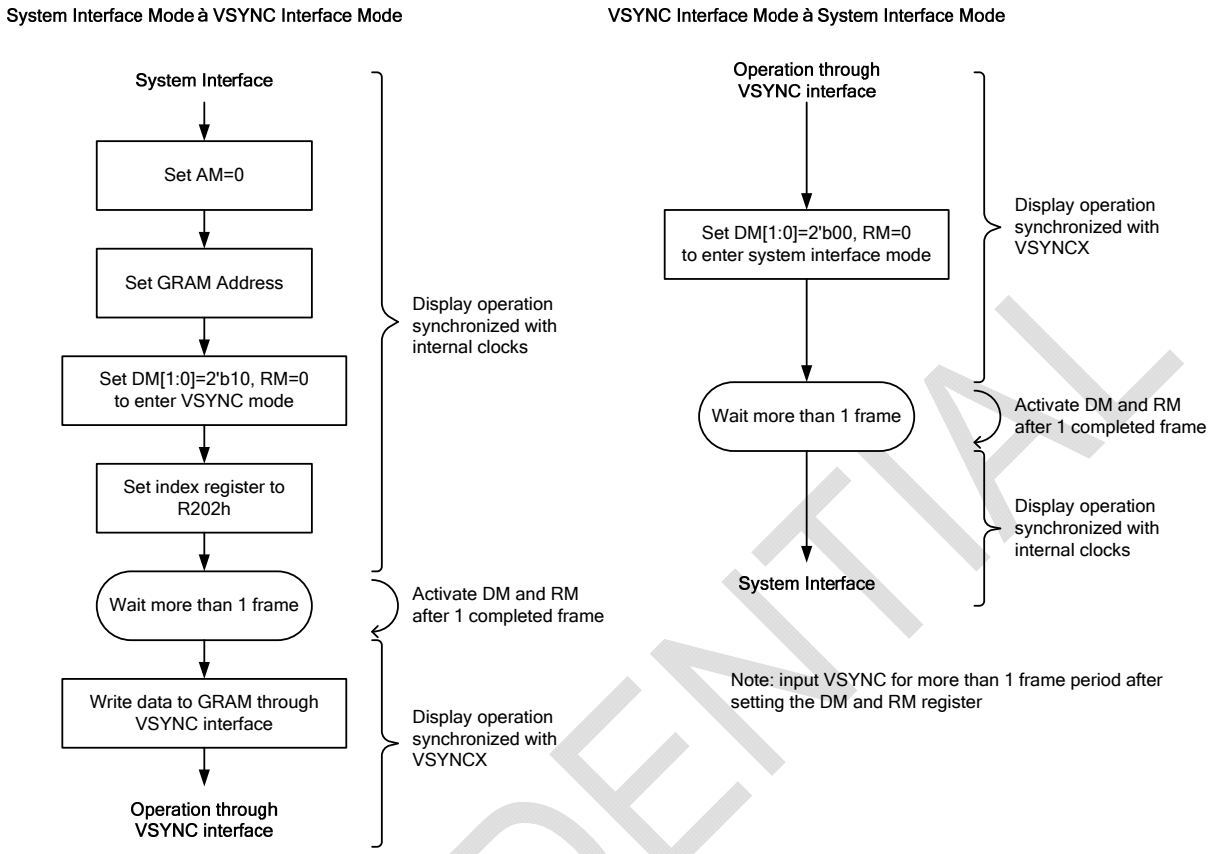


Figure 22 Sequences to Switch between VSYNC and Internal Clock Operation Modes

14. RGB Interface

The RM68080 supports the RGB interface. The interface format is set by RIM[1:0] bits. The internal RAM is accessible via RGB interface.

Table 15 RGB interface

RIM	RGB Interface	DB Pin
0	18-bit RGB interface	DB17-0
1	16-bit RGB interface	DB17-13, DB11-1

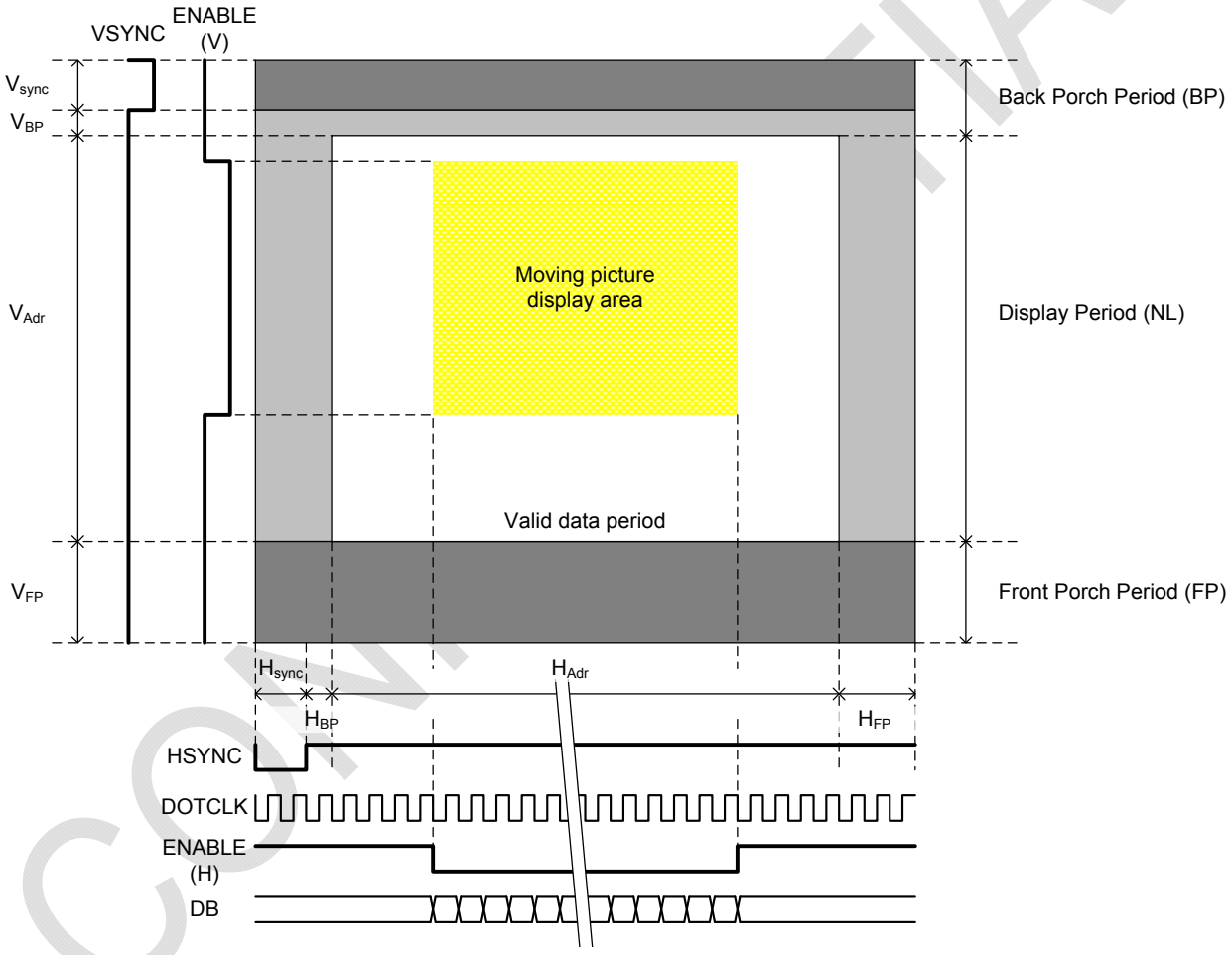


Figure 23 Display Operation via RGB Interface

Signal	Symbol	Parameter	MIN	TYP	MAX	Step	Unit
VSYNC	V_{sync}	Vertical Synchronization	1	2	4	1	Line
	V_{BP}	Vertical Back Porch	1	2	-	1	Line
	V_{Adr}	Vertical Address	-	432	-	1	Line
	V_{FP}	Vertical Front Porch	3	4	-	1	Line
HSYNC	H_{sync}	Horizontal Synchronization	2	10	16	1	DOTCLKCYC
	H_{BP}	Horizontal Back Porch	2	20	24	1	DOTCLKCYC

	H_{Adr}	Horizontal Address	-	240	-	1	DOTCLKCYC
	H_{FP}	Horizontal Front Porch	2	10	16	1	DOTCLKCYC

Note:

1. The front porch period continues until net VSYNCX input is detected.
2. Make sure to match the VSYNCX, HSYNCX, and DOTCLK frequencies to the resolution of liquid crystal panel

14.1 RGB Interface Timing

The timing relationship of signals in RGB interface operation is as follows.

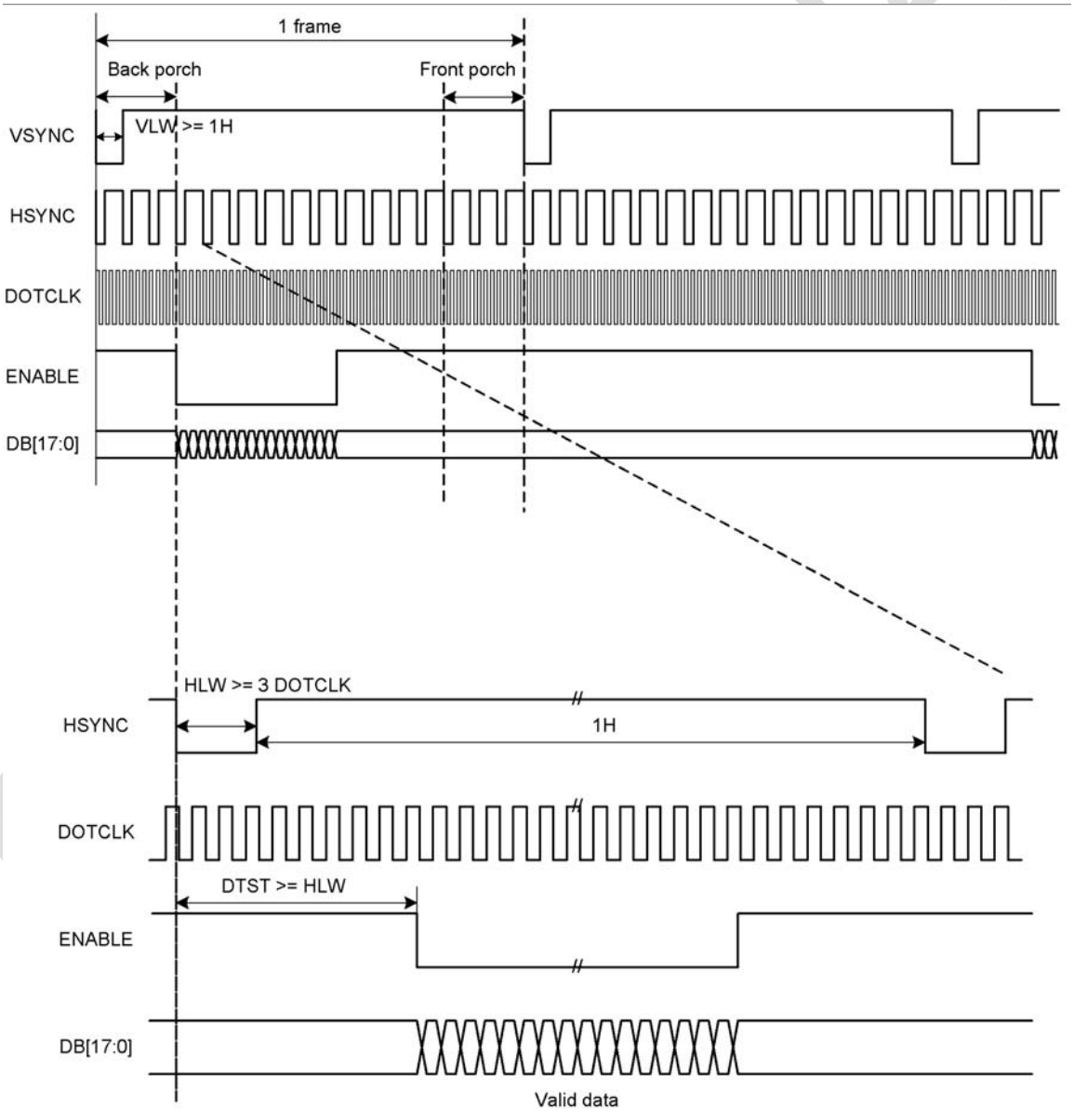


Figure 24 16-/18-bit RGB Interface Timing

Notes:

1. VLW: VSYNCX Low period,
2. HLW: HSYNCX Low period,
3. DTST: data transfer setup time

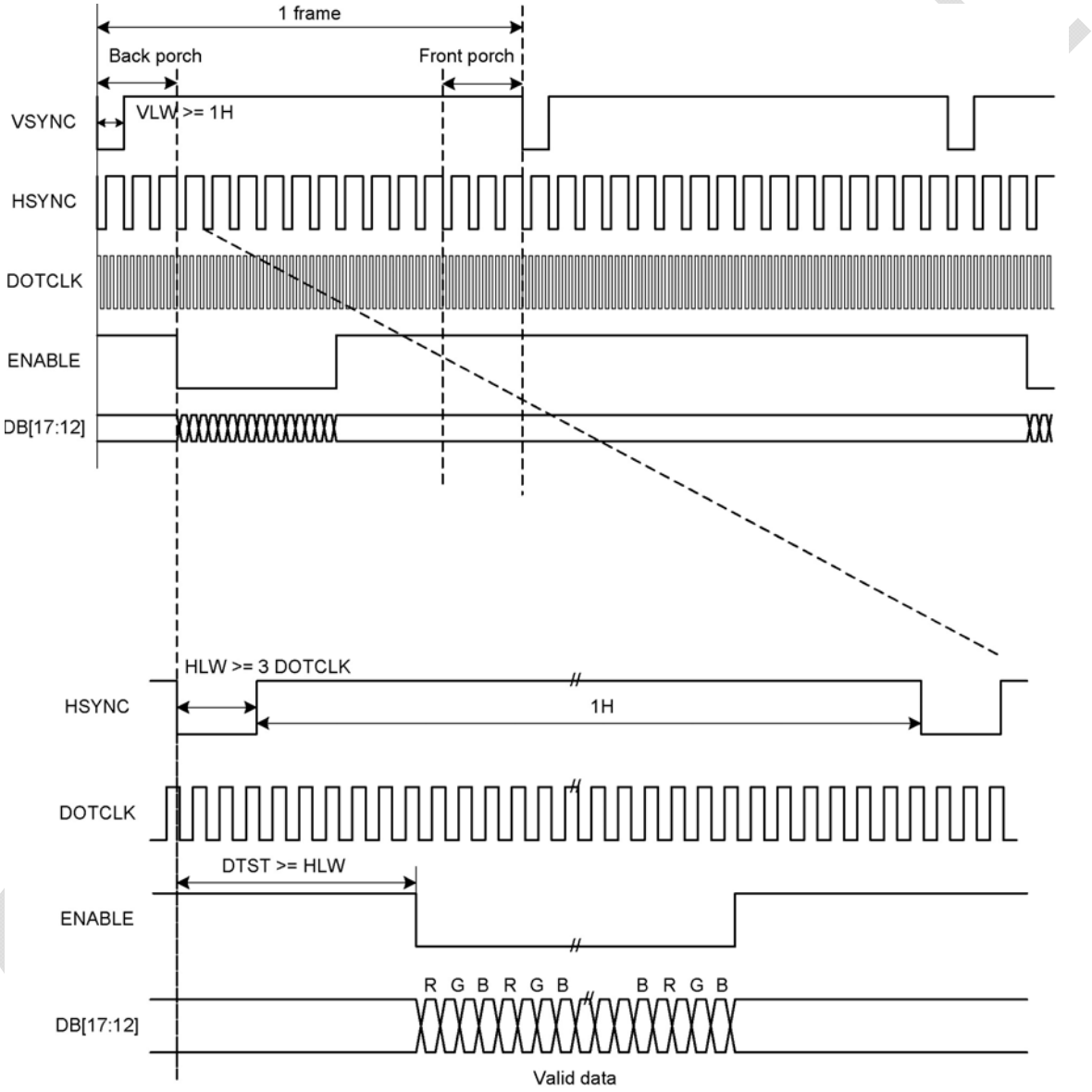


Figure 25 6-bit RGB Interface Timing

Notes:

1. VLW: VSYNC Low period,
2. HLW: HSYNC Low period,

3. DTST: data transfer setup time

14.2 Moving Pictures Mode

RM68080 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following advantages in displaying a moving picture.

• The window address function defined the update area of GRAM.

• Only the moving picture area of GRAM is updated.

• When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

14.3 RAM access via system interface in RGB interface operation

RM68080 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = “0”) and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = “1” and the index register to R202h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the RM68080 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

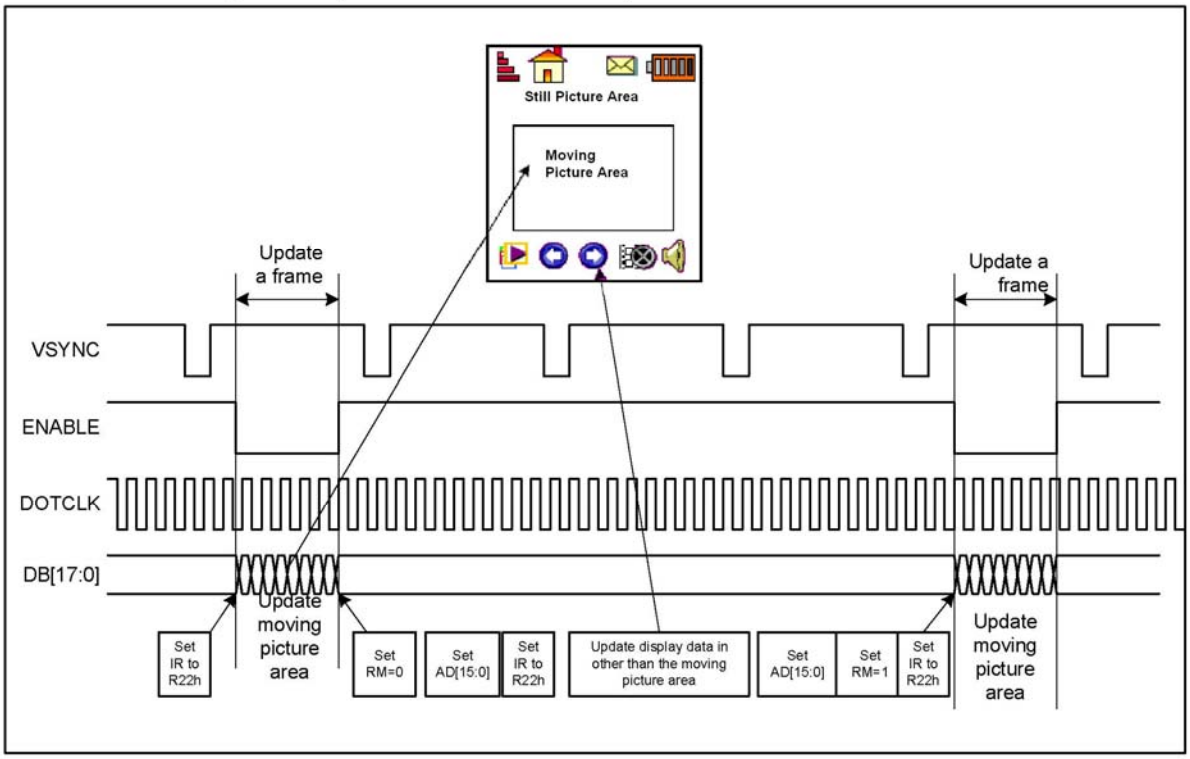


Figure 26 Updating the Still Picture Area while Displaying Moving Picture

14.4 16-bit RGB interface

The 16-bit RGB interface is selected by setting RIM = 1. The display operation is synchronized with VSYNCX, HSYNCX, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit ports while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

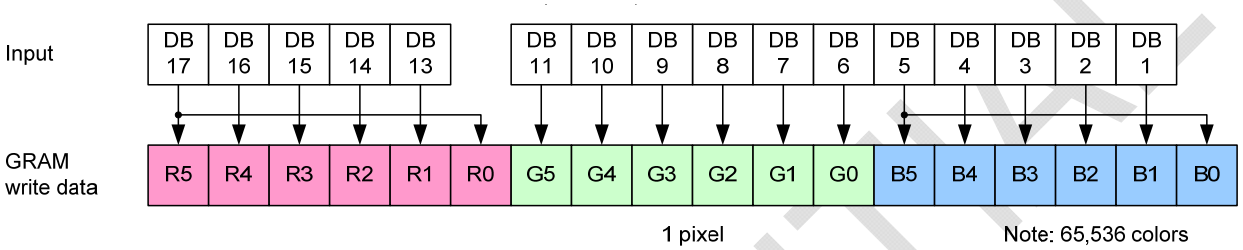


Figure 27 Example of 16-bit RGB Interface and Data Format

14.5 18-bit RGB interface

The 18-bit RGB interface is selected by setting RIM= 0. The display operation is synchronized with VSYNCX, HSYNCX, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit ports (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

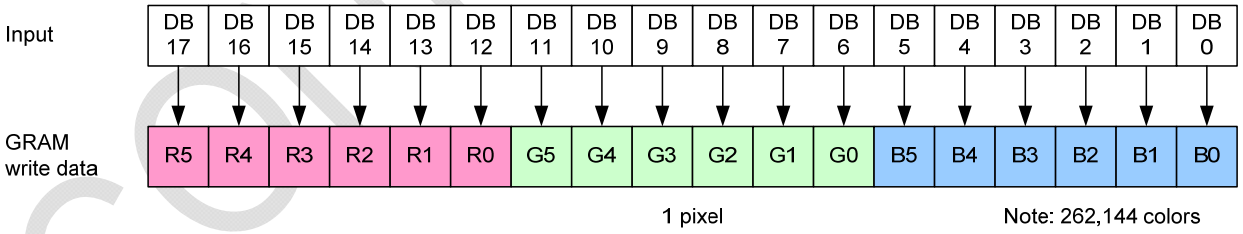


Figure 28 Example of 18-bit RGB Interface and Data Format

14.6 Notes to external display interface operation

1. The following functions are not available in external display interface operation.

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNCX, HSYNCX, and DOTCLK signals must be supplied during display period.
3. The period set with the NOWE[1:0] bits (gate output non-overlap period) is not based on the internal clock but based on DOTCLK in RGB interface mode.
4. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
5. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
6. In RGB interface mode, a RAM address (AD[16:0]) is set in the address counter every frame on the falling edge of VSYNC.

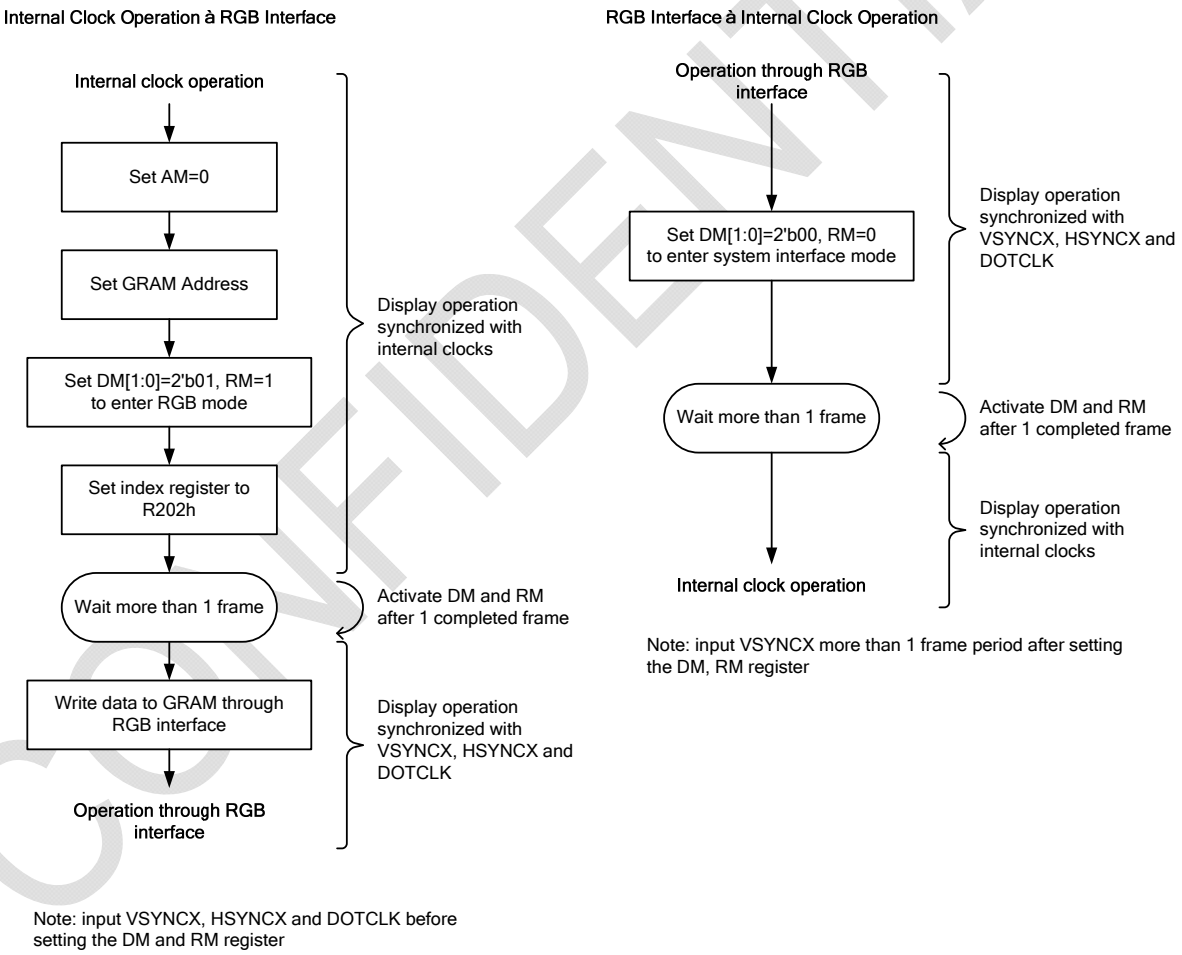


Figure 29 RGB and Internal Clock Operation Mode Switching Sequences

15. Partial Display Function

The RM68080 allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

Partial image 1 display instruction		**Other instruction**	
PTDE	1	BASEE	0
PTSA[8:0]	9'h090	NL[5:0]	6'h35
PTEA[8:0]	9'h09F		
PTDP[8:0]	9'h080		

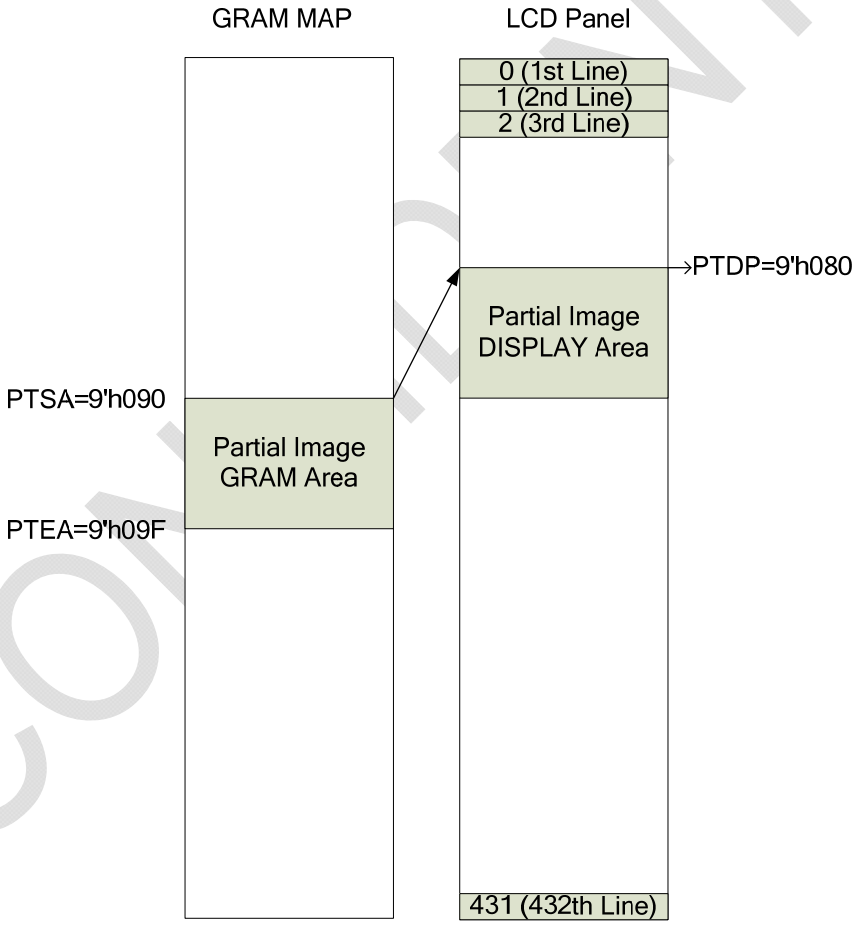


Figure 30 Partial Display example

16. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (increment or decrement, horizontal or vertical, respectively). Setting these bits enables the RM68080 to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

	Window address area setting range	**RAM address area setting range**
Horizontal direction	8'h00 ≤ HSA ≤ HEA ≤ 8'hEF	HSA ≤ AD[7:0] ≤ HEA
Vertical direction	9'h000 ≤ VSA ≤ VEA ≤ 9'h1AF	VSA ≤ AD[16:8] ≤ VEA

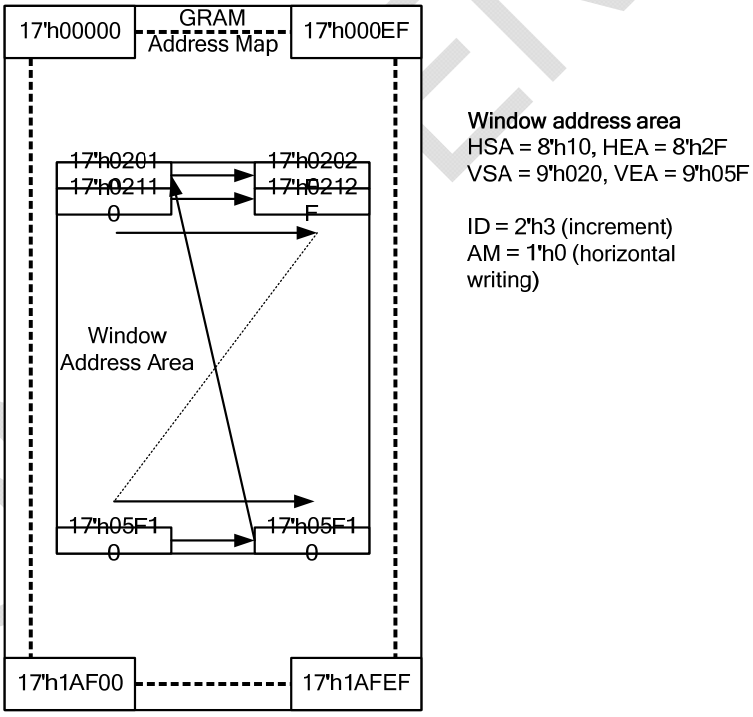


Figure 31 Automatic address update within a Window Address Area

17. γ Correction Function

The RM68080 supports γ-correction function to make the optimal colors according to the characteristics of the panel. The RM68080 has registers for positive and negative polarities.

17.1 γ Correction Circuit

The following figure shows the γ-correction circuit. According to the settings of variable resistors PR0P00/PR0N00 to PR0P08/PR0N08, the voltage level, the difference between VREG1OUT and VGS, is divided into 8 grayscale reference voltages (V0, V1, V8, V20, V43, V55, V62, and V63). Other 56-grayscale voltages are generated by setting the level at a certain interval between the reference voltages. For grayscale voltage, see “Grayscale Voltage Calculation Formula”.

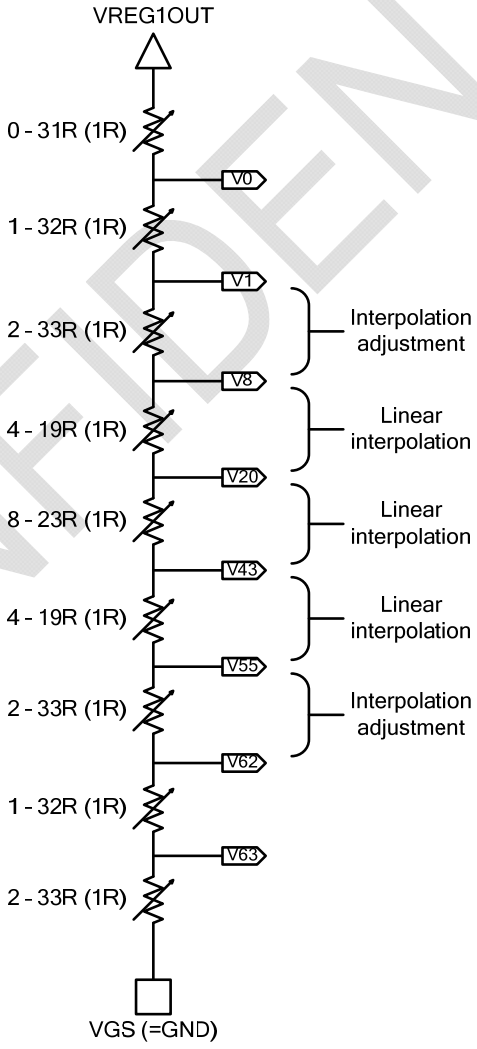


Figure 32 Structure of gamma correction function

17.2 γ Correction Registers

17.2.1 Reference level adjustment registers

Resistor	Register		Resistance	Resistor	Register		Resistance
	Name	Value			Name	Value	
R0	PR0P00[4:0] PR0N00[4:0]	5'h00 5'h01 5'h02 … 5'h1F	0R 1R 2R … 31R	R5	PR0P05[3:0] PR0N05[3:0]	4'h0 4'h1 4'h2 … 4'hF	4R 5R 6R … 19R
R1	PR0P01[4:0] PR0N01[4:0]	5'h00 5'h01 5'h02 … 5'h1F	1R 2R 3R … 32R	R6	PR0P06[4:0] PR0N06[4:0]	5'h00 5'h01 5'h02 … 5'h1F	2R 3R 4R … 33R
R2	PR0P02[4:0] PR0N02[4:0]	5'h00 5'h01 5'h02 … 5'h1F	2R 3R 4R … 33R	R7	PR0P07[4:0] PR0N07[4:0]	5'h00 5'h01 5'h02 … 5'h1F	1R 2R 3R … 32R
R3	PR0P03[3:0] PR0N03[3:0]	4'h0 4'h1 4'h2 … 4'hF	4R 5R 6R … 19R	R8	PR0P08[4:0] PR0N08[4:0]	5'h00 5'h01 5'h02 … 5'h1F	2R 3R 4R … 33R
R4	PR0P04[3:0] PR0N04[3:0]	4'h0 4'h1 4'h2 … 4'hF	8R 9R 10R … 23R				

17.2.2 Interpolation Registers

Interpolation factor for V2 to V7 (See "Grayscale Voltage Calculation Formula" for IPVm level)

PI0P0[1:0] PI0N0[1:0]	PI0P1[1:0] PI0N1[1:0]	IPV2	IPV3	IPV4	IPV5	IPV6	IPV7
2'h0	2'h0	81%	67%	52%	39%	26%	13%
	2'h1	78%	61%	43%	33%	22%	11%
	2'h2	73%	52%	31%	23%	15%	8%
	2'h3	72%	50%	28%	21%	14%	7%
2'h1	2'h0	80%	68%	56%	42%	28%	14%
	2'h1	76%	62%	48%	36%	24%	12%
	2'h2	70%	52%	35%	26%	17%	9%
	2'h3	69%	50%	31%	23%	16%	8%
2'h2	2'h0	78%	70%	61%	46%	30%	15%
	2'h1	74%	63%	53%	39%	26%	13%
	2'h2	66%	53%	39%	29%	20%	10%
	2'h3	64%	50%	36%	27%	18%	9%
2'h3	2'h0	78%	70%	63%	47%	31%	16%
	2'h1	73%	64%	54%	41%	27%	14%

2'h2	65%	53%	41%	31%	20%	10%
2'h3	63%	50%	37%	28%	19%	9%

Interpolation factor for V56 to V61

PI0P3[1:0] PI0N3[1:0]	PI0P2[1:0] PI0N2[1:0]	IPV56	IPV57	IPV58	IPV59	IPV60	IPV61
2'h0	2'h0	87%	74%	61%	48%	33%	19%
	2'h1	89%	78%	67%	57%	39%	22%
	2'h2	92%	85%	77%	69%	48%	27%
	2'h3	93%	86%	79%	72%	50%	28%
2'h1	2'h0	86%	82%	58%	44%	32%	20%
	2'h1	88%	76%	64%	52%	38%	24%
	2'h2	91%	83%	74%	65%	48%	30%
	2'h3	92%	84%	77%	69%	50%	31%
2'h2	2'h0	85%	70%	54%	39%	30%	22%
	2'h1	87%	74%	61%	47%	37%	26%
	2'h2	90%	80%	71%	61%	47%	34%
	2'h3	91%	82%	73%	64%	50%	36%
2'h3	2'h0	84%	69%	53%	38%	30%	22%
	2'h1	86%	73%	59%	46%	36%	27%
	2'h2	90%	80%	69%	59%	47%	35%
	2'h3	91%	81%	72%	63%	50%	37%

17.2.3 Grayscale Voltage Calculation Formula

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	ΔV x ∑(R1 ~ R8)/SUMR	V32	V43 + (V20 - V43) x 11/23
V1	ΔV x ∑(R2 ~ R8)/SUMR	V33	V43 + (V20 - V43) x 10/23
V2	V8 + (V1 - V8) x IPV2	V34	V43 + (V20 - V43) x 9/23
V3	V8 + (V1 - V8) x IPV3	V35	V43 + (V20 - V43) x 8/23
V4	V8 + (V1 - V8) x IPV4	V36	V43 + (V20 - V43) x 7/23
V5	V8 + (V1 - V8) x IPV5	V37	V43 + (V20 - V43) x 6/23
V6	V8 + (V1 - V8) x IPV6	V38	V43 + (V20 - V43) x 5/23
V7	V8 + (V1 - V8) x IPV7	V39	V43 + (V20 - V43) x 4/23
V8	ΔV x ∑(R3 ~ R8)/SUMR	V40	V43 + (V20 - V43) x 3/23
V9	V20 + (V8 - V20) x 11/12	V41	V43 + (V20 - V43) x 2/23
V10	V20 + (V8 - V20) x 10/12	V42	V43 + (V20 - V43) x 1/23
V11	V20 + (V8 - V20) x 9/12	V43	ΔV x ∑(R5 ~ R8)/SUMR
V12	V20 + (V8 - V20) x 8/12	V44	V55 + (V43 - V55) x 11/12
V13	V20 + (V8 - V20) x 7/12	V45	V55 + (V43 - V55) x 10/12
V14	V20 + (V8 - V20) x 6/12	V46	V55 + (V43 - V55) x 9/12
V15	V20 + (V8 - V20) x 5/12	V47	V55 + (V43 - V55) x 8/12
V16	V20 + (V8 - V20) x 4/12	V48	V55 + (V43 - V55) x 7/12
V17	V20 + (V8 - V20) x 3/12	V49	V55 + (V43 - V55) x 6/12
V18	V20 + (V8 - V20) x 2/12	V50	V55 + (V43 - V55) x 5/12
V19	V20 + (V8 - V20) x 1/12	V51	V55 + (V43 - V55) x 4/12
V20	ΔV x ∑(R4 ~ R8)/SUMR	V52	V55 + (V43 - V55) x 3/12
V21	V43 + (V20 - V43) x 22/23	V53	V55 + (V43 - V55) x 2/12
V22	V43 + (V20 - V43) x 21/23	V54	V55 + (V43 - V55) x 1/12
V23	V43 + (V20 - V43) x 20/23	V55	ΔV x ∑(R6 ~ R8)/SUMR
V24	V43 + (V20 - V43) x 19/23	V56	V62 + (V55 - V62) x IPV56
V25	V43 + (V20 - V43) x 18/23	V57	V62 + (V55 - V62) x IPV57
V26	V43 + (V20 - V43) x 17/23	V58	V62 + (V55 - V62) x IPV58
V27	V43 + (V20 - V43) x 16/23	V59	V62 + (V55 - V62) x IPV59

V28	V43 + (V20 - V43) x 15/23	V60	V62 + (V55 - V62) x IPV60
V29	V43 + (V20 - V43) x 14/23	V61	V62 + (V55 - V62) x IPV61
V30	V43 + (V20 - V43) x 13/23	V62	ΔV x ∑(R7 ~ R8)/SUMR
V31	V43 + (V20 - V43) x 12/23	V63	ΔV x R8/SUMR

Note:

1. ΔV = VREG1OUT - VGS
2. SUMR = ∑(R1 ~ R8) ≥ 70R
3. V63 ≥ 0.2V

17.2.4 Frame Memory Data and the Grayscale Volta

Frame memory data	Grayscale Voltage				Frame memory data	Grayscale Voltage			
	REV = 1		REV = 0			REV = 1		REV = 0	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity		Positive polarity	Negative polarity	Positive polarity	Negative polarity
6'h00	V0	V63	V63	V0	6'h20	V32	V31	V31	V32
6'h01	V1	V62	V62	V1	6'h21	V33	V30	V30	V33
6'h02	V2	V61	V61	V2	6'h22	V34	V29	V29	V34
6'h03	V3	V60	V60	V3	6'h23	V35	V28	V28	V35
6'h04	V4	V59	V59	V4	6'h24	V36	V27	V27	V36
6'h05	V5	V58	V58	V5	6'h25	V37	V26	V26	V37
6'h06	V6	V57	V57	V6	6'h26	V38	V25	V25	V38
6'h07	V7	V56	V56	V7	6'h27	V39	V24	V24	V39
6'h08	V8	V55	V55	V8	6'h28	V40	V23	V23	V40
6'h09	V9	V54	V54	V9	6'h29	V41	V22	V22	V41
6'h0A	V10	V53	V53	V10	6'h2A	V42	V21	V21	V42
6'h0B	V11	V52	V52	V11	6'h2B	V43	V20	V20	V43
6'h0C	V12	V51	V51	V12	6'h2C	V44	V19	V19	V44
6'h0D	V13	V50	V50	V13	6'h2D	V45	V18	V18	V45
6'h0E	V14	V49	V49	V14	6'h2E	V46	V17	V17	V46
6'h0F	V15	V48	V48	V15	6'h2F	V47	V16	V16	V47
6'h10	V16	V47	V47	V16	6'h30	V48	V15	V15	V48
6'h11	V17	V46	V46	V17	6'h31	V49	V14	V14	V49
6'h12	V18	V45	V45	V18	6'h32	V50	V13	V13	V50
6'h13	V19	V44	V44	V19	6'h33	V51	V12	V12	V51
6'h14	V20	V43	V43	V20	6'h34	V52	V11	V11	V52
6'h15	V21	V42	V42	V21	6'h35	V53	V10	V10	V53
6'h16	V22	V41	V41	V22	6'h36	V54	V9	V9	V54
6'h17	V23	V40	V40	V23	6'h37	V55	V8	V8	V55
6'h18	V24	V39	V39	V24	6'h38	V56	V7	V7	V56
6'h19	V25	V38	V38	V25	6'h39	V57	V6	V6	V57
6'h1A	V26	V37	V37	V26	6'h3A	V58	V5	V5	V58
6'h1B	V27	V36	V36	V27	6'h3B	V59	V4	V4	V59
6'h1C	V28	V35	V35	V28	6'h3C	V60	V3	V3	V60
6'h1D	V29	V34	V34	V29	6'h3D	V61	V2	V2	V61
6'h1E	V30	V33	V33	V30	6'h3E	V62	V1	V1	V62
6'h1F	V31	V32	V32	V31	6'h3F	V63	V0	V0	V63

18. Power-Supply Generating Circuit

18.1 Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the RM68080 and the TFT display application voltage waveforms and electrical potential relationship.

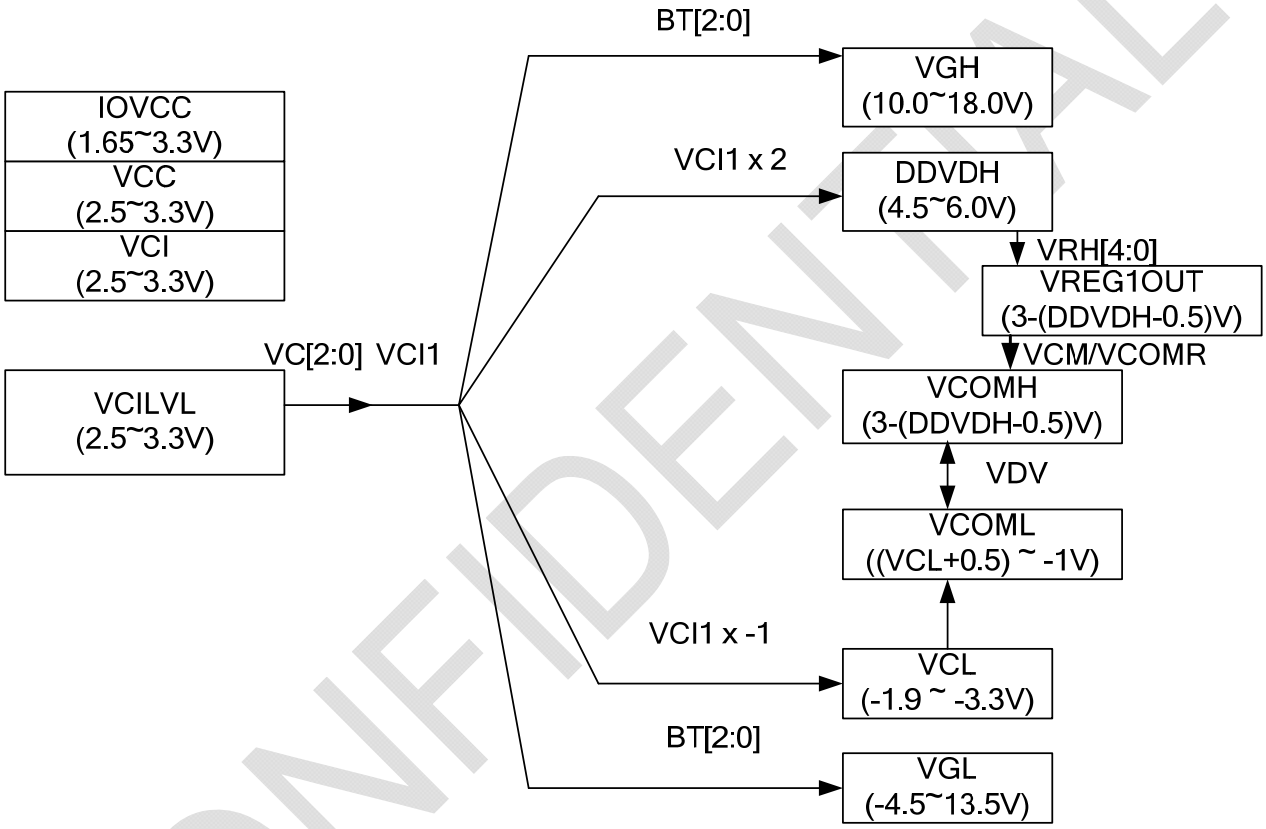


Figure 33 Diagram of voltage generation

Notes:

1. The DDVDH, VGH, VGL, and VCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at each output level. Make sure that output voltage level in operation maintains the following relationship: (DDVDH – VREG1OUT) ≥ 0.5V, (VCOML – VCL) > 0.5V. Also make sure VGH-VGL ≤ 28V, VCI-VCL ≤ 6V. When the alternating cycle of VCOM is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

2. In operation, setting voltages within the respective voltage ranges are recommended.

18.2 Liquid crystal application voltage waveform and electrical potential

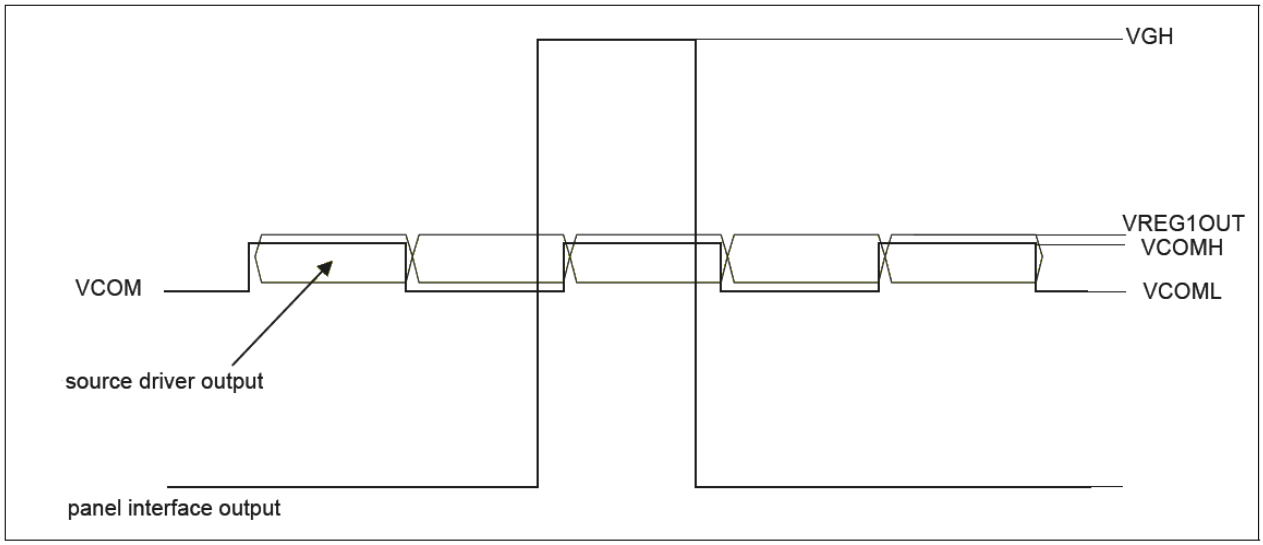


Figure 34 Voltage output to TFT LCD Panel

19. OTP control sequence

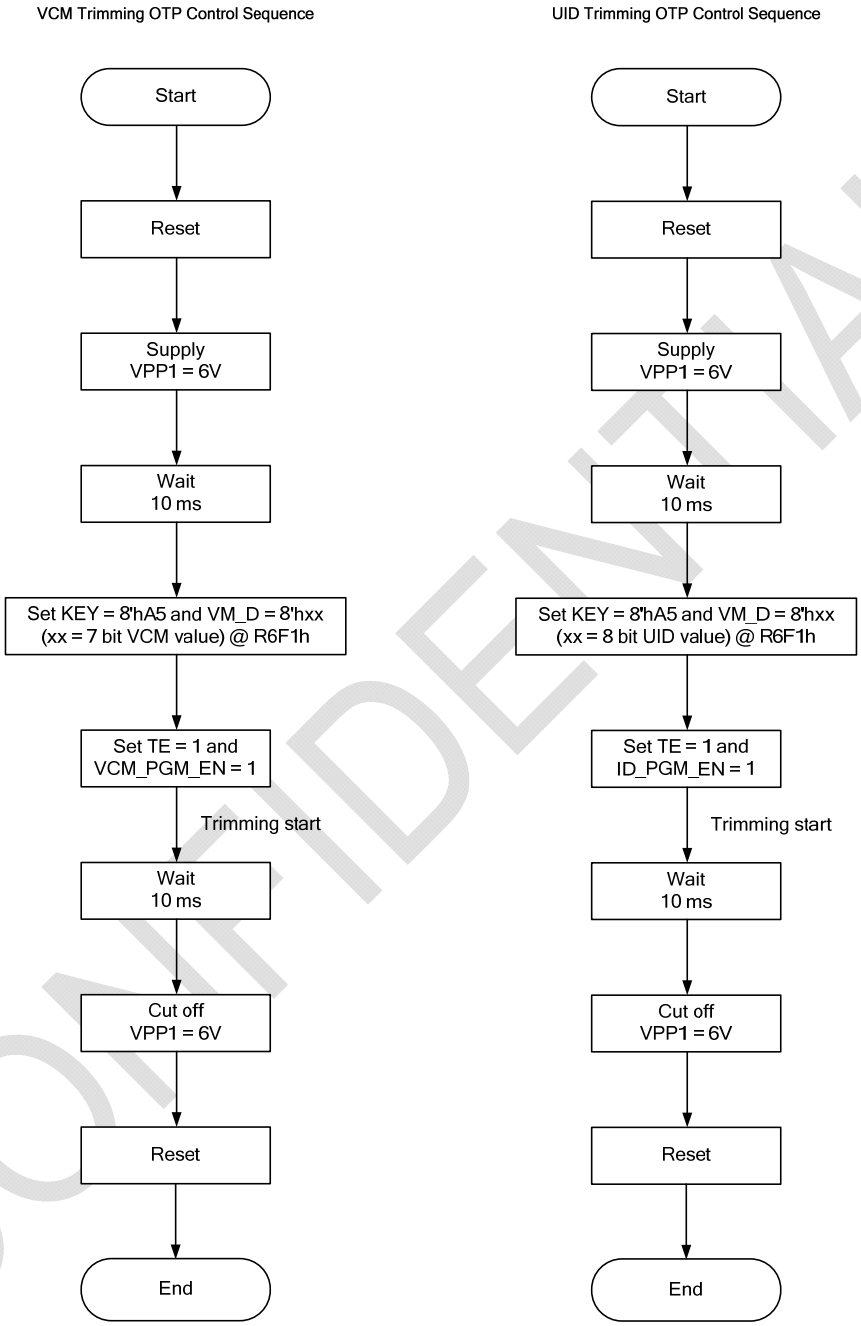


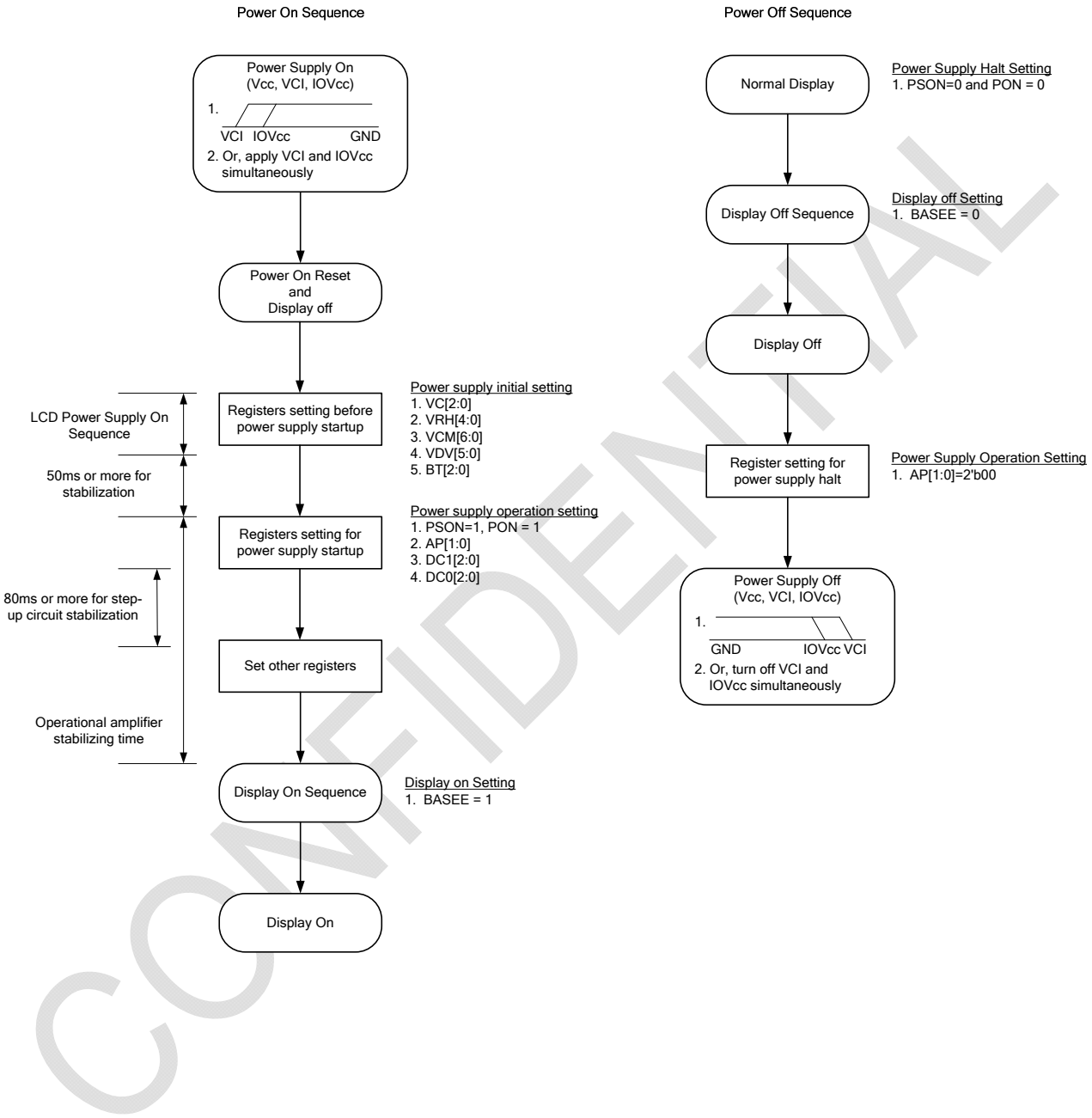
Figure 35 OTP control sequence diagram

20. Power Supply Instruction Setting

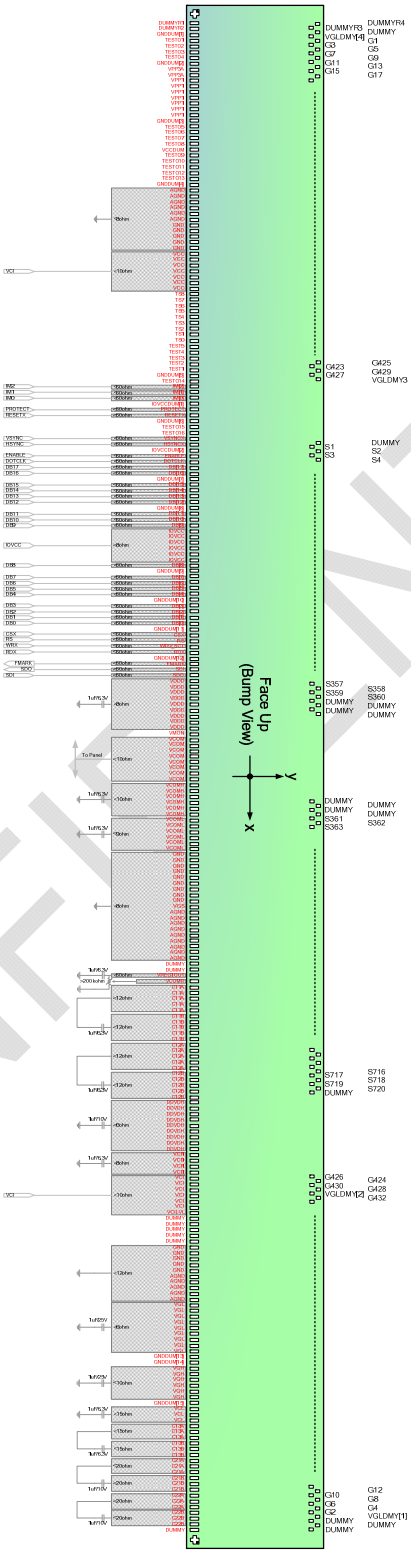
The following are the sequences for setting power supply ON/OFF instructions. Set power supply ON/OFF

instructions according to the following sequences in Display ON/OFF, Sleep set/exit sequences.

20.1 Power Supply Instruction Setting



21. Application Circuit



22. Absolute Maximum Ratings

Table 16

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VCI, IOVCC	V	-0.3 ~ +4.6	1, 2
Power Supply Voltage 2	VCI – GND	V	-0.3 ~ +4.6	1, 4
Power Supply Voltage 3	DDVDH –GND	V	-0.3 ~ +6.0	1, 4
Power Supply Voltage 4	AGND – VCL	V	-0.3 ~ +4.6	1
Power Supply Voltage 5	DDVDH – VCL	V	-0.3 ~ +9.0	1, 5
Power Supply Voltage 6	VGH – VGL	V	-0.3 ~ +30.0	1, 5
Input Voltage	Vt	V	-0.3 ~ IOVCC + 0.3	1
Operating Temperature	Topr	℃	-40 ~ +85	8, 9
Storage Temperature	Tstg	℃	-55 ~ +110	8, 9

Notes:

1. GND must be maintained.
2. Make sure VCI(high)≥DGND(low), IOVCC(high)≥DGND(low).
3. Make sure VCI(high)≥DGND(low).
4. Make sure DDVDH(high)≥AGND(low)
5. Make sure DDVDH(high) ≥VCL(low).
6. Make sure VGH(high) ≥GND(low)
7. Make sure AGND(high)≥VGL(low).
8. For die and wafer products, specified up to 85℃.
9. This temperature specifications apply to the TCP package.

23. Electrical Characteristics

23.1 DC Electrical Characteristics

(VCI = 2.5V ~ 3.3V, IOVCC = 1.65V ~ 3.30V, Ta= -40℃~+85℃)

Item	Symbol	Unit	Test Condition	Min.	Typ	Max.
Input “High” level voltage	V_{IH}	V	IOVCC = 1.65V~3.30V	0.85 x IOVCC	-	IOVCC
Input “Low” level voltage	V_{IL}	V	IOVCC = 1.65V~3.30V	-0.3	-	0.15 x IOVCC
Output “High” level voltage 1 (DB0-17, FMARK)	V_{OH}	V	IOVCC = 1.65V~3.30V IOH = -0.1mA	0.80 x IOVCC	-	-
Output “Low” level voltage 1 (DB0-17, FMARK)	V_{OL}	V	IOVCC = 1.65V~3.30V IOL = 0.1mA	-	-	0.2 x IOVCC
Input/Output leak current	I_{LI}	uA	Vin = 0~IOVCC	-0.1	-	0.1
Current Consumption (IOVCC-GND)+(VCI-GND) Normal operation mode (262k-colors, display operation)	I_{OP1}	uA	fosc=678kHz (432line drive), IOVCC=VCI=2.80V, Ta=25℃, RAM data: 18’h000000	--	TBD	--
Current Consumption (IOVCC-GND)+(VCI-GND) Deep standby mode	I_{DST}	uA	IOVCC=VCI=2.80V, Ta=25℃	-	0.1	1.0
LCD Power Supply Current (DDVDH-GND) 262k-color display operation	ILCD	mA	IOVCC=VCI=2.80V, ddvdh=5.20V, VREG1OUT=4.8V, Frame Rate=70Hz, Ta=25, RAM data: 18’h000000, line-inversion	-	5.5	--
LCD Driving Voltage	DDVDH	V	-	4.5	-	6.0
Output Voltage deviation	ΔV_O	mV	-	-	20	-
Maximum output voltage offset	ΔV_Δ	mV	-	-	35	-

23.2 AC Timing Characteristics

23.2.180-System Bus Interface

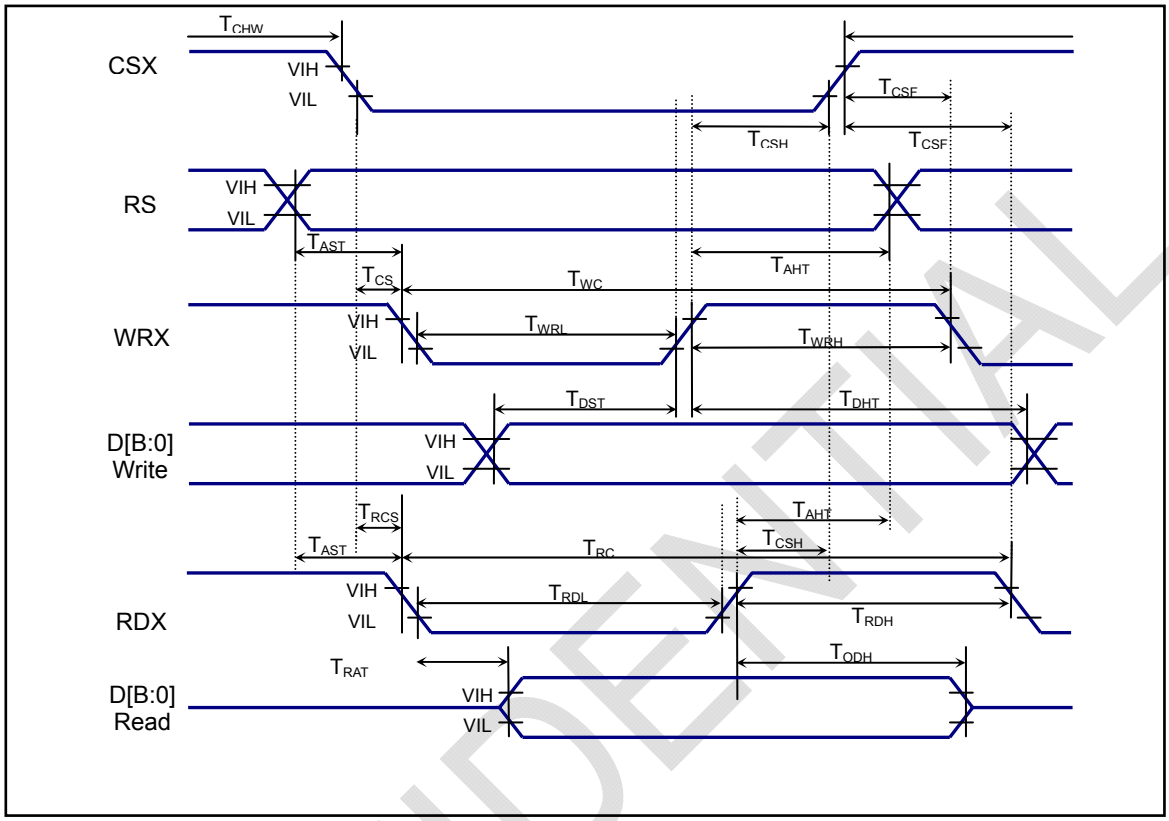


Figure 36 80-system Bus Interface

Normal Write Mode (IOVCC = 1.65~3.3V, VCI=2.5~3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
RS	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	2		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	10		ns	
	T_{RCS}	Chip select setup time (Read)	10		ns	
WRX	T_{CSH}	Chip select hold time	10		ns	
	T_{WC}	Write cycle	75		ns	
	T_{WRH}	Control pulse “H” duration	25		ns	-
	T_{WRL}	Control pulse “L” duration	40		ns	
RDX	T_{CSH}	Chip select hold time	10		ns	
	T_{RC}	Read cycle	450		ns	-
	T_{RDH}	Control pulse “H” duration	250		ns	
	T_{RDL}	Control pulse “L” duration	170		ns	
D[17:0]	T_{DST}	Data setup time	25		ns	-
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time		150	ns	
	T_{ODH}	Output disable time	5		ns	

23.2.2 Clock Synchronous Serial Interface

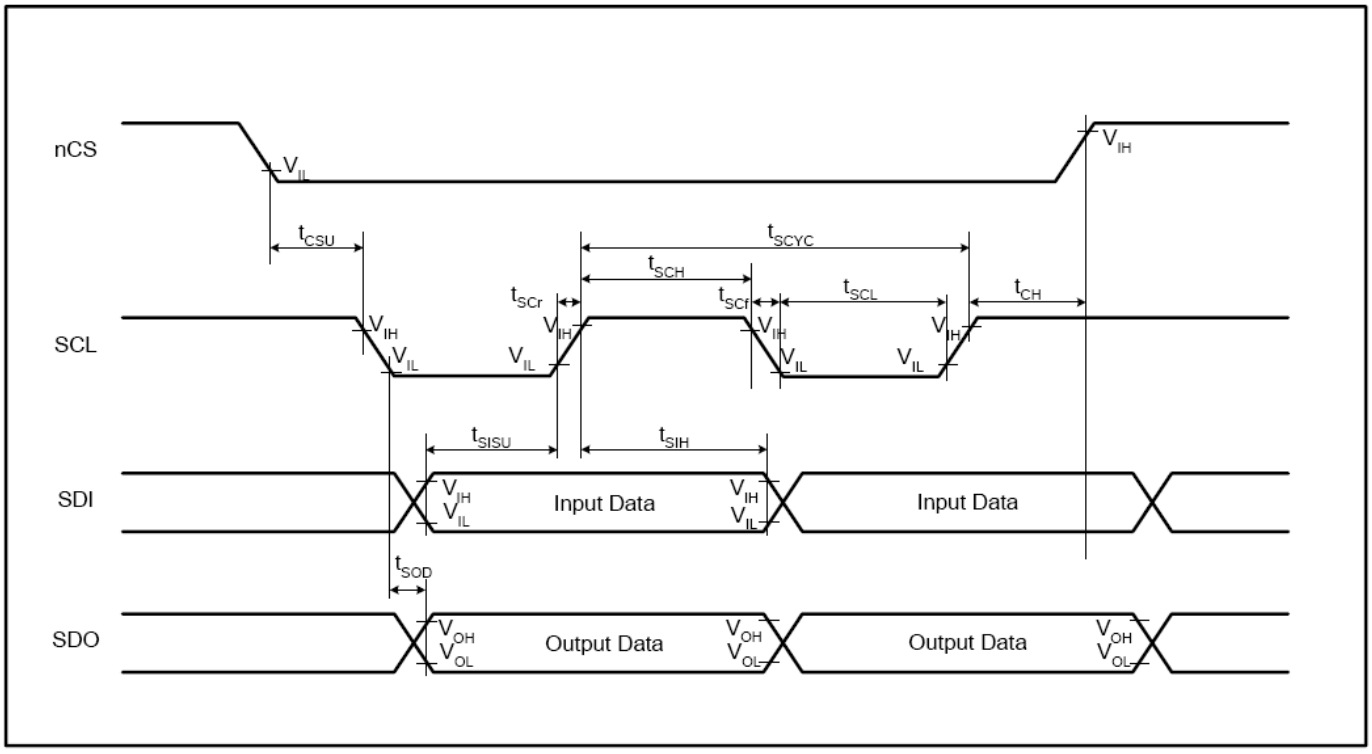


Figure 37 Clock Synchronous Serial Interface

IOVCC = 1.65~3.3V, VCI=2.5~3.3V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T_{SCYC}	Clock cycle (Write)	100		ns	-
	T_{SCYC}	Clock cycle (Read)	350		ns	
	T_{SCH}	Clock “H” pulse width (Write)	40		ns	
	T_{SCH}	Clock “H” pulse width (Read)	150		ns	
	T_{SCL}	Clock “L” pulse width (Write)	40		ns	
	T_{SCL}	Clock “L” pulse width (Read)	150		ns	
	T_{SCr}	Clock rise time		15	ns	
	T_{SCf}	Clock fall time		15	ns	
nCS(CSX)	T_{CSU}	Chip select setup time	20		ns	-
	T_{CH}	Chip select hold time	60		ns	
SDI	T_{SISU}	Data input setup time	30		ns	-
	T_{SIH}	Data input hold time	30		ns	
SDO	T_{SOD}	Data output setup time		130	ns	-
	T_{SOH}	Data output hold time	0		ns	

23.2.3 RGB Interface

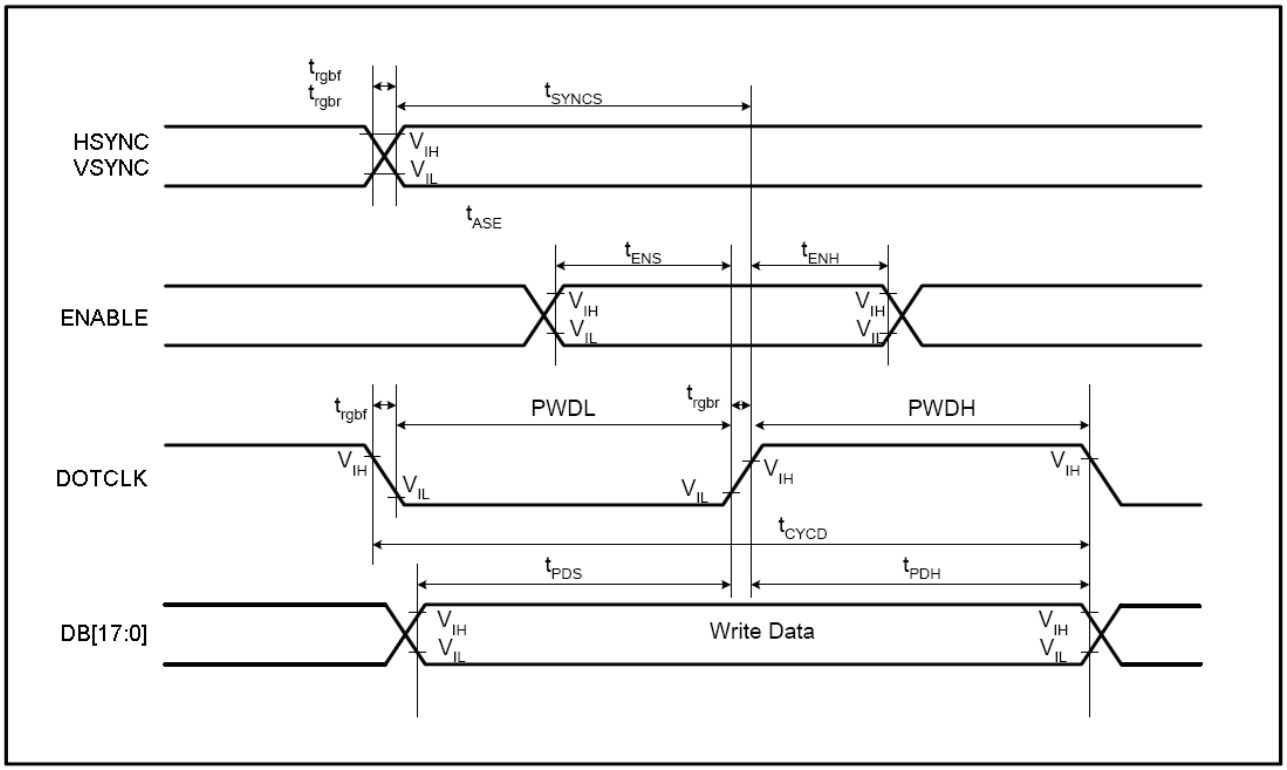


Figure 38 Timing chart for RGB Interface

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65~3.3V, VCI=2.5~3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
VSYNC	T_{SYNCS}	VSYNC setup time	30		ns	-
	T_{rghr}	VSYNC rise time		15	ns	
	T_{rghf}	VSYNC fall time		15	ns	
HSYNC	T_{SYNCS}	HSYNC setup time	30		ns	-
	T_{rghr}	HSYNC rise time		15	ns	
	T_{rghf}	HSYNC fall time		15	ns	
ENABLE	T_{ENS}	ENABLE setup time	30		ns	-
	T_{ENH}	ENABLE hold time	30		ns	
DB[17:0]	T_{PDS}	Data input setup time	40		ns	-
	T_{PDH}	Data input hold time	40		ns	
DOTCLK	PWDH	DOTCLK “H” pulse width	40		ns	-
	PWDL	DOTCLK “L” pulse width	40		ns	
	T_{CYCD}	DOTCLK clock cycle	100		ns	
	T_{rghr}	DOTCLK rise time		15	ns	
	T_{rghf}	DOTCLK fall time		15	ns	

23.3 Reset Timing Characteristics

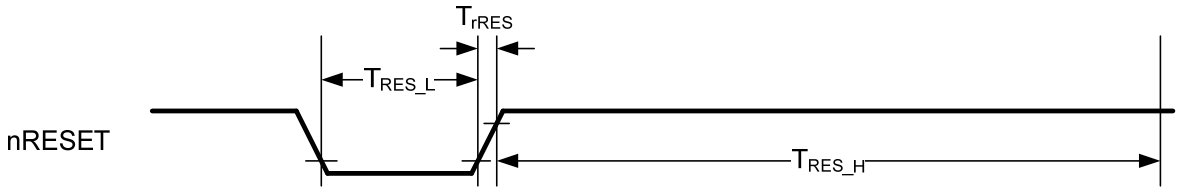


Figure 39 Reset Operation

Reset Timing Characteristics (VCI = 2.5 ~ 3.3 V, IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	MIN	MAX	Unit	Description
Reset low-level width	T_{RES_L}	1		ms	-
Reset rise time	T_{rRES}		10	us	-
Reset high-level witdth	T_{RES_H}	50		ms	-