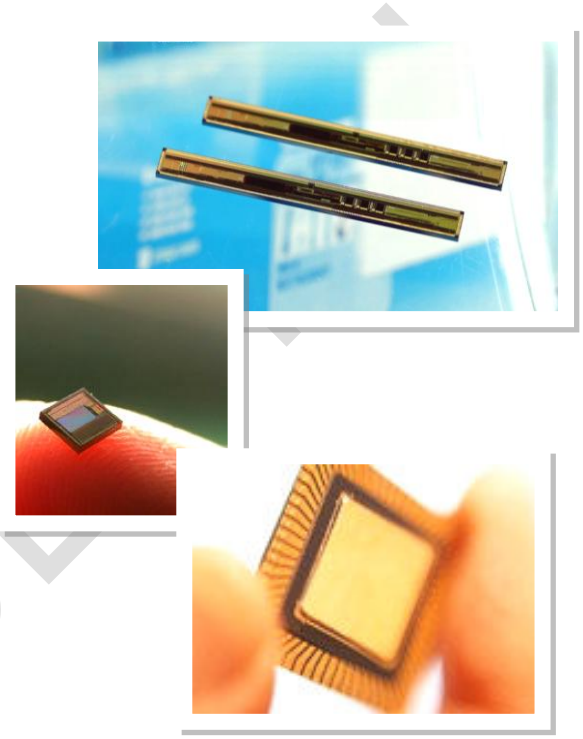
Raydium 瑞鼎科技股份有限公司
Raydium Semiconductor Corporation



# RM69090 Data Sheet

**Single Chip Driver with 16.7M color**
**for 480RGBx480 OLED driver**



***Revision：0.1***
***Date：Mar, 22 2019***

**Revision History**

| Version No. | Date | Description | Page | Modified By | Checked By |
|---|---|---|---|---|---|
| 0.1 | 2019/03/22 | First Release | | Howard Hsiung | CN.Lin |

# TABLE OF CONTENTS

# 1. General Description

The RM69090 device is a single-chip solution for LTPS AMOLED that incorporates gate drivers and is capable of 480RGBx480, 400RGBx400, 360RGBx480, 320RGBx320, 320RGBx480, 272RGBx480, 240RGBx240, 240RGBx320, 180RGBx360, 180RGBx540, 128RGBx432with internal GRAM. It includes a 2,764,800 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The RM69090 supports MIPI Interface, 8-bit system interfaces, serial peripheral interfaces (SPI), dual serial peripheral interfaces (Dual-SPI). The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The RM69090 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 480 x 480 x 1/2 x 24 bits for 16.77M-color images. A deep standby mode is also supported for lower power consumption.

This LSI is suitable for wearable device applications, including I-watch and smart band.

# 2. Features

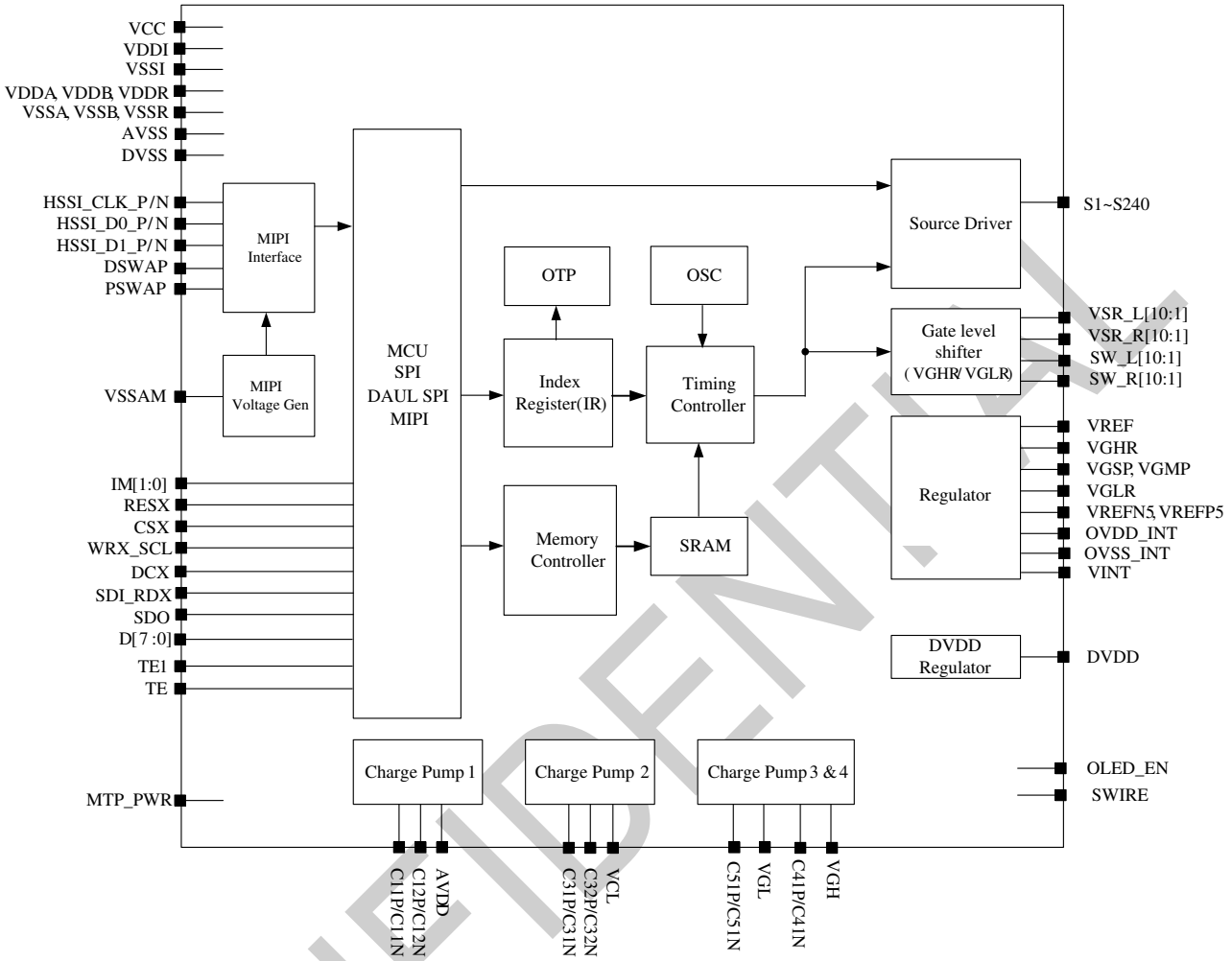
- **Single chip AMOLED controller/driver with display RAM**
- **Display resolution option**
  - 480RGB x 480
  - 400RGB x 400
  - 360RGB x 480
  - 320RGB x 320
  - 320RGB x 480
  - 272RGB x 480
  - 240RGB x 240
  - 240RGB x 320
  - 180RGB x 360
  - 180RGB x 540
  - 128RGB x 432
- **Display data RAM (frame memory): 2,764,800 bits**
- **Display mode (Color mode)**
  - Normal mode: 16.7M-colors, 4096-colors, 8-colors
  - Idle mode: 16.7M-colors, 4096-colors, 8-colors
- **Interface**
  - 8-bits 80-series MPU interface
  - Serial peripheral interface (SPI)
  - Dual serial peripheral interface (Dual-SPI)
  - MIPI Display Serial Interface (1 clock and 2 data lane pairs)
    - Support 1lane/2lane (1lane: 500Mbps)
    - Maximum total bit rate is 500Mbps of 2 data lanes 24-bit data format/ 360Mbps of 2 data lanes 18-bit data format/ 320Mbps of 2 data lanes 16-bit data format
- **Interface pixel format**
  - MIPI: RGB888/ RGB666/ RGB565
  - SPI: RGB888/ RGB666/ RGB565/ RGB332/ RGB111/ Gray 256.
- **Abundant color display and drawing functions**
  - Programmable γ-correction function for 16.7 million color display
  - Individual gamma correction setting for RGB dots
  - Partial display function
- **Sunlight readable**
- **Control power IC by one-wire interface**
- **On chip**
  - VREFP5/VREFN5 voltage generator for panel voltage
  - VGHR/VGLR voltage for gate control signal
  - Internal oscillator for display clock
  - Source output MUX 1-6 with 240ch source output pins
  - Supports gate control signals to gate driver in the panel

- **Built-in OTP function to adjust panel setting**
- **Logic / interface power supply voltage VDDI = 1.65V ~ 3.3V**
- **Analog power supply voltage VDD = 2.7V ~ 3.6V**
- **Output voltage levels**
  - Positive gate driver voltage range for VGHR: 3 ~ 10.5V (Max<=VGH-0.3v)
  - Negative gate driver voltage range for VGLR: -2V ~ -9.5V (Min>=VGL+0.3v)
  - VREFP5 panel voltage range : 0~5V (Max<=AVDD-0.3v)
  - VREFN5 panel voltage range : -0.5~-4.5V (Min>=VCL+0.3v)
  - Step-up 1,2 output voltage range for AVDD: 4.5 ~ 6.5V, VCL: -3.5 ~ -5.0V
  - Gamma high/low voltage range for VGMP: 2.0V ~ 6.0V (Max<=AVDD-0.5v) , VGSP: 0V, 0.2125V ~ 4.5V
- **Package: COF/COG**
- **Chip size evaluation : 8300um x 2060um(including scribe line)**

## ■ Power Supply Specifications

| No. | Item | | Description |
|---|---|---|---|
| 1 | Source Driver | | 240 pins (480 x RGB) |
| 2 | gate control timing Level shift | | VGHR-VGLR |
| 3 | Input Voltage | VDDI | 1.65 ~ 3.3V |
| | | VCC | Connect to VDDI or VDD(VCI) |
| | | VDD (VDDA/VDDB/VDDR) | 2.70 ~ 3.60V |
| 4 | OLED drive voltages | AVDD | 4.5V ~ 6.5V |
| | | VGHR | 3V ~ 10.5V (Max<=VGH-0.3v) |
| | | VGLR | -2V ~ -9.5V (Min>=VGL+0.3v) |
| | | VREFP5 | 0V ~ 5V (Max<=AVDD-0.3v) |
| | | VREFN5 | -0.5V ~ -4.5V (Min>=VCL+0.3v) |
| 5 | Internal step-up circuits | AVDD | VCI x2.0(dual), x3.0(single) |
| | | VCL | VCI x -1.0(dual), x-2.0(single) |
| | | VGH | VCI x2, x3, x4 |
| | | VGL | VCI x-2, x-3, x-4 |

# 3. Block Diagram






### Interface

The RM69090 supports MIPI DSI interface. MIPI DSI can access both internal command and display data.

### Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a drive voltage, which corresponds to grayscale level set in the γ correction register. The RM69090 displays 16.7M colors at the maximum.

### Power Supply Circuit

The power supply circuit generates supply voltages to OLED panel, VGH, VGL.

### Timing Generating

The timing controller generates timing signals for internal circuits such as the display timing.

### Oscillator

The RM69090 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

### Panel Driver Circuit

The OLED display driver circuit consists of 240 source drivers (S1~S240). The gate signal consists of VSR_R/L[1:10], SW_R/L[1:10] and outputs either VGHR or VGLR level.

# 4. Pin Description

## 4.1 Power Supply Pins

| Signal | I/O | Function |
|---|---|---|
| VDDB | P | Power supply for DC/DC converter<br>VDDB, VDDA and VDDR should be the same input voltage level |
| VDDA | P | Power supply for analog system.<br>VDDB, VDDA and VDDR should be the same input voltage level |
| VDDR | P | Power supply for regulator system<br>VDDB, VDDA and VDDR should be the same input voltage level |
| VDDI | P | Power supply for interface system except MIPI interface. |
| VCC | P | Power supply for DVDD regulator |
| VSSB | P | System ground for DC/DC converter |
| VSSA | P | System ground for analog system |
| VSSR | P | System ground for regulator system |
| VSSAM | P | System ground for internal MIPI analog system |
| VSSI | P | System ground for interface system except MIPI interface |
| DVSS | P | System ground for internal digital system |
| AVSS | P | System ground for source OP system. |
| MTP_PWR | P | MTP programming power supply pin (7.5V typical)<br>Must be left open or connected to DVSS in normal condition. |

## 4.2 Interface Pins

| Signal | I/O | Function |
|---|---|---|
| CSX | I | Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F.<br>If not used, please connect to VDDI. |
| WRX_SCL | I | WRX : Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F.<br>SCL: A synchronous clock signal in SPI I/F.<br>If not used, please connect to VSSI. |
| D/CX | I | Display data / command selection in 80-series MPU I/F and 4-wire SPI I/F.<br>D/CX = ”0” : Command<br>D/CX = ”1” : Display data or Parameter<br>If not used, please connect to VSSI. |
| SDI_RDX | I/O | SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal.<br>RDX : Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface.<br>If not used, please leave it Open. |
| SDO | O | Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal.<br>If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together.<br>If not used, please open this pin. |
| D[7:0] | I/O | 8-bit bi-directional data bus for 80-series MPU I/F and 8-bit input data bus for RGB I/F.<br>These pins are not used for SPI, MIPI, please leave it Open. |

## 4.3 MIPI Interface Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>HSSI_CLK_P<br>HSSI_CLK_N</td><td>I</td><td>-These pins are DSI-CLK+/- differential clock signals if MIPI interface is used.<br>-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D0_P<br>HSSI_D0_N</td><td>I/O</td><td>-These pins are DSI-D0+/- differential data signals if MIPI interface is used.<br>-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D1_P<br>HSSI_D1_N</td><td>I/O</td><td>-These pins are DSI-D1+/- differential data signals if MIPI interface is used.<br>-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>DSWAP<br>PSWAP</td><td>I</td><td>Input pin to select HSSI_D0/D1 data lane sequence and polarity in high speed interface only.
<table>
<tr><th>Pin Name</th><th>HSSI_D0_P</th><th>HSSI_D0_N</th><th>HSSI_CLK_P</th><th>HSSI_CLK_N</th><th>HSSI_D1_P</th><th>HSSI_D1_N</th></tr>
<tr><td>DSWAP=0<br>PSWAP=0</td><td>DSI<br>D0+</td><td>DSI<br>D0-</td><td>DSI<br>CLK+</td><td>DSI<br>CLK-</td><td>DSI<br>D1+</td><td>DSI<br>D1-</td></tr>
<tr><td>DSWAP=0<br>PSWAP=1</td><td>DSI<br>D0-</td><td>DSI<br>D0+</td><td>DSI<br>CLK-</td><td>DSI<br>CLK+</td><td>DSI<br>D1-</td><td>DSI<br>D1+</td></tr>
<tr><td>DSWAP=1<br>PSWAP=0</td><td>DSI<br>D1+</td><td>DSI<br>D1-</td><td>DSI<br>CLK+</td><td>DSI<br>CLK-</td><td>DSI<br>D0+</td><td>DSI<br>D0-</td></tr>
<tr><td>DSWAP=1<br>PSWAP=1</td><td>DSI<br>D1-</td><td>DSI<br>D1+</td><td>DSI<br>CLK-</td><td>DSI<br>CLK+</td><td>DSI<br>D0-</td><td>DSI<br>D0+</td></tr>
</table>
If not used, please connect to VSSI.</td></tr>
</table>

**NOTE: “1” = VDDI level, “0” = VSSI level.**

## 4.4 Interface Logic Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>RESX</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip.<br>Signal is active low.</td></tr>
<tr><td>IM[1:0]</td><td>I</td><td>Interface type selection. The connections of IM[1:0] which not shown in table are invalid.
<table>
<tr><th>IM[1:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>00</td><td>MIPI / 3-wire SPI</td><td>MIPI / 3-wire SPI</td></tr>
<tr><td>01</td><td>MIPI / 4-wire SPI</td><td>MIPI / 4-wire SPI</td></tr>
<tr><td>10</td><td>MIPI / QAD-SPI</td><td>MIPI / QAD-SPI</td></tr>
<tr><td>11</td><td>MCU 8-bit</td><td>MCU 8-bit</td></tr>
</table></td></tr>
<tr><td>BSTM</td><td>I</td><td>Boost mode selection pin.
<table>
<tr><th>BSTM</th><th>Mode</th></tr>
<tr><td>0</td><td>2 PWR(VDDI, VCI)<br>AVDD --> internal CP<br>VCL --> internal CP</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>TE</td><td>O</td><td rowspan="2">Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.<br>When this pin is not activated, this pin is output low.<br>If not used, please open this pin.</td></tr>
<tr><td>TE1</td><td>O</td></tr>
<tr><td>SWIRE</td><td>O</td><td>Swire protocol setting pin of Power IC, If not used, please open this pin.</td></tr>
<tr><td>OLED_EN</td><td>O</td><td>Power IC enable control pin, If not used, please open this pin.</td></tr>
</table>

**NOTE: “1” = VDDI level, “0” = VSSI level.**

## 4.5 Driver Output Pins (Pins for Panel)

| Signal | I/O | Function |
|---|---|---|
| S1 ~ S240 | O | Pixel electrode driving output. |
| SDMY[1] ~ SDMY[21] | O | Dummy Source, leave it Open. |
| VSR_L[10:1]<br>VSR_R[10:1] | O | VSR control signals, Level shift output, (VGHR-VGLR) |
| SW_L[10:1]<br>SW_R[10:1] | O | VSR control signals, Level shift output, (VGHR-VGLR) |

## 4.6 DC/DC Convert Pins

| Signal | I/O | Function |
|---|---|---|
| AVDD | O | Output voltage from step-up circuit 1, generated from VDDB.<br>Connect a capacitor for stabilization. |
| VCL | O | Output voltage from step-up circuit 3, generated from VDDB.<br>Connect a capacitor for stabilization. |
| VGH | O | Output voltage from step-up circuit 4.<br>Connect a capacitor for stabilization. |
| VGL | O | Output voltage from step-up circuit 5.<br>Connect a capacitor for stabilization. |
| C11P, C11N<br>C12P, C12N | IO | Capacitor connection pins for the step-up circuit which generate AVDD.<br>Connect capacitor as requirement. When not in used, please open these pins. |
| C31P, C31N<br>C32P, C32N | IO | Capacitor connection pins for the step-up circuit which generate VCL.<br>Connect capacitor as requirement. |
| C41P, C41N | IO | Capacitor connection pins for the step-up circuit which generate VGH.<br>Connect capacitor as requirement. |
| C51P, C51N | IO | Capacitor connection pins for the step-up circuit which generate VGL.<br>Connect capacitor as requirement. |
| VGHR | O | Output voltage generated from VGH. LDO output used for panel voltage.<br>Connect a capacitor for stabilization.<br>When not in use, please open this pin. |
| VGLR | O | Output voltage generated from VGL. LDO output used for panel voltage.<br>Connect a capacitor for stabilization.<br>When not in use, please open this pin. |
| VGMP | O | Output voltage generated from AVDD. LDO output for positive gamma high voltage generator. |
| VGSP | O | Output voltage generated from AVDD. LDO output for positive gamma low voltage generator. |
| VREF | O | Regulator output for internal reference voltage.<br>Connect capacitor for stabilization. |
| DVDD | O | Regulator output for logic system power.<br>Connect a capacitor for stabilization. |
| VREFP5 | O | Regulator output for VREFP(0~5V) |
| VREFN5 | O | Regulator output for VREFP(-0.5~-5V) |
| VINT | O | Connect a capacitor for stabilization. |

## 4.7 Test Pins

| Signal | I/O | Function |
|---|---|---|
| ANALOG_TEST 1~2 | O | Test pin, not accessible to user. Must be left open. |
| TEST1~3 | IO | Test pin, not accessible to user. Must be left open. |
| TESTEN | I | Test pin, not accessible to user. Must be left open., Internal pull low |
| EXTCLK | I | Test pin, not accessible to user. Must be left open. |
| DUMMY | I | Dummy PAD, leave it open |

# 5. Function Description

## 5.1 Interface Type Selection

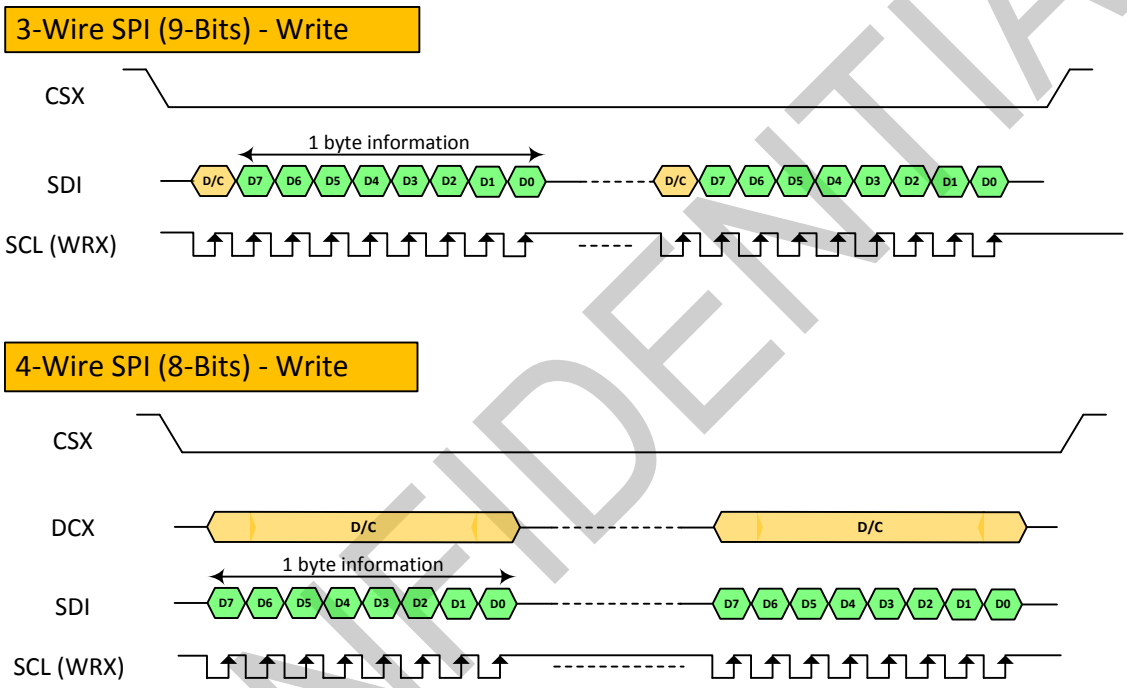
Interface type selection. The connections of IM[1:0] which not shown in table are invalid.

| IM[1:0] | Display Data | Command |
|---|---|---|
| 00 | MIPI / 3-wire SPI | MIPI / 3-wire SPI |
| 01 | MIPI / 4-wire SPI | MIPI / 4-wire SPI |
| 10 | MIPI / QAD-SPI | MIPI / QAD-SPI |
| 11 | MCU 8-bit | MCU 8-bit |

## 5.2 Three-wire/four-wire SPI Interface

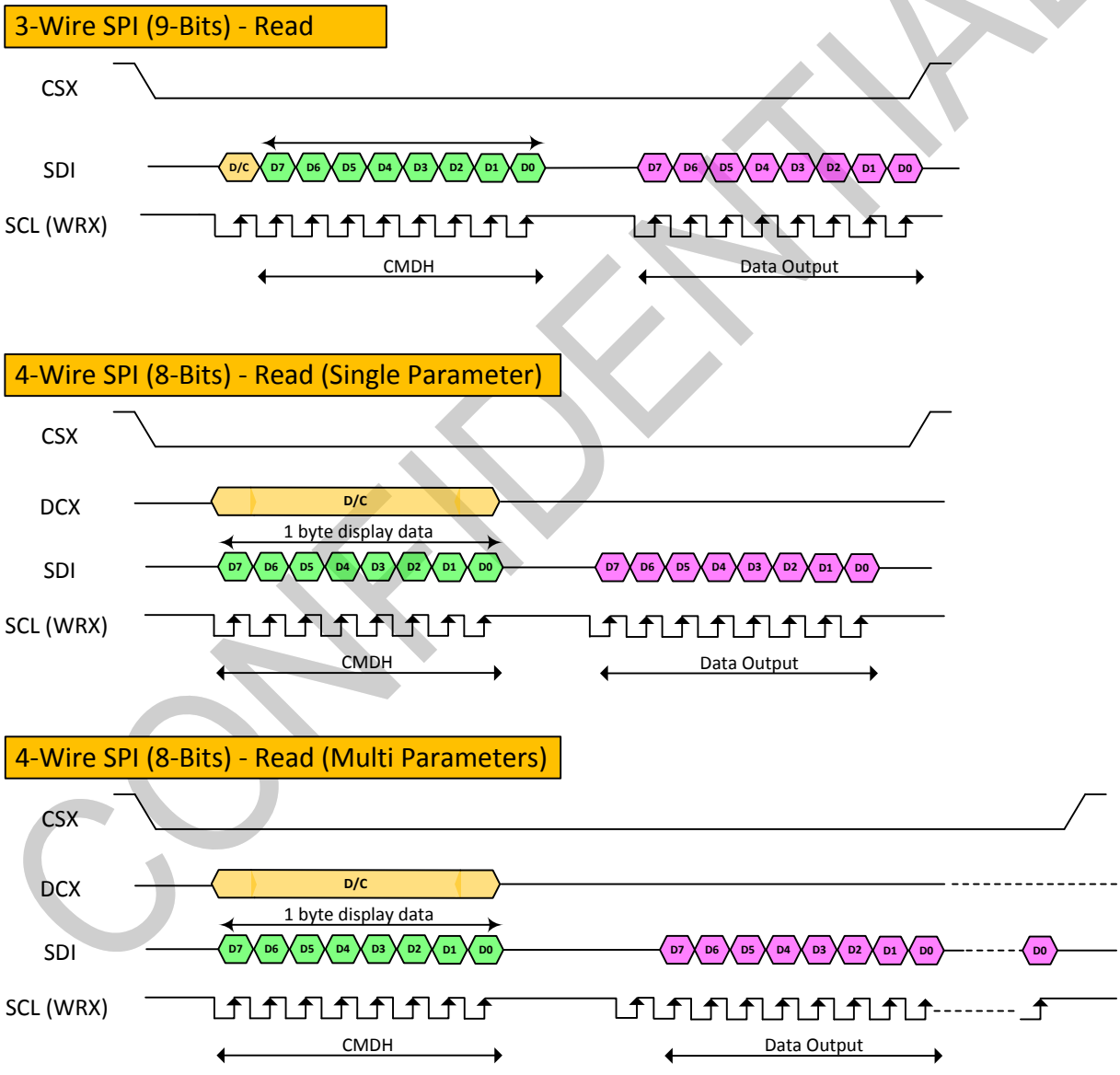
### 5.2.1 Write Cycle and Sequence

During a write cycle, the host processor sends a series bit string of either command or display data to the display module via the interface. The 3-wire SPI utilizes CSX, SCL, and SDA for data transmission. As to 4-wire SPI, DCX is a must for the host to indicate whether the input information is data/parameter or command.
The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. SCL is driven from high to low then pulled back to high during the write cycle for the data latch. Therefore, the host must transmit valid information on the rising edge of SCL with enough setup time and hold time. DCX is driven low while command is input and pulled to high while input information are data/parameter. The 3-wire/4-wire SPI interface write command sequences are illustrated in the following figures.



### 5.2.2 Read Cycle and Sequence

During a read cycle, the host reads a single bit of data from the display module via the interface. The 3-wire/4-wire SPI interface utilizes CSX, SCL and SDA for data transmission. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides readout information during the read cycle while the host reads the display module information back on the rising edge of SCL. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. The 3-wire/4-wire SPI interface read command sequences are described in the following figure.
There is one restriction for the read operation of this interface, and that is, not all data can be readout. Only the data with the following address in the DCS can be read, and they are 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, DAh, DBh, DCh, 52h, 54h, 59h, 64h, AAh, AFh, DAh, DBh, DCh, E1h, E2h, and E3h. An extra dummy clock as depicted in the following is necessary for those multi-parameter addresses such as 04h, 45h, A1h, and A8h.

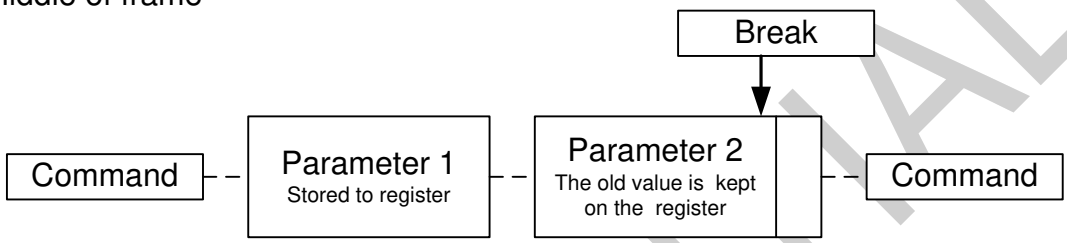


### 5.2.3 Break and Pause Sequence

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

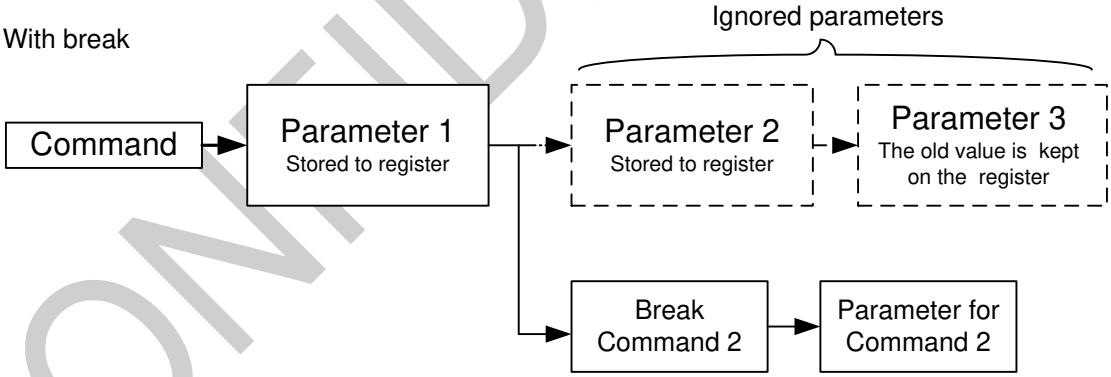
1. Middle of frame




2. Between frames

Without break


With break




Break can be e.g. another command or noise pulse.

## 5.3 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

RM69090 is capable of both Command Mode operation and Video Mode operation. Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a display module that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller.

The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface. Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

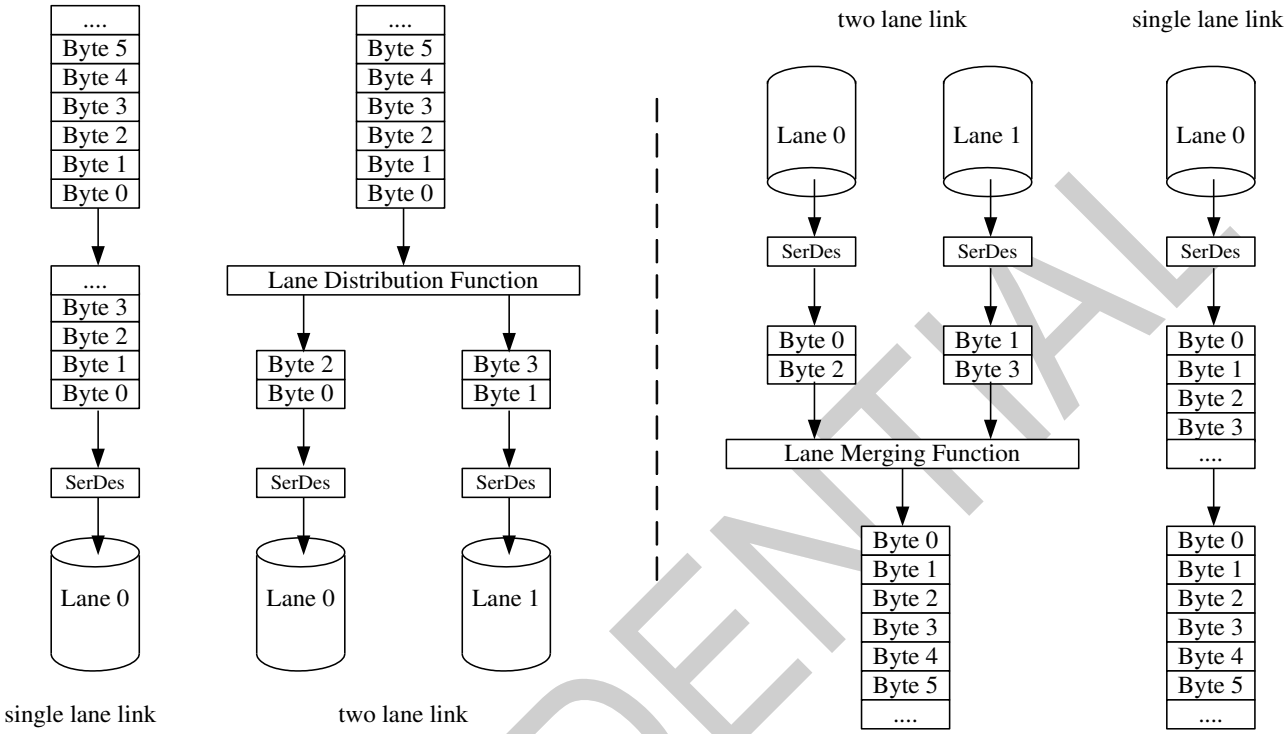
RM69090 Video Mode architectures also include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to reduce power consumption.

RM69090 Configuration:

| Lane Pair | MCU(Master)　RM69090(Slave) |
|---|---|
| Clock Lane | Unidirectional Lane<br>Clock only |
| Data Lane 0 | Bi-directional Lane<br>Forward High-speed<br>Bi-directional Escape Mode<br>Bi-directional LPDT |
| Data Lane 1 | Unidirectional Lane<br>Forward High-Speed<br>Escape Mode<br>No LPDT |

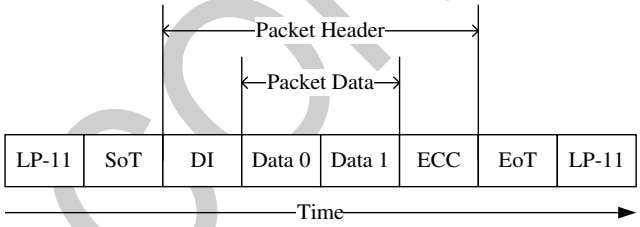
### 5.3.1 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted to packets. These packets are sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.




There are two kinds of packets, **short packet and long packet**.

Short packet structure:
LP-11: low power mode
SoT: start of transmission
DI: data identification
Data 0, Data1: packet data
ECC: error correction code
EoT: End of Transmission



DI structure:
Virtual Channel: these two bits identify the data as directed to one of four virtual channels
Data Type: It specifies the packet structure and packet format

| Virtual Channel (VC) | | Data Type (DT) | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

Long packet structure:
LP-11: low power mode
SoT: start of transmission
DI: data identification
Word Count: the number of data bytes of packet data
ECC: error correction code
Checksum: The 16-bit CRC generator to check packet data. If the calculated checksum of receiver are equal to the packet data, the packet data is correct. If the calculated checksum of receiver are not equal, the packet data are not correct.

EoT: end of transmission

### 5.3.2 Processor to Peripheral Transactions

Processor to Peripheral Direction Packet Data Types

| Data Type | Data Type binary | Description | Packet Size |
|---|---|---|---|
| 01h | 00 0001 | Sync Event, V Sync Start | Short |
| 11h | 01 0001 | Sync Event, V Sync End | Short |
| 21h | 10 0001 | Sync Event, H Sync Start | Short |
| 31h | 11 0001 | Sync Event, H Sync End | Short |
| 08h | 00 1000 | End of Transmission packet (EoTp) | Short |
| 02h | 00 0010 | Color Mode (CM) Off Command | Short |
| 12h | 01 0010 | Color Mode (CM) On Command | Short |
| 22h | 10 0010 | reserved | Short |
| 32h | 11 0010 | reserved | Short |
| 03h | 00 0011 | reserved | Short |
| 13h | 01 0011 | Generic Short WRITE, 1 parameter | Short |
| 23h | 10 0011 | Generic Short WRITE, 2 parameters | Short |
| 04h | 00 0100 | reserved | Short |
| 14h | 01 0100 | Generic READ, 1 parameter | Short |
| 24h | 10 0100 | Generic READ, 2 parameters | Short |
| 05h | 00 0101 | DCS Short WRITE, no parameters | Short |
| 15h | 01 0101 | DCS Short WRITE, 1 parameter | Short |
| 06h | 00 0110 | DCS READ, no parameters | Short |
| 37h | 11 0111 | Set Maximum Return Packet Size | Short |
| 09h | 00 1001 | Null Packet, no data | Long |
| 19h | 01 1001 | Blanking Packet, no data | Long |
| 29h | 10 1001 | Generic Long Write | Long |
| 39h | 11 1001 | DCS Long Write/write_LUT Command Packet | Long |
| 0Eh | 00 1110 | Packed Pixel Stream, 16-bit RGB, 5-6-5 Format | Long |
| 1Eh | 01 1110 | Packed Pixel Stream, 18-bit RGB, 6-6-6 Format | Long |
| 2Eh | 10 1110 | Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format | Long |
| 3Eh | 11 1110 | Packed Pixel Stream, 24-bit RGB, 8-8-8 Format | Long |

Sync Event, Data Type = xx 0001
Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode.

EoT packet
This short packet is used to indicate the end of a high speed (HS) transmission. This packet will enhance overall syntem reliability. Although the main objective of the EoTp is to enhance robustness during HS transmission mode, RM69090 can detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes)

Color Mode Off / On Command
They are short packet commands to switch video display module between normal display mode and low-color mode for power saving.

Generic short write / read packet
Generic Short WRITE command is a Short packet type for sending generic data to the peripheral. Generic READ request is a Short packet requesting data from the peripheral.

DCS commands
DCS short write command
DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h.

DCS read commands
The commands are used to request data from s display module.

DCS Long Write / write_LUT command
The commands are used to send larger blocks of data to a display module.

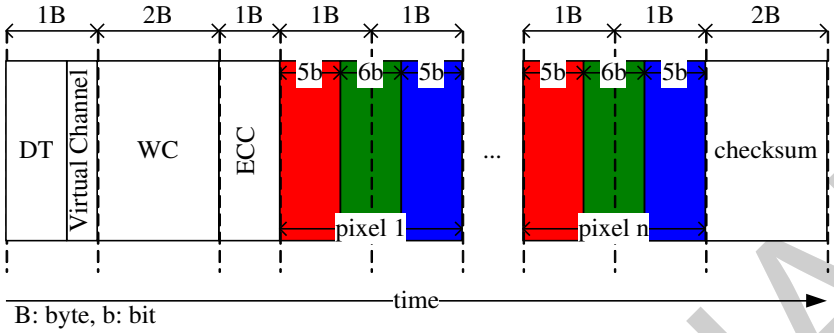
Maximum return packet size
This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

Null Packet
This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

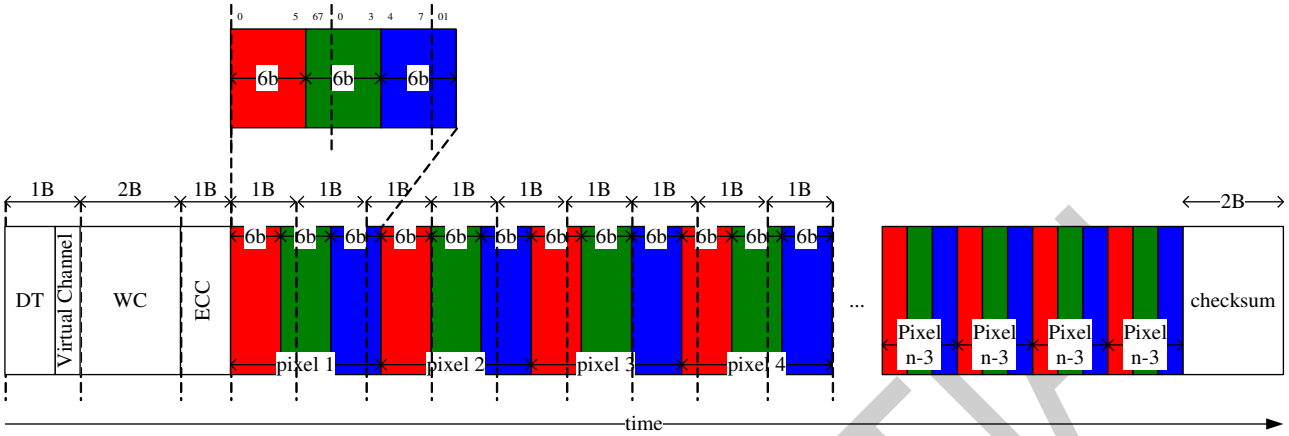
Blanking Packet
A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

Generic Long Write
This is used to transmit arbitrary blocks of data from a host processor to a peripheral.

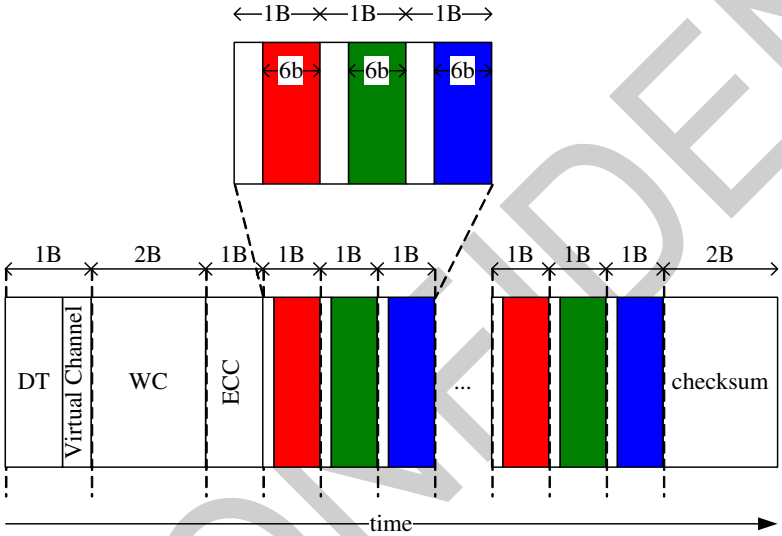
Packed Pixel Stream, 16-bit Format, Data Type: 00 1110
The pixel format is five bits red, six bits green and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.



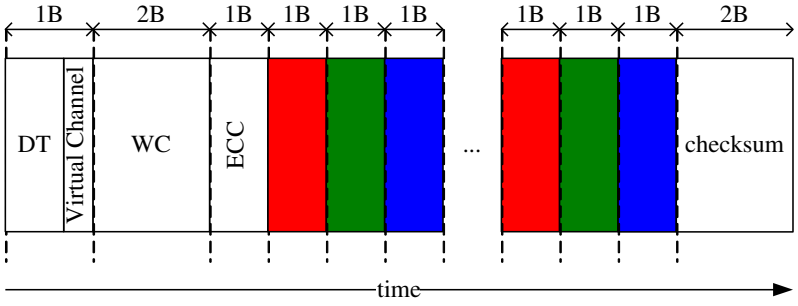
Packet pixel stream, 18-bit format, Data Type: 01 1110
The pixel format is six bits red, six bits green and six bits blue. Within a color component, the LSB is sent first, the MSB last.




Packet pixel stream, 18-bit format in three bytes, Data Type: 10 1110
This is 18-bit pixel lossely packed format, each R, G or B color component is six bits but shifted to the upper bits of byte.



Packet pixel stream, 24-bit format, Data Type: 11 1110
The pixel format is eight bits red, eight bits green and eight bits blue.



### 5.3.3 Peripheral-to-Processor LP Transmission

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use low power mode transmission.

Packet structure for peripheral-to-processor transaction is the same as for the processor-to-peripheral direction. For the processor-to-peripheral direction, two basic packet formats are the same as the peripheral-to-processor direction: Short and Long packet structure. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

There are four basic types of peripheral-to-processor transactions.

Tearing Effect: It is a Trigger message sent to convey display timing information to the host processor.
Acknowledge: It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.

Acknowledge and Error Report: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor.
Response to Read Request: It may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:
Following a non-Read command: If no errors were detected, the peripheral shall respond with Acknowledge.

Following a Read request: The peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.

Following a Read request: If only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet and a 4-byte Acknowledge and Error Report packet in the same LP transmission.

Following a non-Read command: If only a single-bit ECC error was detected and corrected, the peripheral shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet.

Following a Read request: If multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data.

Following a non-Read command: If multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet.

Following any command: If SoT Error, SoT Sync Error, the VC of DSI or the ID of DSI Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response.

Following any command: If EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet.

### 5.3.4 Error Report Format

The following table shows the bit assignment for all error report.

| Bit | Description |
|---|---|
| 0 | SoT Error |
| 1 | SoT Sync Error |
| 2 | EoT Sync Error |
| 3 | Escape Mode Entry Command Error |
| 4 | Low-Power Transmit Sync Error |
| 5 | HS Receive Timeout Error |
| 6 | False Control Error |
| 7 | Reserved |
| 8 | ECC Error, single-bit (detected and corrected) |
| 9 | ECC Error, multi-bit (detected, not corrected) |
| 10 | Checksum Error (Long packet only) |
| 11 | DSI Data Type Not Recognized |
| 12 | DSI VC ID Invalid |
| 13 | reserved |
| 14 | reserved |
| 15 | reserved |

### 5.3.5 Peripheral-to-Processor Transaction – Detail Format Description

The following list is the complete set of peripheral-to-processor data types.

| Data type, hex | Data type binary | Description | Packet size |
|---|---|---|---|
| 02h | 00 0010 | Acknowledge and error report | short |
| 08h | 00 1000 | reserved | short |
| 11h | 01 0001 | GEN short read reponse, 1byte returned | short |
| 12h | 01 0010 | GEN short read reponse, 2bytes returned | short |
| 1Ah | 01 1010 | Generic long read reponse | long |
| 1Ch | 01 1100 | DCS long read reponse | long |
| 21h | 10 0001 | DCS short read reponse, 1byte returned | short |
| 22h | 10 0010 | DCS short read reponse, 2bytes returned | short |

Acknowledge and error report: It is sent with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.

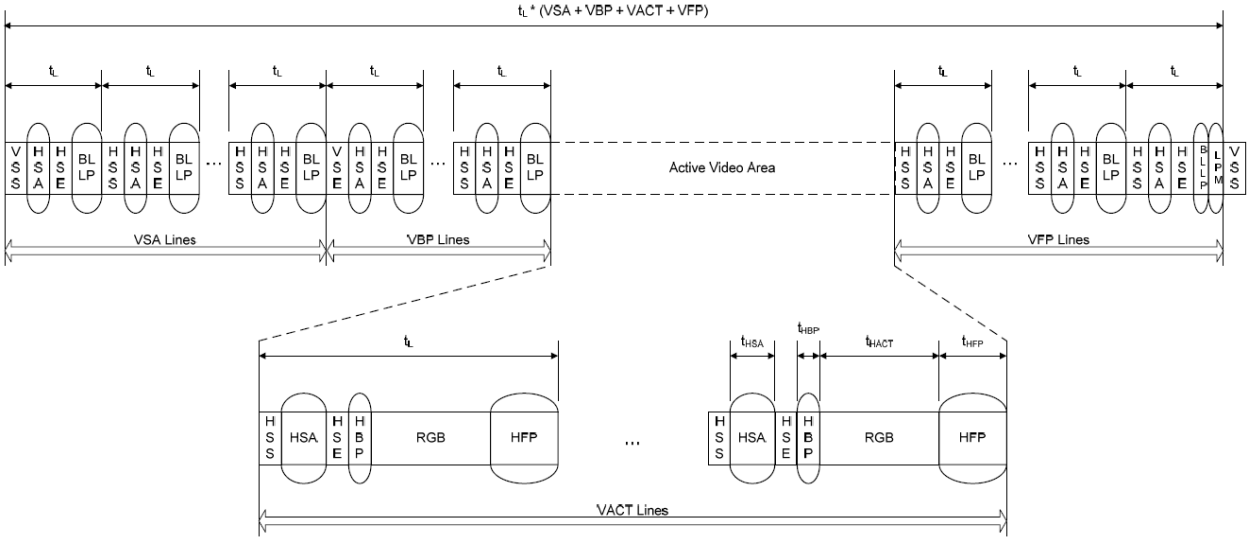
Generic Short Read Response: This is the short-packet response to Generic READ Request. Packet composition is the Data Identifier (DI) byte, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

Generic long read reponse: This is the long-packet response to Generic READ Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS long read reponse: This is a Long packet response to DCS Read Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS short read reponse: This is the short-packet response to DCS Read Request. Packet composition is DI, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

### 5.3.6 DSI Video Mode Interface Timing



### 5.3.7 Error Correction Code (ECC)

ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals with Bidirectional Links shall also generate and send ECC.

The number of parity or error check bits required is given by the Hamming rule, which uses parity to correct a single-bit error or detect a two-bit error, but are not capable of doing both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both single error correction as well as two-bit error detection.

Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set both bits to zero before processing ECC.

The parity bits of ECC are defined as below:
P7 = 0
P6 = 0
P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

The table below shows a compact way to specify the encoding of parity and decoding of syndromes.

ECC Parity Generation Rules:

| Data Bit | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | Hex |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0x07 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0x0B |
| 2 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0x0D |
| 3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0x0E |
| 4 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0x13 |
| 5 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0x15 |
| 6 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0x16 |
| 7 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0x19 |
| 8 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0x1A |
| 9 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0x1C |
| 10 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0x23 |
| 11 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0x25 |
| 12 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0x26 |
| 13 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0x29 |
| 14 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0x2A |
| 15 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0x2C |
| 16 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0x31 |
| 17 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0x32 |
| 18 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0x34 |
| 19 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0x38 |
| 20 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0x1F |
| 21 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0x2F |
| 22 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0x37 |
| 23 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0x3B |

**5.3.8 Notice**

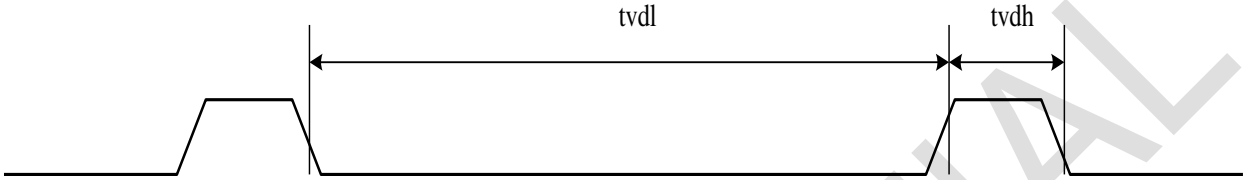
1. We recommend users to stay in STOP state for 500ns when switching from LPDT to HSDT.
2. We recommend users to adopt EoTp to enhance overall robustness of the system during HSDT.

## 5.4 Tearing Effect Output

The tearing effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

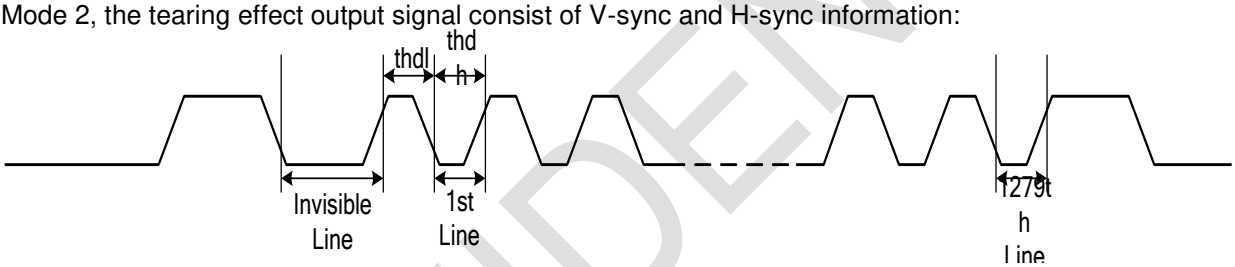
### 5.4.1 Tearing Effect Line Mode

Mode 1, the tearing effect output signal consist of V-sync information only:



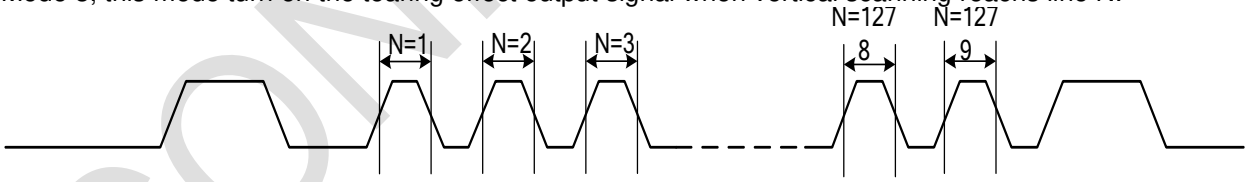

tvdh = Display is not updated from the frame memory.
tvdl = Display is updated from the frame memory.

Mode 2, the tearing effect output signal consist of V-sync and H-sync information:

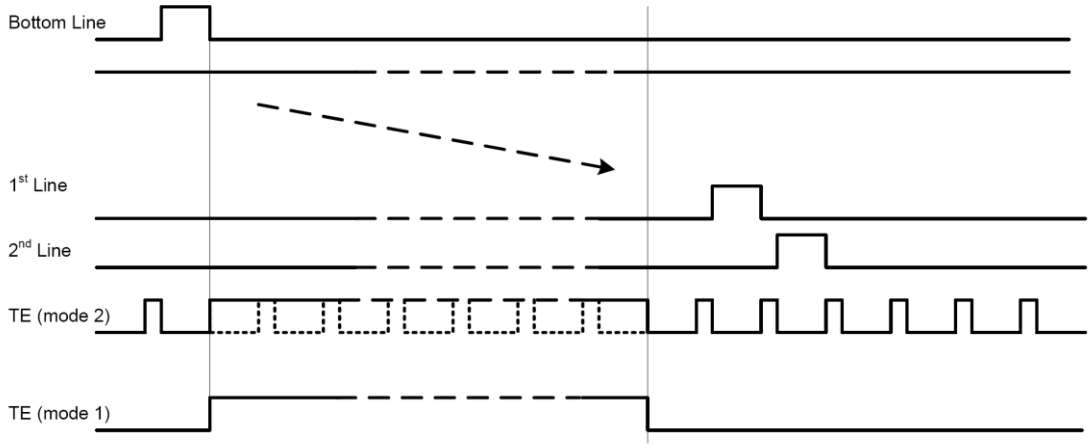



thdh = Display is not updated from the frame memory.
thdl = Display is updated from the frame memory.

Mode 3, this mode turn on the tearing effect output signal when vertical scanning reachs line N.



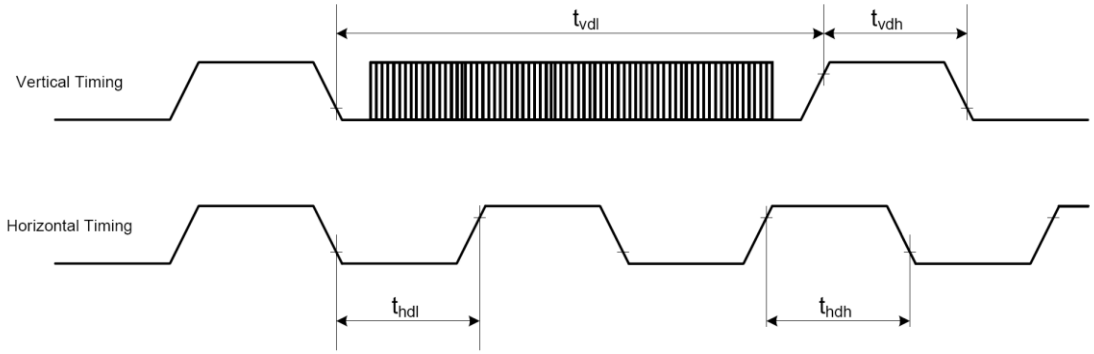

N = The N-th scanning line which set by register N[15:0] of command STESL(44h).




Note. During Sleep In mode, the tearing effect output signal is active low.

### 5.4.2 Tearing Effect Line Timing

The tearing effect signal is described as below:

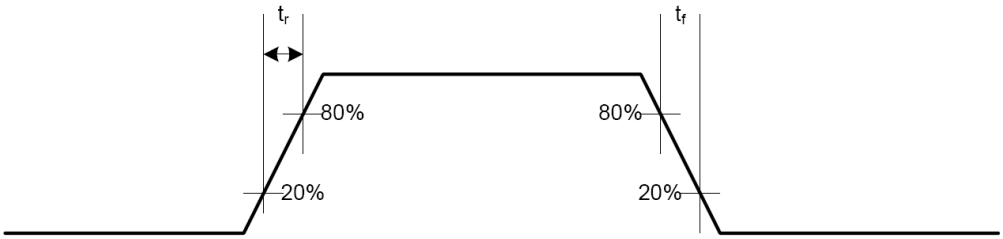



AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

| Symbol | Parameter | Typ. | Unit | Description |
|---|---|---|---|---|
| tvdl | Vertical timing low duration | | | 1*frame time- tvdh |
| tvdh | Vertical timing high duration | | | tvdh =V Porch time if STS[15:0]=0.<br>tvdh =31* line time if STS[15:0] not equal to 0. |
| thdl | Horizontal timing low duration | | | 1* line time- 32*PCLK |
| thdh | Horizontal timing high duration | 1.45 | us | 32*PCLK |

Notes:

1. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.




The Tearing Effect Output Line is fed back to the HOST and should be used as shown below to avoid tearing effect:

The Tearing Effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

| TEON (35h) | TELOM (35h, 1st bit) | TE signal Output |
|---|---|---|
| 0 | * | GND |
| 1 | 0 | TE (Mode 1) |
| 1 | 1 | TE (Mode 2) |

# 6. Command

## 6.1 Command List

| Command | | | W/R | Function | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default (hex) | MTP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Page | Add. | Para. | | | | | | | | | | | | |
| CMD1 | 00h | - | W | NOP | No Argument | | | | | | | | - | - |
| CMD1 | 01h | - | W | Software reset | No Argument | | | | | | | | - | - |
| CMD1 | 04h | 1st | R | Read display identification information | ID1[7:0] | | | | | | | | 00h | - |
| CMD1 | 04h | 2nd | | | ID2[7:0] | | | | | | | | 80h | - |
| CMD1 | 04h | 3rd | | | ID3[7:0] | | | | | | | | 00h | - |
| CMD1 | 05h | - | R | Read number of the errors on DSI | P[7:0] | | | | | | | | 00h | - |
| CMD1 | 0Ah | 1st | R | Read display power mode | BSTON | IDMON | PTLON | SLPOUT | NORON | DISPON | - | - | 08h | - |
| CMD1 | 0Bh | 1st | R | Read display MADCTR | - | MX | - | - | RGB | - | - | - | 00h | - |
| CMD1 | 0Ch | 1st | R | Read display pixel format | SPI_IFPF_SEL | VIPF2 | VIPF1 | VIPF0 | - | IFPF2 | IFPF1 | IFPF0 | 77h | - |
| CMD1 | 0Dh | 1st | R | Read display image mode | 0 | 0 | INVON | ALLPON | ALLPOFF | 0 | 0 | 0 | 00h | - |
| CMD1 | 0Eh | 1st | R | Read display signal mode | TEON | M | 0 | 0 | 0 | 0 | 0 | ERR | 00h | - |
| CMD1 | 0Fh | 1st | R | Read display self-diagnostic result | 0 | 0 | 0 | 0 | 0 | 0 | 0 | checksum_comp | 00h | - |
| CMD1 | 10h | - | W | Sleep-in | No Argument | | | | | | | | - | - |
| CMD1 | 11h | - | W | Sleep-out | No Argument | | | | | | | | - | - |
| CMD1 | 12h | - | W | Partial display mode on | No Argument | | | | | | | | - | - |
| CMD1 | 13h | - | W | Normal display mode on | No Argument | | | | | | | | - | - |
| CMD1 | 20h | - | W | Display inversion off | No Argument | | | | | | | | - | - |
| CMD1 | 21h | - | W | Display inversion on | No Argument | | | | | | | | - | - |
| CMD1 | 22h | - | W | All pixel off | No Argument | | | | | | | | - | - |
| CMD1 | 23h | - | W | All pixel on | No Argument | | | | | | | | - | - |
| CMD1 | 28h | - | W | Display off | No Argument | | | | | | | | - | - |
| CMD1 | 29h | - | W | Display on | No Argument | | | | | | | | - | - |
| CMD1 | 2Ah | 1st | W | Set column start address | SC[9:8] | | | | | | | | 00h | - |
| CMD1 | | 2nd | W | | SC[7:0] | | | | | | | | 00h | - |
| CMD1 | | 3rd | W | | EC[9:8] | | | | | | | | 01h | - |
| CMD1 | | 4th | W | | EC[7:0] | | | | | | | | 8Fh | - |
| CMD1 | 2Bh | 1st | W | Set row start address | SP[9:8] | | | | | | | | 00h | - |
| CMD1 | | 2nd | W | | SP[7:0] | | | | | | | | 00h | - |
| CMD1 | | 3rd | W | | EP[9:8] | | | | | | | | 01h | - |
| CMD1 | | 4th | W | | EP[7:0] | | | | | | | | 8Fh | - |
| CMD1 | 2Ch | - | W | Memory write | No Argument | | | | | | | | - | - |
| CMD1 | 30h | 1st | W | Partial area | SR[9:8] | | | | | | | | 00h | - |
| CMD1 | | 2nd | W | | SR[7:0] | | | | | | | | 00h | - |
| CMD1 | | 3rd | W | | ER[9:8] | | | | | | | | 01h | - |
| CMD1 | | 4th | W | | ER[7:0] | | | | | | | | 8Fh | - |
| CMD1 | 31h | 1st | W | Vertical partial area | PSC[9:8] | | | | | | | | 00h | - |
| CMD1 | | 2nd | W | | PSC[7:0] | | | | | | | | 00h | - |
| CMD1 | | 3rd | W | | PEC[9:8] | | | | | | | | 01h | - |
| CMD1 | | 4th | W | | PEC[7:0] | | | | | | | | 8Fh | - |
| CMD1 | 34h | - | W | Tearing effect line off | No Argument | | | | | | | | - | - |
| CMD1 | 35h | - | W | Tearing effect line on | 0 | 0 | 0 | 0 | 0 | 0 | TE_M | TELOM | 00h | - |
| CMD1 | 36h | - | W | Scan direction control | MADCTR[7:0] | | | | | | | | 00h | - |
| CMD1 | 38h | - | W | Idle mode off | No Argument | | | | | | | | - | - |
| CMD1 | 39h | - | W | Enter idle mode | No Argument | | | | | | | | - | - |
| CMD1 | 3Ah | - | W | Interface Pixel Format | SPI_IFPF_SEL | VIPF2 | VIPF1 | VIPF0 | 0 | IFPF[2] | IFPF[1] | IFPF[0] | 77h | - |
| CMD1 | 3Ch | - | W | Memory Continuous Write | No Argument | | | | | | | | - | - |
| CMD1 | 44h | 1st | W | Set tear scan-line | STS[15:8] | | | | | | | | 00h | - |
| CMD1 | | 2nd | W | | STS[7:0] | | | | | | | | 00h | - |
| CMD1 | 45h | 1st | R | Get scan line | GTS[15:8] | | | | | | | | 00h | - |

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CMD1 | | 2nd | R | | GTS[7:0] | | | | | | | | 00h | - |
| CMD1 | 4Fh | - | W | Deep standby | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DSTB | 00h | - |
| CMD1 | 51h | - | W | Write display brightness | DBV[7:0] | | | | | | | | 00h | - |
| CMD1 | 52h | - | R | Read display brightness | DBV[7:0] | | | | | | | | 00h | - |
| CMD1 | 53h | - | W | Write CTRL display | 0 | 0 | BCTRL | 0 | DD | 0 | 0 | 0 | 28h | - |
| CMD1 | 54h | - | R | Read CTRL display | 0 | 0 | BCTRL | 0 | DD | 0 | 0 | 0 | 28h | - |
| CMD1 | 55h | - | W | Write RAD_ACL function | 0 | 0 | 0 | 0 | 0 | 0 | RAD_ACL[1:0] | | 00h | |
| CMD1 | 56h | - | R | Read RAD_ACL function | 0 | 0 | 0 | 0 | 0 | 0 | RAD_ACL[1:0] | | 00h | |
| CMD1 | 58h | - | W | Set color enhancement | 0 | 0 | 0 | 0 | 0 | SLR_EN | SLR_LEVEL1 | SLR_LEVEL0 | 00h | - |
| CMD1 | 59h | - | R | Read color enhancement | 0 | 0 | 0 | 0 | 0 | SLR_EN | SLR_LEVEL1 | SLR_LEVEL0 | 00h | - |
| CMD1 | 63h | - | W | Write HBM display brightness | DBV_HBM[7:0] | | | | | | | | 00h | |
| CMD1 | 64h | - | R | Read HBM display brightness | DBV_HBM[7:0] | | | | | | | | 00h | |
| CMD1 | 66h | | W | HBM enable | - | - | - | - | - | - | HBM_en | - | 00h | |
| CMD1 | 67h | | W | Deep idle enable | - | - | - | - | - | - | - | DEEP_IDLE_EN | 00h | |
| CMD1 | | 1st | W | COLSET | R_0000[7:0] | | | | | | | | 00h | |
| CMD1 | 70h | 2nd | W | COLSET | G_0000[7:0] | | | | | | | | 00h | |
| CMD1 | | 3rd | W | COLSET | B_0000[7:0] | | | | | | | | 00h | |
| CMD1 | | 1st | W | COLSET | R_0001[7:0] | | | | | | | | 00h | |
| CMD1 | 71h | 2nd | W | COLSET | G_0001[7:0] | | | | | | | | 00h | |
| CMD1 | | 3rd | W | COLSET | B_0001[7:0] | | | | | | | | FFh | |
| CMD1 | | 1st | W | COLSET | R_0010[7:0] | | | | | | | | 00h | |
| CMD1 | 72h | 2nd | W | COLSET | G_0010[7:0] | | | | | | | | FFh | |
| CMD1 | | 3rd | W | COLSET | B_0010[7:0] | | | | | | | | 00h | |
| CMD1 | | 1st | W | COLSET | R_0011[7:0] | | | | | | | | 00h | |
| CMD1 | 73h | 2nd | W | COLSET | G_0011[7:0] | | | | | | | | FFh | |
| CMD1 | | 3rd | W | COLSET | B_0011[7:0] | | | | | | | | FFh | |
| CMD1 | | 1st | W | COLSET | R_0100[7:0] | | | | | | | | FFh | |
| CMD1 | 74h | 2nd | W | COLSET | G_0100[7:0] | | | | | | | | 00h | |
| CMD1 | | 3rd | W | COLSET | B_0100[7:0] | | | | | | | | 00h | |
| CMD1 | | 1st | W | COLSET | R_0101[7:0] | | | | | | | | FFh | |
| CMD1 | 75h | 2nd | W | COLSET | G_0101[7:0] | | | | | | | | 00h | |
| CMD1 | | 3rd | W | COLSET | B_0101[7:0] | | | | | | | | FFh | |
| CMD1 | | 1st | W | COLSET | R_0110[7:0] | | | | | | | | FFh | |
| CMD1 | 76h | 2nd | W | COLSET | G_0110[7:0] | | | | | | | | FFh | |
| CMD1 | | 3rd | W | COLSET | B_0110[7:0] | | | | | | | | 00h | |
| CMD1 | | 1st | W | COLSET | R_0111[7:0] | | | | | | | | FFh | |
| CMD1 | 77h | 2nd | W | COLSET | G_0111[7:0] | | | | | | | | FFh | |
| CMD1 | | 3rd | W | COLSET | B_0111[7:0] | | | | | | | | FFh | |
| CMD1 | | 1st | W | COLSET | R_1000[7:0] | | | | | | | | 00h | |
| CMD1 | 78h | 2nd | W | COLSET | G_1000[7:0] | | | | | | | | 00h | |
| CMD1 | | 3rd | W | COLSET | B_1000[7:0] | | | | | | | | 00h | |
| CMD1 | | 1st | W | COLSET | R_1001[7:0] | | | | | | | | 00h | |
| CMD1 | 79h | 2nd | W | COLSET | G_1001[7:0] | | | | | | | | 00h | |
| CMD1 | | 3rd | W | COLSET | B_1001[7:0] | | | | | | | | FFh | |
| CMD1 | | 1st | W | COLSET | R_1010[7:0] | | | | | | | | 00h | |
| CMD1 | 7Ah | 2nd | W | COLSET | G_1010[7:0] | | | | | | | | FFh | |
| CMD1 | | 3rd | W | COLSET | B_1010[7:0] | | | | | | | | 00h | |
| CMD1 | | 1st | W | COLSET | R_1011[7:0] | | | | | | | | 00h | |
| CMD1 | 7Bh | 2nd | W | COLSET | G_1011[7:0] | | | | | | | | FFh | |
| CMD1 | | 3rd | W | COLSET | B_1011[7:0] | | | | | | | | FFh | |
| CMD1 | | 1st | W | COLSET | R_1100[7:0] | | | | | | | | FFh | |
| CMD1 | 7Ch | 2nd | W | COLSET | G_1100[7:0] | | | | | | | | 00h | |
| CMD1 | | 3rd | W | COLSET | B_1100[7:0] | | | | | | | | 00h | |
| CMD1 | | 1st | W | COLSET | R_1101[7:0] | | | | | | | | FFh | |
| CMD1 | 7Dh | 2nd | W | COLSET | G_1101[7:0] | | | | | | | | 00h | |
| CMD1 | | 3rd | W | COLSET | B_1101[7:0] | | | | | | | | FFh | |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CMD1 | | 1st | W | COLSET | R_1110[7:0] | | | | | | | | FFh | |
| CMD1 | 7Eh | 2nd | W | COLSET | G_1110[7:0] | | | | | | | | FFh | |
| CMD1 | | 3rd | W | COLSET | B_1110[7:0] | | | | | | | | 00h | |
| CMD1 | | 1st | W | COLSET | R_1111[7:0] | | | | | | | | FFh | |
| CMD1 | 7Fh | 2nd | W | COLSET | G_1111[7:0] | | | | | | | | FFh | |
| CMD1 | | 3rd | W | COLSET | B_1111[7:0] | | | | | | | | FFh | |
| CMD1 | 80h | 1st | W | COLOPT | - | RGB111_opt | - | - | RGB4bit_en | gray256_color[2] | gray256_color[1] | gray256_color[0] | 07h | |
| CMD1 | | 1st | R | Read DDB | SID[7:0] | | | | | | | | D0h | - |
| CMD1 | | 2nd | R | | SID[15:8] | | | | | | | | 01h | - |
| CMD1 | A1h | 3rd | R | | MID[7:0] | | | | | | | | 80h | - |
| CMD1 | | 4th | R | | MID[15:8] | | | | | | | | 90h | - |
| CMD1 | | 5th | R | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFh | - |
| CMD1 | | 1st | R | Read DDB Continuous | SID[7:0] | | | | | | | | D0h | - |
| CMD1 | | 2nd | R | | SID[15:8] | | | | | | | | 01h | - |
| CMD1 | A8h | 3rd | R | | MID[7:0] | | | | | | | | 80h | - |
| CMD1 | | 4th | R | | MID[15:8] | | | | | | | | 90h | - |
| CMD1 | | 5th | R | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFh | - |
| CMD1 | AAh | - | R | Read first checksum | FCS[7:0] | | | | | | | | 00h | - |
| CMD1 | AFh | - | R | Read continuous checksum | CCS[7:0] | | | | | | | | 00h | - |
| CMD1 | C2h | | | Set_DSIP Mode | 0 | 0 | 0 | 0 | 0 | 0 | DM1 | DM0 | 00h | - |
| CMD1 | C4h | | | Set_DSPI Mode | SPI_WRAM | 0 | DSPI_CFG1 | DSPI_CFG0 | 0 | 0 | 0 | DSPI_EN | 00h | - |
| CMD1 | DAh | - | R | Read display identification information (the same as 04h) | ID1[7:0] | | | | | | | | 00h | - |
| CMD1 | DBh | - | R | | ID2[7:0] | | | | | | | | 80h | - |
| CMD1 | DCh | - | R | | ID3[7:0] | | | | | | | | 00h | - |
| CMD1 | FEh | - | W | Write CMD mode page | 0 | 0 | 0 | 0 | CMD_Page[3:0] | | | | 00h | - |
| CMD1 | FFh | - | R | Read CMD page Status | 0 | 0 | 0 | 0 | CMD_Status[3:0] | | | | 00h | - |

## 6.2 Command Description

### NOP (0000h)

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 0000h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command is an empty command; it does not have any effect on the display module.<br>X = Don't care. |
| Restriction | None |

### SWRESET(0100h) : Software Reset

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 0100h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) |
| Restriction | Software Reset Command cannot be sent during Sleep Out sequence.<br>Any new command cannot be sent for 10-frame period until the RM69090 enters Sleep-In mode. Do not send any command. |

## RDDID(0400h~0402h) : Read Display ID

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 0400h | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | 00 |
| | 0401h | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | 80 |
| | 0402h | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | 00 |

| | |
|---|---|
| Description | The 1st parameter (ID1): the Module's manufacture ID<br>The 2nd parameter (ID2): the Module/driver version ID<br>The 3rd parameter (ID3): the Module/driver ID<br>Note: Commands RDID1/2/3 (DAh/DBh/DCh) read data correspond to the parameter 1, 2, 3 of command 04h, respectively. |
| Restriction | - |

## RDNUMED(0500h) : Read Number of Errors on DSI

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 0500h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

| | |
|---|---|
| Description | The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below.<br>D[6..0] bits are telling a number of the parity errors.<br>D[7] is set to “1” if there is overflow with D[6..0] bits.<br>D[7..0] bits are set to “0”s (as well as RDDSM(0Eh)’s D0 are set “0” at the same time) after there is sent the first parameter information (= The read function is completed).<br>This command is used for MIPI DSI only. It is no function for others interface operation. |
| Restriction | - |

## RDDPM (0A00h) : Read Display Power Mode

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 0A00h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 08 |

Description

This command indicates the current status of the display as described in the table below:

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | BSTON | Booster Voltage Status | '1'=Booster on,<br>'0'=Booster off |
| D6 | IDMON | Idle Mode On/Off | '1' = Idle Mode On,<br>'0' = Idle Mode Off |
| D5 | PTLON | Partial Mode On/Off | '1' = Partial Mode On,<br>'0' = Partial Mode Off |
| D4 | SLPON | Sleep In/Out | '1' = Sleep Out,<br>'0' = Sleep In |
| D3 | NORON | Display Normal Mode On/Off | '1' = Normal Display,<br>'0' = Partial Display |
| D2 | DISON | Display On/Off | '1' = Display On,<br>'0' = Display Off |
| D1 | Reserved | | 0 |
| D0 | Reserved | | 0 |

## RDDMADCTR (0B00h): Read Display MADCTR

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 0B00h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

Description

This command indicates the current status of the display as described in the table below:

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D6 | MX | Column Address Increment | 0: Increasing in horizontal<br>1: Decreasing in horizontal |
| D3 | RGB | RGB/BGR Order | ‘1’ =BGR, “0”=RGB |
| others | Reserved | - | - |

## RDDCOLMOD (0C00h): Read Display Pixel Format

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 0C00h | SPI_IFPF_SE | VIPF[0] | VIPF[0] | VIPF[0] | 0 | IFPF[2] | IFPF[1] | IFPF[0] | 77 |

**Description**

To return the status of 0x3A00.

This command sets the pixel format for the RGB image data used by the interface.
If SPI_IFPF_SEL(3Ah-B7) = 1: The VIPF[2:0] pixel format used by the SPI interface
If SPI_IFPF_SEL(3Ah-B7) = 0: The IFPF[2:0] pixel format used by the SPI / MCU interface

| Control Interface Color Format | IFPF[2] | IFPF[1] | IFPF[0] |
|---|---|---|---|
| SPI 8 bit/pixel (256 colors); SPI 256 Gray (Support IF: SPI3/SPI4) | 0 | 0 | 1 |
| SPI 8 bit/pixel (256 colors); SPI 3-3-2 (Support IF: SPI3/SPI4) | 0 | 1 | 0 |
| SPI 3 bit/pixel (8 colors); SPI 1-1-1 (Support IF: SPI3/SPI4) | 0 | 1 | 1 |
| 16bit/pixel (65,536 colors) | 1 | 0 | 1 |
| 18bit/pixel (262,144 colors) | 1 | 1 | 0 |
| 24bit/pixel (16.7M colors) | 1 | 1 | 1 |

## RDDIM (0D00h): Read Display Image Mode

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 0D00h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

Description

The display module returns the display image mode status.

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | Reserved | | ‘0’ |
| D6 | Reserved | | ‘0’ |
| D5 | INVON | Inversion On/Off | “1” = Inversion is On,<br>“0” = Inversion is Off |
| D4 | ALLON | All Pixel On | ‘0’ = Normal display<br>‘1’ = White display |
| D3 | ALLOFF | All Pixel Off | ‘0’ = Normal display<br>‘1’ = Black display |
| D2~ D0 | Reserved | | ‘000’ |

## RDDSM (0E00h): Read Display Signal Mode

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 0E00h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

Description

The display module returns the Display Signal Mode.

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | TEON | Tearing Effect Line On/Off | “1” = On, “0” = Off |
| D6 | TELOM | Tearing effect line mode | “0” = mode1,<br>“1” = mode2 |
| D5 | Reserved | | ‘0’ |
| D4 | Reserved | | ‘0’ |
| D3 | Reserved | | ‘0’ |
| D2 | Reserved | | ‘0’ |
| D1 | Reserved | | ‘0’ |
| D0 | Error on DSI | Error on DSI | ‘0’ = No Error<br>‘1’ = Error |

## RDDSDR (0F00h): Read Display Self-Diagnostic Result

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 0F00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | checksum_comp | 00 |

**Description**

The display module returns the self-diagnostic results following a Sleep Out command.

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D0 | Reserved | checksum_comp | ‘0’ |

## SLPIN (1000h): Sleep In

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 1000h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. The control Interface such as registers is still working and keeps its values. |
| Restriction | This command has no effect when the display module is already in Sleep mode.<br>Sleep In Mode can only be exit by the Sleep Out Command (11h).<br>It must wait 5msec before sending next command for the supply voltages and clock circuits to stabilize.<br>It must wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent. |

## SLPOUT (1100h): Sleep Out

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 1100h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to exit Sleep mode. |
| Restriction | This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize.<br>The host processor must wait 60 milliseconds after sending a Sleep Out command before sending a Sleep-In command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received. |

## PTLON (1200h): Partial Display Mode On

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 1200h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h) command.<br>To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written. |
| Restriction | This command has no effect when Partial Display Mode is already active. |

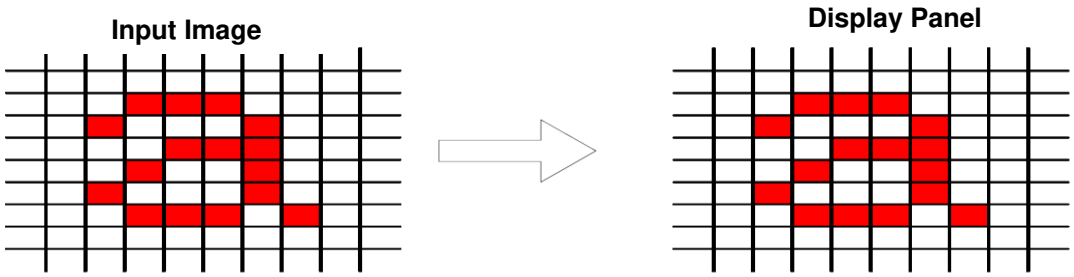
## NORON (1300h): Normal Display Mode On

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 1300h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode. |
| Restriction | This command has no effect when Normal Display mode is already active. |

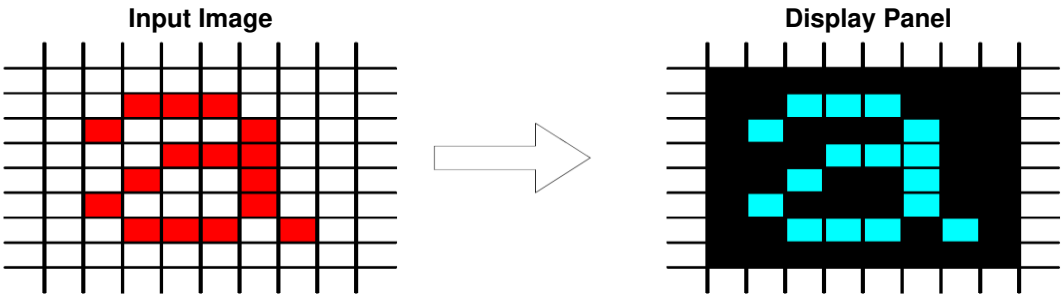
## INVOFF (2000H): Display Inversion Off

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 2000h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to stop inverting the image data on the display device. No status bits are changed.<br>  |
| Restriction | This command has no effect when the display module is not inverting the display image. |

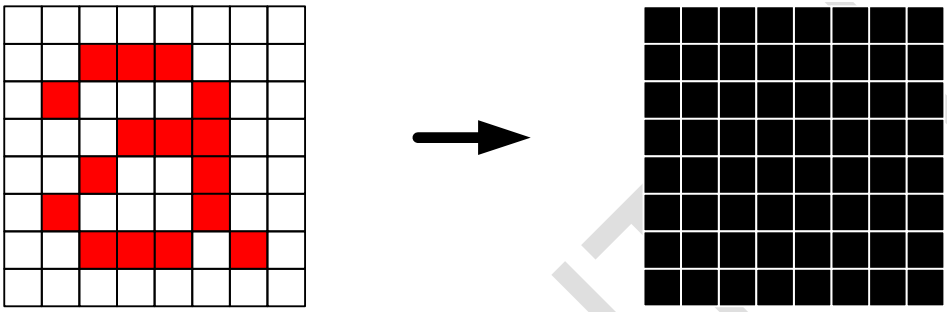
## INVON (2100H): Display Inversion On

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 2100h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to invert the image data only on the display device. No status bits are changed.<br>  |
| Restriction | This command has no effect when module is already in inversion on mode. |

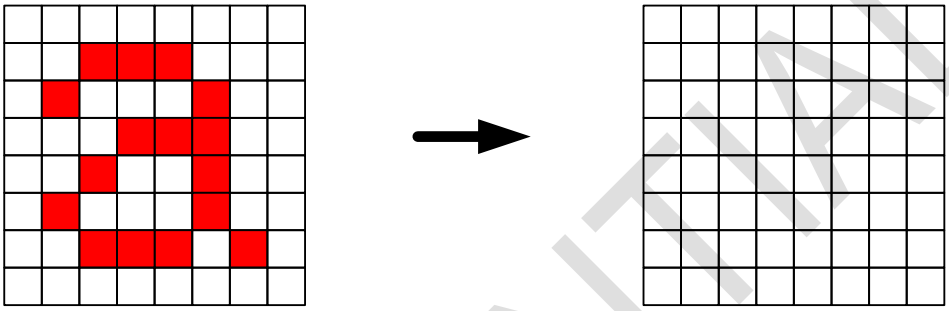
## ALLPOFF (2200H): All Pixel Off

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 2200h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off.<br>This command does not change any other status.<br>**Input Image** **Display Panel**<br>  <br>"All Pixels On", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the Input Image after "Normal Display On" and "Partial Mode On" commands. |
| Restriction | - |

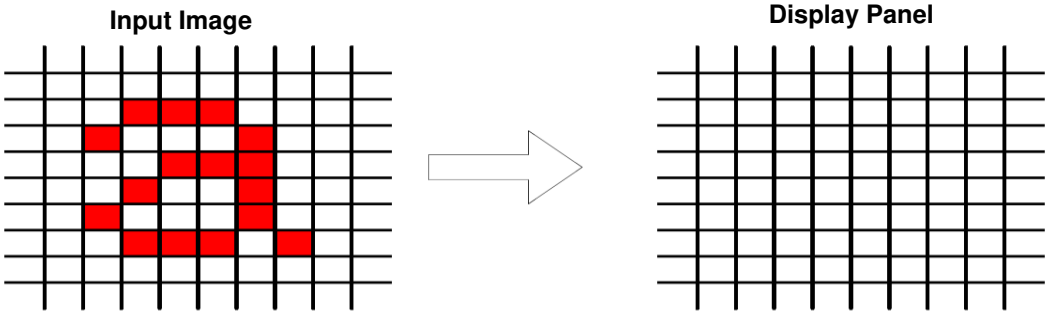
## ALLPON (2300H): All Pixel On

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 2300h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.<br>This command does not change any other status.<br>**Input Image** **Display Panel**<br>  <br>"All Pixels Off", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the Input Image after "Normal Display On" and "Partial Mode On" commands. |
| Restriction | - |

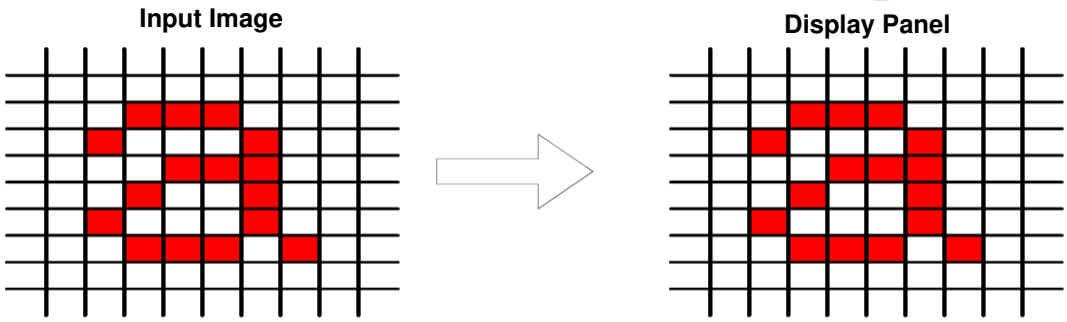
## DISPOFF (2800h): Display Off

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 2800h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to stop displaying the image data on the display device. No status bits are changed.<br>  |
| Restriction | This command has no effect when module is already in display off mode. |

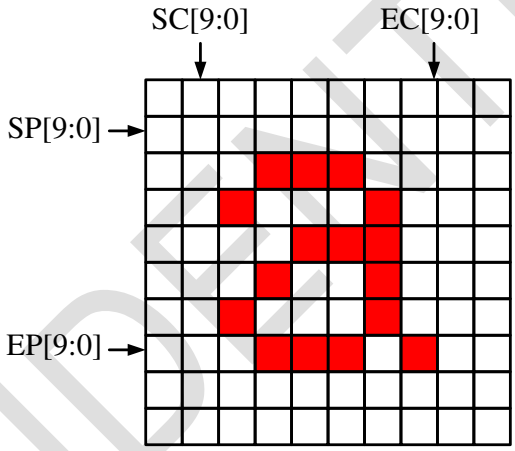
## DISPON (2900h): Display On

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 2900h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to start displaying the image data on the display device. No status bits are changed.<br>  |
| Restriction | This command has no effect when module is already in display on mode. |

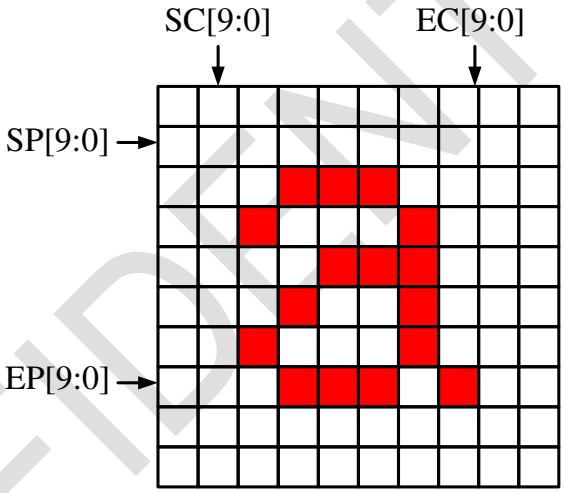
## CASET(2A00h~2A03h) : Set Column Start Address

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 2A00h | - | - | - | - | - | - | SC9 | SC8 | 00 |
| | 2A01h | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 | 00 |
| | 2A02h | - | - | - | - | - | - | EC9 | EC8 | 01 |
| | 2A03h | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 | 8F |

| | |
|---|---|
| Description | This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands.<br>This command makes no change on the other driver status. The values of SC[9:0] and EC[9:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.<br>  <br> |
| Restriction | (1) SC[9:0] always must be equal to or less than EC[9:0].<br>(2) The SC[9:0] and EC[9:0]-SC[9:0]+1 must can be divisible by 2. |

## RASET(2B00h~2B03h) : Set Row Start Address

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 2B00h | - | - | - | - | - | - | SP9 | SP8 | 00 |
| | 2B01h | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 00 |
| | 2B02h | - | - | - | - | - | - | EP9 | EP8 | 01 |
| | 2B03h | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 | 8F |

| | |
|---|---|
| Description | This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command.<br>This command makes no change on theother driver status. The values of SP[9:0] and EP[9:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.<br>  <br> |
| Restriction | (1) SP[9:0] always must be equal to or less than EP[9:0]<br>(2) The SP[9:0] and EP[9:0]-SP[9:0]+1 must can be divisible by 2. |

## RAMWR (2C00h): Memory Write

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 2C00h | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C |
| | 1st Pixel | $D_1$7 | $D_1$6 | $D_1$5 | $D_1$4 | $D_1$3 | $D_1$2 | $D_1$1 | $D_1$0 | |
| | : | : | : | : | : | : | : | : | : | |
| | Nth Pixel | $D_N$7 | $D_N$6 | $D_N$5 | $D_N$4 | $D_N$3 | $D_N$2 | $D_N$1 | $D_N$0 | |

| | |
|---|---|
| Description | This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. |
| Restriction | A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations. |

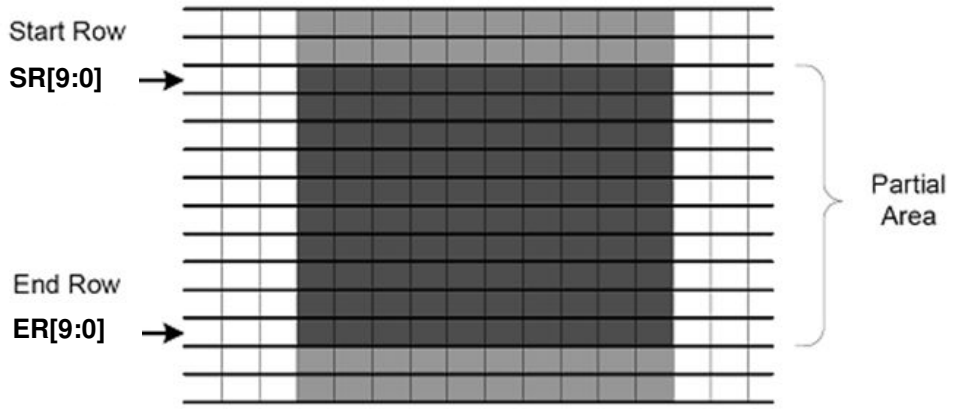
## PTLAR (3000h): Partial Area

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 3000h | - | - | - | - | - | - | SR9 | SR8 | 00 |
| | 3001h | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | 00 |
| | 3002h | - | - | - | - | - | - | ER9 | ER8 | 01 |
| | 3003h | ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 | 8F |

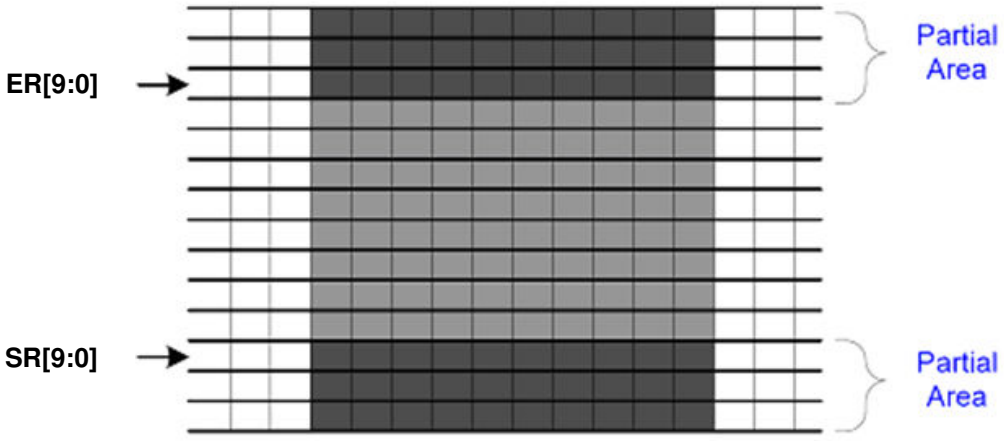
**Description**

This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure.

If End Row > Start Row




If End Row < Start Row




If End Row = Start Row then the Partial Area will be one row deep.

**Restriction**

SR[9:0] and ER[9:0] settings should be within max available Display Area.

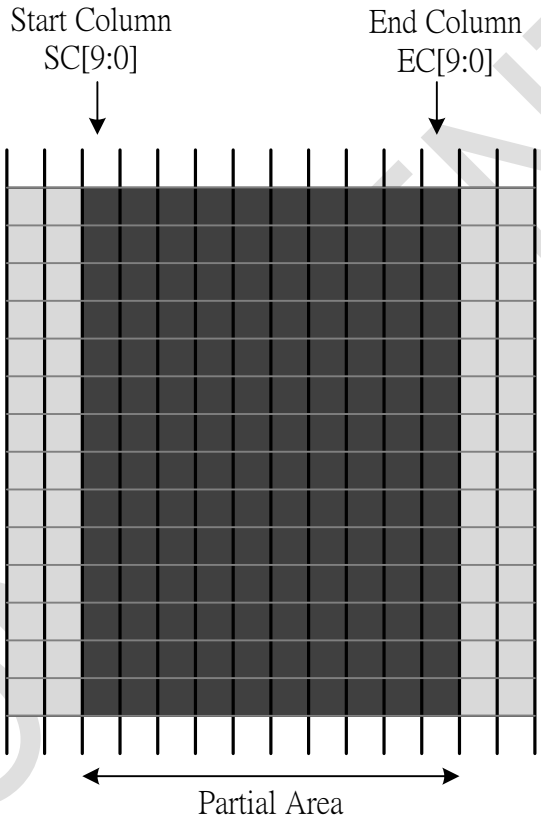
## PTLAR (3100h): Vertical Partial Area

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 3100h | - | - | - | - | - | - | - | SC8 | 00 |
| | 3101h | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 | 00 |
| | 3102h | - | - | - | - | - | - | - | EC8 | 01 |
| | 3103h | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 | 8F |

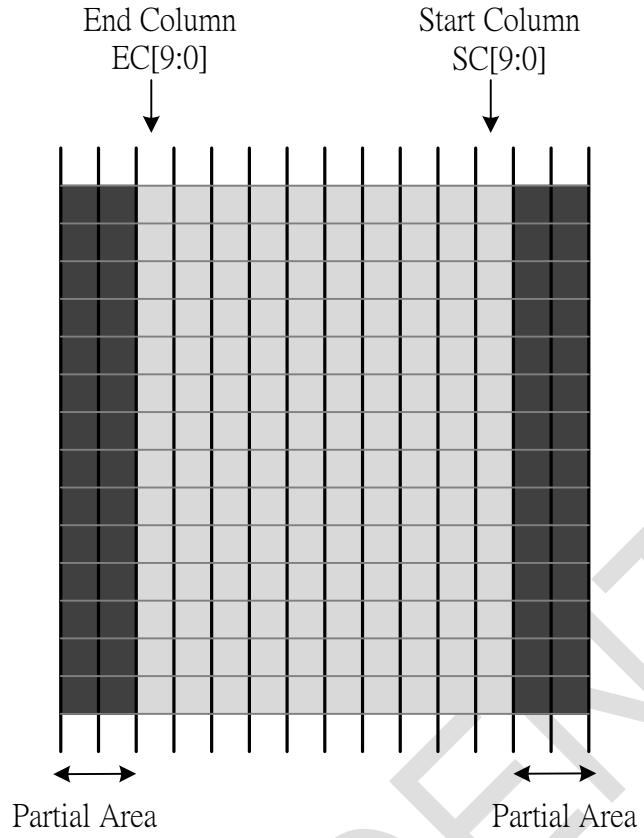
Description

This command defines the Vertical Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Column (SC) and the second the End Column (EC), as illustrated in the following figure.

If End Column > Start Column




If End Column < Start Column

| | |
|---|---|
| |  <br>If End Column = Start Column then the Partial Area will be one column deep. |
| Restriction | SC[9:0] and EC[9:0] settings should be within max available Display Area. |

## TEOFF (3400h): Tearing Effect Line OFF

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 3400h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command turns off the display module's Tearing Effect output signal on the TE signal line. |
| Restriction | This command has no effect when the Tearing Effect output is already off. |

## TEON (3500h): Tearing Effect Line ON

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 3500h | 0 | 0 | 0 | 0 | 0 | 0] | TE_M | TELOM | 00 |

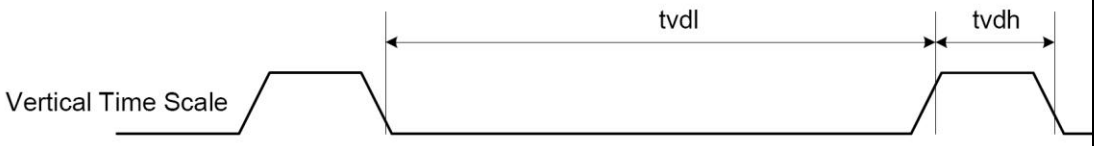
**Description**

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D1 | TE_M | Output mode of TE signal set | 1: Refresh frame active<br><br><Note><br>TE output active at refresh frame to avoid tearing effect, command can be set:<br>1. 0x3500=00.or<br>2. 0x3500=02. |
| D0 | TELOM | Output mode of TE signal | 0:only V-blanking<br>1:V-blanking +H-blanking |

This command turns on the tearing Effect output signal on the TE signal line.
The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

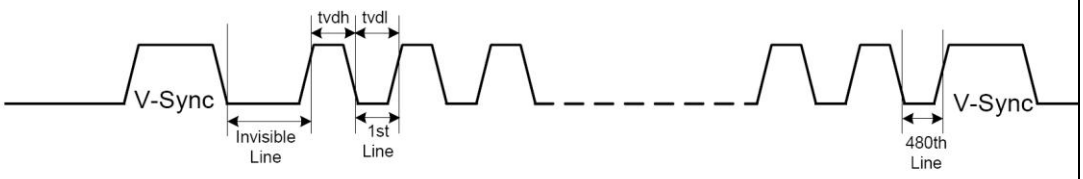
If TELOM = 0:

The Tearing Effect Output line consists of V-Blanking information only.




If TELOM = 1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.




***The Tearing Effect Output line shall be active low when the display module is in Sleep mode.***

**Restriction**

This command has no effect when Tearing Effect output is already ON.

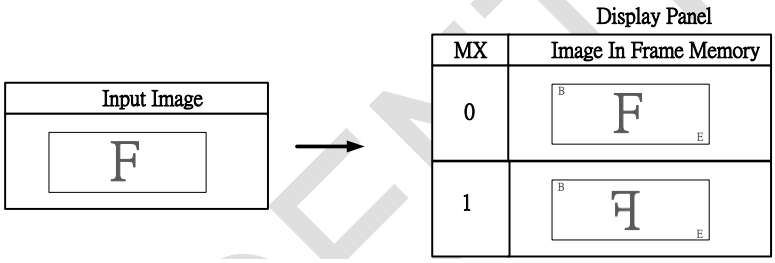
## MADCTR (3600h): Scan Direction Control

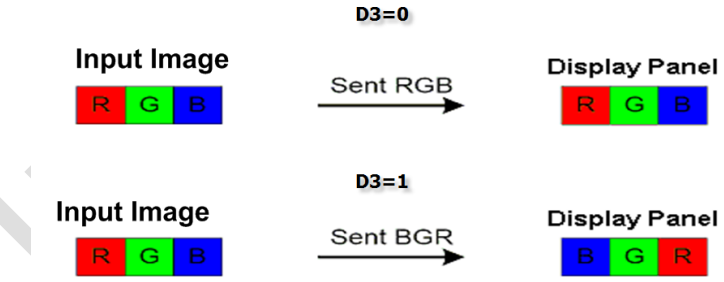
| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 3600h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

**Description**

This command defines the scan direction of Source and Gate Driver. This command makes no change on the other driver status.

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | Reserved | | |
| D6 | MX | Column Address Increment | 0: Increasing in horizontal<br>1: Decreasing in horizontal |
| D3 | RGB | RGB/BGR Order | '1' =BGR, "0"=RGB |
| D2 | Reserved | | |
| D1 | Reserved | | |
| D0 | Reserved | | |







**Restriction**

## IDMOFF (3800h): Idle Mode Off

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 3800h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to exit Idle mode. |
| Restriction | This command has no effect when the display module is not in Idle mode. |

## IDMON (3900h): Enter_idle_mode

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 3900h | No Argument | | | | | | | | |

| | |
|---|---|
| Description | This command causes the display module to enter Idle Mode. |
| Restriction | This command has no effect when module is already in idle on mode. |

## COLMOD (3A00h): Interface Pixel Format

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 3A00h | SPI_IFPF_SEL | VIPF[2] | VIPF[1] | VIPF[0] | 0 | IFPF[2] | IFPF[1] | IFPF[0] | 77 |

**Description**

This command sets the pixel format for the RGB image data used by the interface.
The IFPF[2:0] pixel format used by the MIPI/ MCU interface.
If SPI_IFPF_SEL(3Ah-D7) = 1: The VIPF[2:0] pixel format used by the SPI interface
If SPI_IFPF_SEL(3Ah-D7) = 0: The IFPF[2:0] pixel format used by the SPI interface

| Control Interface Color Format | IFPF[2] | IFPF[1] | IFPF[0] |
|---|---|---|---|
| SPI 8 bit/pixel (256 colors); SPI 256 Gray (Support IF: SPI3/SPI4) | 0 | 0 | 1 |
| SPI 8 bit/pixel (256 colors); SPI 3-3-2 (Support IF: SPI3/SPI4) | 0 | 1 | 0 |
| SPI 3 bit/pixel (8 colors); SPI 1-1-1 (Support IF: SPI3/SPI4) | 0 | 1 | 1 |
| 16bit/pixel (65,536 colors) | 1 | 0 | 1 |
| 18bit/pixel (262,144 colors) | 1 | 1 | 0 |
| 24bit/pixel (16.7M colors) | 1 | 1 | 1 |

SPI 1-1-1

| RGB 1-1-1 Bit | DCX | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| CMDWR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x2C for GRAM Write |
| 1st RAM Data Write | 1 | X | X | R1[0] | G1[0] | B1[0] | R2[0] | G2[0] | B2[0] | 1,2 pixel Data Write |
| 2nd RAM Data Write | 1 | X | X | R3[0] | G3[0] | B3[0] | R4[0] | G4[0] | B4[0] | 3,4 pixel Data Write |
| 3rd RAM Data Write | 1 | X | X | R5[0] | G5[0] | B5[0] | R6[0] | G6[0] | B6[0] | 5,6 pixel Data Write |
| So on... | | | | | | | | | | |

SPI 3-3-2

| RGB 3-3-2 Bit | DCX | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| CMDWR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x2C for GRAM Write |
| 1st RAM Data Write | 1 | R1[2] | R1[1] | R1[0] | G1[2] | G1[1] | G1[0] | B1[1] | B1[0] | 1st pixel Data Write |
| 2nd RAM Data Write | 1 | R2[2] | R2[1] | R2[0] | G2[2] | G2[1] | G2[0] | B2[1] | B2[0] | 2nd pixel Data Write |
| 3rd RAM Data Write | 1 | R3[2] | R3[1] | R3[0] | G3[2] | G3[1] | G3[0] | B3[1] | B3[0] | 3rd pixel Data Write |
| So on... | | | | | | | | | | |

SPI 256 Gray

| RGB 256 Gray | DCX | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| CMDWR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x2C for GRAM Write |
| 1st RAM Data Write | 1 | P1[7] | P1[6] | P1[5] | P1[4] | P1[3] | P1[2] | P1[1] | P1[0] | 1st pixel Data Write |
| 2nd RAM Data Write | 1 | P2[7] | P2[6] | P2[5] | P2[4] | P2[3] | P2[2] | P2[1] | P2[0] | 2nd pixel Data Write |
| 3rd RAM Data Write | 1 | P3[7] | P3[6] | P3[5] | P3[4] | P3[3] | P3[2] | P3[1] | P3[0] | 3rd pixel Data Write |
| So on... | | | | | | | | | | |

**Restriction**

-

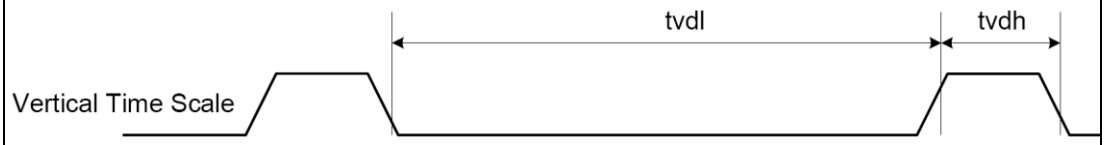
## RAMWRC (3C00h): Memory Continuous Write

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 3C00h | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3C |
| | 1st Pixel | $D_1$7 | $D_1$6 | $D_1$5 | $D_1$4 | $D_1$3 | $D_1$2 | $D_1$1 | $D_1$0 | |
| | : | : | : | : | : | : | : | : | : | |
| | Nth Pixel | $D_N$7 | $D_N$6 | $D_N$5 | $D_N$4 | $D_N$3 | $D_N$2 | $D_N$1 | $D_N$0 | |

| | |
|---|---|
| Description | This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. |
| Restriction | A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations. |

## STESL(4400h) : Set_Tear_Scanline

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 4400h | STS[15] | STS[14] | STS[13] | STS[12] | STS[11] | STS[10] | STS[9] | STS[8] | 00 |
| | 4401h | STS[7] | STS[6] | STS[5] | STS[4] | STS[3] | STS[2] | STS[1] | STS[0] | 00 |

| | |
|---|---|
| Description | This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.<br>  <br>The Tearing Effect Output line shall be active low when the display module is in Sleep mode. |
| Restriction | |

## GSL (4500h) : Get_Scanline

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 4500h | GTS[15] | GTS[14] | GTS[13] | GTS[12] | GTS[11] | GTS[10] | GTS[9] | GTS[8] | 0x |
| | 4501h | GTS[7] | GTS[6] | GTS[5] | GTS[4] | GTS[3] | GTS[2] | GTS[1] | GTS[0] | xx |

| | |
|---|---|
| Description | The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.<br>When in Sleep Mode, the value returned by get scanline is undefined. |
| Restriction | - |

## DSTBON (4F00h): Deep Standby Mode On

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 4F00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DSTB | 00 |

| | |
|---|---|
| Description | This command is used to enter deep standby mode.<br>DSTB=”1”, enter deep standby mode.<br>Notes:<br>1. To exit Deep Standby Mode, input low pulse more than 3 msec to pin RESX.<br>2. For MIPI IF, if deep standby mode is used, please pull HSSI_CLK_P/N & HSSI_D0~D1_P/N to GND after executing deep standby command. |
| Restriction | - |

## WRDISBV (5100h): Write Display Brightness

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 5100h | DBV7 | DBV6 | DBV5 | DBV4 | DBV3 | DBV2 | DBV1 | DBV0 | 00 |

| | |
|---|---|
| Description | This command is used to adjust brightness value.<br>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. |
| Restriction | The display supplier cannot use this command for tuning |

**RDDISBV (5200h): Read Display Brightness**

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 5200h | DBV7 | DBV6 | DBV5 | DBV4 | DBV3 | DBV2 | DBV1 | DBV0 | 00 |

| | |
|---|---|
| Description | This command returns brightness value.<br>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. |
| Restriction | - |

## WRCTRLD (5300h): Write Display Control

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 5300h | 0 | 0 | BCTRL | 0 | DD | 0 | 0 | 0 | 28 |

| | |
|---|---|
| Description | BCTRL: Brightness control ,1=enable<br>DD: Display dimming control ,1=enable |
| Restriction | The display supplier cannot use this command for tuning |

## RDCTRLD (5400h): Read Display Control

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 5400h | 0 | 0 | BCTRL | 0 | DD | 0 | 0 | 0 | 28 |

| | |
|---|---|
| Description | BCTRL: Brightness control ,1=enable<br>DD: Display dimming control ,1=enable |
| Restriction | - |

## WRRADACL (5500h): RAD_ACL Control

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 5500h | 0 | 0 | 0 | 0 | 0 | 0 | RAD_ACL[1:0] | | 00 |

| | |
|---|---|
| Description | This command is used to control Raydium specific function for ACL (Auto Current Limit)<br>RAD_ACL[1:0]=11, Enable Raydium ACL function.<br>RAD_ACL[1:0]=00, Disable Raydium ACL function. |
| Restriction | - |

## IMGEHCCTR (5800h) : Set_color_enhance

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 5800h | 0 | 0 | 0 | 0 | 0 | SLR_EN | SLR_LEVEL 1 | SLR_LEVEL 0 | 00 |

Description

| Bit | Description | Value |
|---|---|---|
| SLR_EN | Sunlight Readable Enhancement Enable | '0' : disable;<br>'1': enable |
| SLR_LEVEL[1:0] | Sunlight Readable Enhancement Level | 0~2, low to high |

Restriction: -

## IMGEHCCTR (5900h) : Read_color_enhance

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 5900h | 0 | 0 | 0 | 0 | 0 | SLR_EN | SLR_LEVEL1 | SLR_LEVEL0 | 00 |

| | |
|---|---|
| Description | <table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>SLR_EN</td><td>Sunlight Readable Enhancement Enable</td><td>‘0’ : disable;<br>‘1’: enable</td></tr><tr><td>SLR_LEVEL[1:0]</td><td>Sunlight Readable Enhancement Level</td><td>0~2, low to high</td></tr></table> |
| Restriction | - |

## WRDISBV (6300h): Write HBM Display Brightness

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 6300h | DBV_HBM[7:0] | | | | | | | | 00 |

| | |
|---|---|
| Description | This command is used to adjust brightness value in HBM mode if hbm_gidx_type=1.(0xC840h) |
| Restriction | 1. The display supplier cannot use this command for tuning<br>2. DBV_HBM[7:0] setting value must be greater than G_ratio_to2 (0xAC60h )/ G_ratio_to3 (0x5530h ) value. |

## RDDISBV (6400h): Read HBM Display Brightness

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | 6400h | DBV_HBM[7:0] | | | | | | | | 00 |

| | |
|---|---|
| Description | This command returns brightness value in HBM mode. |
| Restriction | - |

## HBM_Mode (6600h) : Set_HBM_Mode

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 6600h | 0 | 0 | 0 | 0 | 0 | 0 | HBM_en | 0 | 00 |

| | |
|---|---|
| Description | HBM_en = 1, This command causes the display module to enter HBM mode (exit normal, idle and<br>deep idle)<br><br>HBM_en = 0, This command causes the display module to exit HBM mode (to normal mode) |
| Restriction | under display area |

## Deep_Idle_Mode (6700h) : Set_Deep Idle Mode

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 6700h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DEEP_IDLE_EN | 00 |

| | |
|---|---|
| Description | Deep_Idle_en = 1, This command causes the display module to enter deep idle mode (exit normal, idle and HBM)<br><br>Deep_Idle_en = 0, This command causes the display module to exit deep idle mode (to idle mode) |
| Restriction | under display area |

## COLSET (7000~7F00h): Interface Pixel Format Set

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 7000h | R_0000[7:0] | | | | | | | | 00 |
| | 7001h | G_0000[7:0] | | | | | | | | 00 |
| | 7002h | B_0000[7:0] | | | | | | | | 00 |
| W | 7100h | R_0001[7:0] | | | | | | | | 00 |
| | 7101h | G_0001[7:0] | | | | | | | | 00 |
| | 7102h | B_0001[7:0] | | | | | | | | FF |
| W | 7200h | R_0010[7:0] | | | | | | | | 00 |
| | 7201h | G_0010[7:0] | | | | | | | | FF |
| | 7202h | B_0010[7:0] | | | | | | | | 00 |
| W | 7300h | R_0011[7:0] | | | | | | | | 00 |
| | 7301h | G_0011[7:0] | | | | | | | | FF |
| | 7302h | B_0011[7:0] | | | | | | | | FF |
| W | 7400h | R_0100[7:0] | | | | | | | | FF |
| | 7401h | G_0100[7:0] | | | | | | | | 00 |
| | 7402h | B_0100[7:0] | | | | | | | | 00 |
| W | 7500h | R_0101[7:0] | | | | | | | | FF |
| | 7501h | G_0101[7:0] | | | | | | | | 00 |
| | 7502h | B_0101[7:0] | | | | | | | | FF |
| W | 7600h | R_0110[7:0] | | | | | | | | FF |
| | 7601h | G_0110[7:0] | | | | | | | | FF |
| | 7602h | B_0110[7:0] | | | | | | | | 00 |
| W | 7700h | R_0111[7:0] | | | | | | | | FF |
| | 7701h | G_0111[7:0] | | | | | | | | FF |
| | 7702h | B_0111[7:0] | | | | | | | | FF |
| W | 7800h | R_1000[7:0] | | | | | | | | 00 |
| | 7801h | G_1000[7:0] | | | | | | | | 00 |
| | 7802h | B_1000[7:0] | | | | | | | | 00 |
| W | 7900h | R_1001[7:0] | | | | | | | | 00 |
| | 7901h | G_1001[7:0] | | | | | | | | 00 |
| | 7902h | B_1001[7:0] | | | | | | | | FF |
| W | 7A00h | R_1010[7:0] | | | | | | | | 00 |
| | 7A01h | G_1010[7:0] | | | | | | | | FF |
| | 7A02h | B_1010[7:0] | | | | | | | | 00 |
| W | 7B00h | R_1011[7:0] | | | | | | | | 00 |
| | 7B01h | G_1011[7:0] | | | | | | | | FF |
| | 7B02h | B_1011[7:0] | | | | | | | | FF |
| W | 7C00h | R_1100[7:0] | | | | | | | | FF |
| | 7C01h | G_1100[7:0] | | | | | | | | 00 |
| | 7C02h | B_1100[7:0] | | | | | | | | 00 |
| W | 7D00h | R_1101[7:0] | | | | | | | | FF |
| | 7D01h | G_1101[7:0] | | | | | | | | 00 |
| | 7D02h | B_1101[7:0] | | | | | | | | FF |
| W | 7E00h | R_1110[7:0] | | | | | | | | FF |

| | | | |
|---|---|---|---|
| | 7E01h | G_1110[7:0] | FF |
| | 7E02h | B_1110[7:0] | 00 |
| W | 7F00h | R_1111[7:0] | FF |
| | 7F01h | G_1111[7:0] | FF |
| | 7F02h | B_1111[7:0] | FF |

Description

This command set the 1-1-1 color format map directly to 24 bits by CMD 7000h-7F00h

| RGB111 color mapping | R[7:0] | G[7:0] | B[7:0] |
|---|---|---|---|
| 0000 (70h) | R_0000[7:0] | G_0000[7:0] | B_0000[7:0] |
| 0001 (71h) | R_0001[7:0] | G_0001[7:0] | B_0001[7:0] |
| 0010 (72h) | R_0010[7:0] | G_0010[7:0] | B_0010[7:0] |
| 0011 (73h) | R_0011[7:0] | G_0011[7:0] | B_0011[7:0] |
| 0100 (74h) | R_0100[7:0] | G_0100[7:0] | B_0100[7:0] |
| 0101 (75h) | R_0101[7:0] | G_0101[7:0] | B_0101[7:0] |
| 0110 (76h) | R_0110[7:0] | G_0110[7:0] | B_0110[7:0] |
| 0111 (77h) | R_0111[7:0] | G_0111[7:0] | B_0111[7:0] |
| 1000 (78h) | R_1000[7:0] | G_1000[7:0] | B_1000[7:0] |
| 1001 (79h) | R_1001[7:0] | G_1001[7:0] | B_1001[7:0] |
| 1010 (7Ah) | R_1010[7:0] | G_1010[7:0] | B_1010[7:0] |
| 1011 (7Bh) | R_1011[7:0] | G_1011[7:0] | B_1011[7:0] |
| 1100 (7Ch) | R_1100[7:0] | G_1100[7:0] | B_1100[7:0] |
| 1101 (7Dh) | R_1101[7:0] | G_1101[7:0] | B_1101[7:0] |
| 1110 (7Eh) | R_1110[7:0] | G_1110[7:0] | B_1110[7:0] |
| 1111 (7Fh) | R_1111[7:0] | G_1111[7:0] | B_1111[7:0] |

Restriction

## COLOPT (8000h): Interface Pixel Format Option

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | 8000h | x | RGB111_opt | x | x | RGB4bit_en | gray256_color[2] | gray256_color[1] | gray256_color[0] | 07 |

Description

This command sets the 1-1-1/256 gray color format option used by SPI interface.

RGB111_opt = 0 (80h-B6):
Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).

| RGB 1-1-1 Bit | DCX | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| CMDWR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x2C for GRAM Write |
| 1st RAM Data Write | 1 | X | X | R1[0] | G1[0] | B1[0] | R2[0] | G2[0] | B2[0] | 1,2 pixel Data Write |
| 2nd RAM Data Write | 1 | X | X | R3[0] | G3[0] | B3[0] | R4[0] | G4[0] | B4[0] | 3,4 pixel Data Write |
| 3rd RAM Data Write | 1 | X | X | R5[0] | G5[0] | B5[0] | R6[0] | G6[0] | B6[0] | 5,6 pixel Data Write |
| So on... | | | | | | | | | | |

RGB111_opt = 1 (80h-B6):
Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).

| RGB 1-1-1 Bit | DCX | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| CMDWR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x2C for GRAM Write |
| 1st RAM Data Write | 1 | x | R1[0] | G1[0] | B1[0] | x | R2[0] | G2[0] | B2[0] | 1,2 Pixel Data Write |
| 2nd RAM Data Write | 1 | x | R3[0] | G3[0] | B3[0] | x | R4[0] | G4[0] | B4[0] | 3,4 Pixel Data Write |
| 3rd RAM Data Write | 1 | x | R5[0] | G5[0] | B5[0] | x | R6[0] | G6[0] | B6[0] | 5,6 Pixel Data Write |
| So on… | | | | | | | | | | |

RGB4bit_en = 0 (80h-B3):
Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).
Three bits per pixel formats map directly to 24bits by CMD 7000h-7700h

| RGB 1-1-1 Bit | DCX | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| CMDWR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x2C for GRAM Write |
| 1st RAM Data Write | 1 | x | x | P1[2] | P1[1] | P1[0] | P2[2] | P2[1] | P2[0] | 1,2 Pixel Data Write |
| 2nd RAM Data Write | 1 | x | x | P3[2] | P3[1] | P3[0] | P4[2] | P4[1] | P4[0] | 3,4 Pixel Data Write |
| 3rd RAM Data Write | 1 | x | x | P5[2] | P5[1] | P5[0] | P6[2] | P6[1] | P6[0] | 5,6 Pixel Data Write |
| So on… | | | | | | | | | | |

Example:
P1[2:0] = 3'b101 = { R_0101[7:0], G_0101[7:0], B_0101[7:0] } CMD 7500h-7502h

Description

RGB4bit_en = 1(80h-B3):
Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).
Four bits per pixel formats map directly to 24bits by CMD 7000h-7F00h

| RGB 1-1-1 Bit | DCX | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| CMDWR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x2C for GRAM Write |
| 1st RAM Data Write | 1 | P1[3] | P1[2] | P1[1] | P1[0] | P2[3] | P2[2] | P2[1] | P2[0] | 1,2 Pixel Data Write |
| 2nd RAM Data Write | 1 | P3[3] | P3[2] | P3[1] | P3[0] | P4[3] | P4[2] | P4[1] | P4[0] | 3,4 Pixel Data Write |
| 3rd RAM Data Write | 1 | P5[3] | P5[2] | P5[1] | P5[0] | P6[3] | P6[2] | P6[1] | P6[0] | 5,6 Pixel Data Write |
| So on… | | | | | | | | | | |

Example:
P1[3:0] = 4'b1101 = { R_1101[7:0], G_1101[7:0], B_1101[7:0] } CMD 7D00h-7D02h

gray256_color(80h-B[2:0]):
Supporting in IFPF[2:0]=001 case setting by 3A00h (interface pixel format is SPI 256 Gray).
This command sets the valid red, green and blue 256 grayscale

| gray256_color[2:0] | Red grayscale | Green grayscale | Blue grayscale |
|---|---|---|---|
| 000 | 00000000 | 00000000 | 00000000 |
| 001 | 00000000 | 00000000 | P[7:0] |
| 010 | 00000000 | P[7:0] | 00000000 |
| 011 | 00000000 | P[7:0] | P[7:0] |
| 100 | P[7:0] | 00000000 | 00000000 |
| 101 | P[7:0] | 00000000 | P[7:0] |
| 110 | P[7:0] | P[7:0] | 00000000 |
| 111 | P[7:0] | P[7:0] | P[7:0] |

Restriction

-

## RDDDBS(A100h) : Read_DDB_Start

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | A100h | SID[7] | SID [6] | SID [5] | SID [4] | SID [3] | SID [2] | SID [1] | SID [0] | D0 |
| | A101h | SID[15] | SID[14] | SID[13] | SID[12] | SID[11] | SID[10] | SID[9] | SID[8] | 01 |
| | A102h | MID[7] | MID[6] | MID[5] | MID[4] | MID[3] | MID[2] | MID[1] | MID[0] | 80 |
| | A103h | MID[15] | MID[14] | MID[13] | MID[12] | MID[11] | MID[10] | MID[9] | MID[8] | 90 |
| | A104h | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |

| | |
|---|---|
| Description | 1st parameter: Supplier ID code<br>2nd parameter: Supplier ID code<br>3rd parameter: Module ID<br>4th parameter: Module ID<br>5th Exit code (FFh). |
| Restriction | |

## RDDDBC(A800h) : Read DDB Continous

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | A800h | SID[7] | SID [6] | SID [5] | SID [4] | SID [3] | SID [2] | SID [1] | SID [0] | D0 |
| | A801h | SID[15] | SID[14] | SID[13] | SID[12] | SID[11] | SID[10] | SID[9] | SID[8] | 01 |
| | A802h | MID[7] | MID[6] | MID[5] | MID[4] | MID[3] | MID[2] | MID[1] | MID[0] | 80 |
| | A803h | MID[15] | MID[14] | MID[13] | MID[12] | MID[11] | MID[10] | MID[9] | MID[8] | 90 |
| | A804h | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |

| | |
|---|---|
| Description | This command returns the supplier identification and display module mode/revision information from the<br>point where RDDDBS command was interrupted by an other command.<br>*Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.*<br>*Note: For use example,*<br>*1. Set maximum return packet size=3*<br>*2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0]*<br>*3. Read* 0xA8*, return 2 bytes MID[15:8],RID[7:0], RID[15:8] and 0xFF* |
| Restriction | A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue<br>command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue c ommnd is undefined. |

## RDFCS(AA00h) : Read First Checksum

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | AA00h | FCS7 | FCS6 | FCS5 | FCS4 | FCS3 | FCS2 | FCS1 | FCS0 | 00 |

| | |
|---|---|
| Description | This command returns the first checksum what has been calculated from “User Command Set” area<br>registers (not include “Manufacture Command Set) and the frame memory after the write access to those<br>registers and/or frame memory has been done. |
| Restriction | It will be necessary to wait 150ms after there is the last write access on “User Command Set” area<br>registers before there can read this checksum value. |

## RDCCS(AF00h) : Read Continue Checksum

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | AF00h | CCS7 | CCS6 | CCS5 | CCS4 | CCS3 | CCS2 | CCS1 | CCS0 | 00 |

| | |
|---|---|
| Description | This command returns the continue checksum what has been calculated continuously after the first<br>checksum has calculated from “User Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done. |
| Restriction | It will be necessary to wait 300ms after there is the last write access on “User Command Set” area registers before there can read this checksum value in the first time. |

## SetDISPMode (C200h) : set_DISP Mode

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | C200h | 0 | 0 | 0 | 0 | 0 | 0 | DM1 | DM0 | 00 |

**Description**

| Bit | Description | Value |
|---|---|---|
| DM[1:0] | Display timing mode selection | 2'b00: internal timing<br>2'b01: reserved<br>2'b10: reserved<br>2'b11: external timing (VSYNC + HSYNC align mode) |

**Restriction**

Note:
(1) If video mode, need to set DM[1:0] = 2'b11.
(2) System video mode parameter V-total and H-total setting has restriction, it must match driver IC V-total and H-total setting.
Related video mode parameter settings suggest asking Raydium.

## SetDSPIMode (C400h) : set_DSPI Mode

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | C400h | SPI_WRAM | 0 | DSPI_CFG 1 | DSPI_CFG 0 | 0 | 0 | 0 | DSPI_EN | 00 |

**Description**

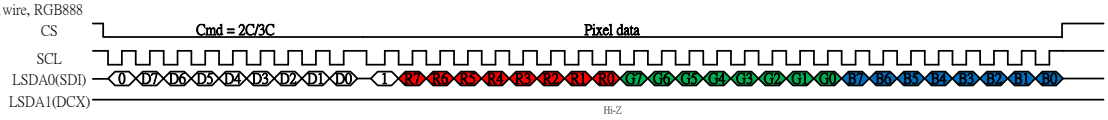
| Bit | Description | Value |
|---|---|---|
| DSPI_EN | DAUL SPI MODE Enable | 0: disable<br>1: enable |
| DSPI_CFG[1:0] | DAUL SPI MODE Selection | 00: 1P1T for 1 wire<br>10: 1P1T for 2 wire<br>11: 2P3T for 2 wire<br>01: reserved |
| SPI_WRAM | This command is used in SPI/SPINK interfaces.<br>Making sure to set SPI_WRAM=1 before host writes SRAM via SPI/SPINK interfaces. | 0: disable<br>1: SPI interface write RAM enable |

Note: detailed DAUL SPI formats are described at next page.

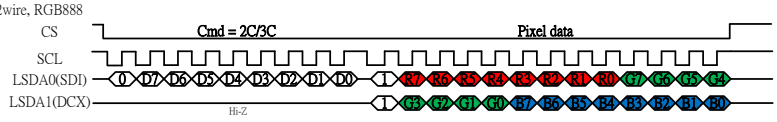
**Restriction**

DUAL SPI via SPI3 interface :

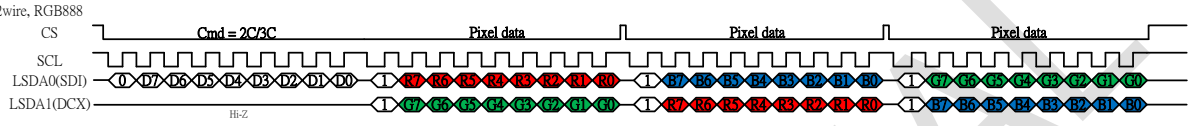
SPI3-1P1T 1wire, RGB888



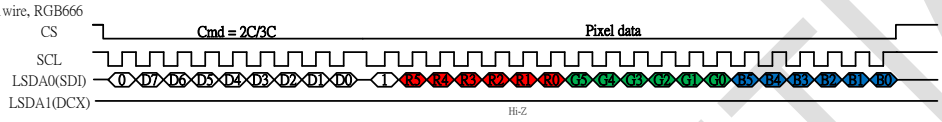

SPI3-1P1T 2wire, RGB888



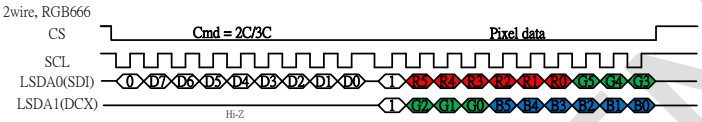

SPI3-2P3T 2wire, RGB888



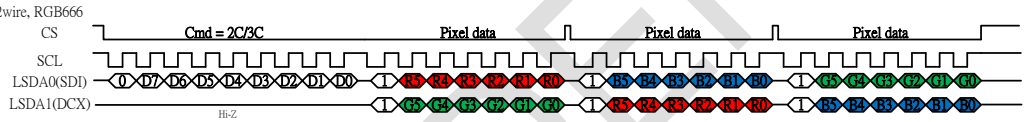

SPI3-1P1T 1wire, RGB666



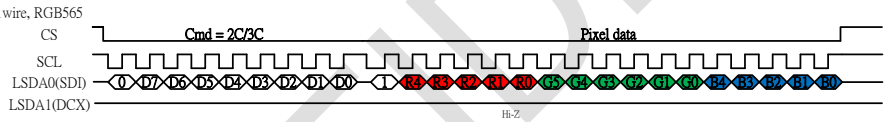

SPI3-1P1T 2wire, RGB666



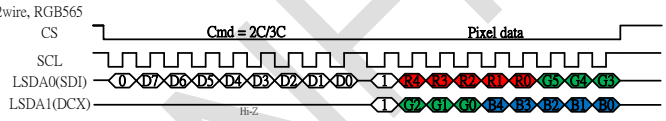

SPI3-2P3T 2wire, RGB666




SPI3-1P1T 1wire, RGB565

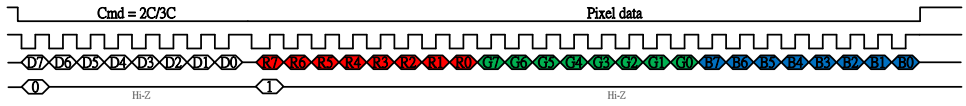



SPI3-1P1T 2wire, RGB565

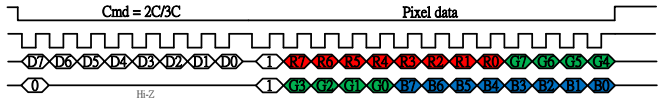


DUAL SPI via SPI4 interface :

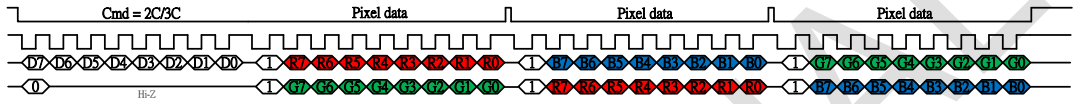
SPI4-1P1T 1wire, RGB888



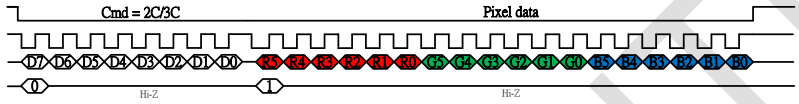

SPI4-1P1T 2wire, RGB888



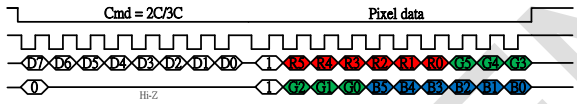

SPI4-2P3T 2wire, RGB888



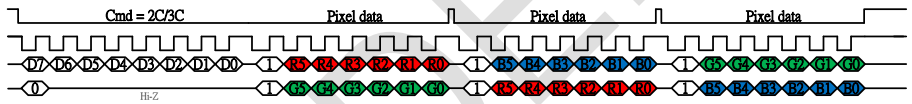

SPI4-1P1T 1wire, RGB666



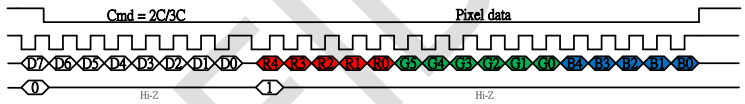

SPI4-1P1T 2wire, RGB666



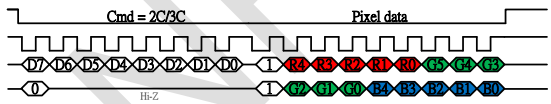

SPI4-2P3T 2wire, RGB666




SPI4-1P1T 1wire, RGB565




SPI4-1P1T 2iwre, RGB565



## RDID1 (DA00h): ID1 Code

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | DA00h | ID1[7:0] | | | | | | | | 00h |

| | |
|---|---|
| Description | This command is for Module Manufacture Number |
| Restriction | |

| Bit | Description | Data |
|---|---|---|
| ID1[7:0] | Module Manufactor Number | |

## RDID2 (DB00h): ID2 Code

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | DB00h | ID2[7:0] | | | | | | | | 80h |

| | |
|---|---|
| **Description** | This command is for Module/Driver Version Number |

| Bit | Description | Data |
|---|---|---|
| ID2[7:0] | Module/Driver Version Number | |

| | |
|---|---|
| **Restriction** | |

## RDID3 (DC00h): ID3 Code

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | DC00h | ID3[7:0] | | | | | | | | 00h |

| | |
|---|---|
| **Description** | This command is for Module / Driver ID<br>Bit: ID3[7:0] — Description: Module /Driver ID — Data: |
| **Restriction** | |

## (FE00h): CMD Mode Switch

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| W | FE00h | - | - | - | - | CMD_Page[3:0] | | | | 00 |

| | |
|---|---|
| Description | This command is used to switch the Manufacture Command Pages and User Commands sets. |

| CMD_Page[3:0] | Hex Value | Description |
|---|---|---|
| 0000 | 00h (default) | User Command Set (UCS = CMD1) |
| 0001 | 01h | Manufacture Command Set Page0 |
| 1100 | 0Ch | Manufacture Command Set Page0 extension |
| 1011 | 0Bh | Manufacture Command Set Page Panel ID |
| 0010 | 02h | Manufacture Command Set Page Gamma1 |
| 0011 | 03h | Manufacture Command Set Page Gamma2 |
| 1101 | 0Dh | Manufacture Command Set Page Gamma3 |
| 0100 | 04h | Manufacture Command Set Page VSR |
| 0110 | 06h | Manufacture Command Set Page DBC |

| | |
|---|---|
| Restriction | - |

## (FF00h): Read CMD Status

| R/W | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| R | FF00h | - | - | - | - | CMD_Status[3:0] | | | | 00 |

**Description**

This command is used to switch the Manufacture Command Pages and User Commands sets.

| CMD_Status[3:0] | Hex Value | Description |
|---|---|---|
| 0000 | 00h (default) | User Command Set (UCS = CMD1) |
| 0001 | 01h | Manufacture Command Set Page0 |
| 1100 | 0Ch | Manufacture Command Set Page0 extension |
| 1011 | 0Bh | Manufacture Command Set Page Panel ID |
| 0010 | 02h | Manufacture Command Set Page Gamma1 |
| 0011 | 03h | Manufacture Command Set Page Gamma2 |
| 1101 | 0Dh | Manufacture Command Set Page Gamma3 |
| 0100 | 04h | Manufacture Command Set Page VSR |
| 0110 | 06h | Manufacture Command Set Page DBC |

**Restriction**

-

# 7. Electrical Characteristics

## 7.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM69090 is used out of the absolute maximum ratings, the RM69090 may be permanently damaged. To use the RM69090 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM69090 will malfunction and cause poor reliability.

| item | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage | VDDI | -0.3 ~ + 5.5 | V |
| Power supply voltage | VDD (VDDA, VDDB, VDDR) | -0.3 ~ + 5.5 | V |
| Supply voltage (MV) | AVDD- AVSS | -0.3 ~ + 6.6 | V |
| | AVSS- VCL | -0.3 ~ + 5.0 | V |
| Supply voltage (HV) | VGH- VGLX | -0.3 ~ + 33 | V |
| Input voltage | VIN | -0.3 ~ VDDI+ 0.3 | V |
| Output voltage | VO | -0.3 ~ VDDI+ 0.3 | V |
| Operating temperature | Topr | -40 ~ + 85 | °C |
| Storage temperature | Tstg | -55 ~ + 125 | °C |
| Notes:<br>If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range. | | | |

## 7.2 ESD Protection Level

| Model | Test Condition | Level |
|---|---|---|
| Human Body Mode | R = 1.5 kohm / C = 100 pF | Pass 3KV |
| Machine Mode | R = 0 ohm / C = 200 pF | Pass 300V |

## 7.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.

## 7.4 DC Characteristics

### 7.4.1 Basic Characteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Related Pins |
|---|---|---|---|---|---|---|---|
| Analog Power Supply Voltage | VDD | Operation Voltage | 2.7 | 2.8 | 3.6 | V | Note 1 |
| I/O pin Power Supply Voltage | VDDI | I/O supply voltage | 1.65 | 1.8 | 3.3 | V | Note 1,2 |
| | | | | | | | |
| | | | | | | | |
| Logic High level input voltage | VIH | VDDI = 1.65V ~ 3.3V | 0.8* VDDI | - | VDDI | V | Note 3 |
| Logic Low level input voltage | VIL | VDDI = 1.65V ~ 3.3V | 0.0 | - | 0.2* VDDI | V | Note 3 |
| Logic High level Output voltage | VOH | Iout = -1 mA | 0.8* VDDI | - | VDDI | V | Note 3 |
| Logic Low level Output voltage | VOL | Iout = +1 mA | 0.0 | - | 0.2* VDDI | V | Note 3 |
| Logic High level input current (Except MIPI) | IIHD | Vin=0~VDDI | | | 1 | uA | Note 3 |
| Logic Low level input current (Except MIPI) | IILD | Vin=0~VDDI | -1 | | | uA | Note 3 |
| Logic High level input current (MIPI) | IIHD | Vin=0~VDDI | | | 1 | uA | Note 3 |
| Logic Low level input current (MIPI) | IILD | Vin=0~VDDI | -1 | | | uA | Note 3 |
| | | | | | | | |
| AVDD booster voltage | AVDD | | 4.5 | | 6.5 | V | Note 3 |
| VCL booster voltage | VCL | | -3.5 | | -5 | V | Note 3 |
| VGH booster voltage | VGH | | AVDD | | 2AVDD | V | Note 3 |
| VGL booster voltage | VGL | | VCL | | VCL -AVDD | V | Note 3 |
| Voltage difference between VGH and VGL | VGHL | \|VGH-VGL\| | | | 30 | V | Note 3 |
| Gamma reference voltage | VGMP | | 2.0 | | 6.0 | V | Note 3,4 |
| Gamma reference voltage | VGSP | | 0.0 | | 4.5 | V | Note 3 |
| | | | | | | | |
| | | | | | | | |
| OSC | Fosc | | 20.24 | 22 | 23.76 | MHz | |
| Channel deviation voltage | $V_{DEV}$ | Sout ≥ AVDD-1.0V, and 0V < Sout ≤ 1.0V | | | | mV | TBD |
| Channel deviation voltage | $V_{DEV}$ | 1.0V < Sout < AVDD-1.0V | | | | mV | TBD |
| | | | | | | | |

Notes:

1. VDD means VDDA, VDDR, VDDB. And VSS means VSSA, VSSR, VSSB, AVSS, VSSAM. VDDB, VDDA and VDDR should be the same input voltage level and larger than VDDI voltage.
2. Recommend VDDI=1.8V for power saving.
3. Ta(ambient temperature) ranges from -30℃ to 85 ℃.
4. VGMP <= AVDD – 0.5V

### 7.4.2 Operation current

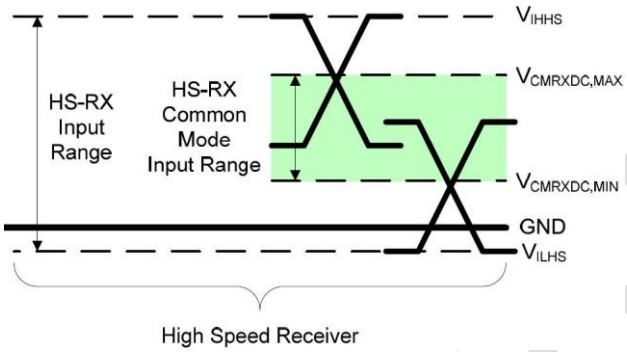
**VCI=2.8V and VDDI=1.8V**

| Parameter | Symbol | Condition | Max. | Unit |
|---|---|---|---|---|
| Sleep In Mode | I_SLP_VCI | VDDI=VCC=1.8V<br>VCI=VDDA=VDDB=VDDR=2.8V<br>HSSI_D0P/N=HSSI_D1P/N=HSSI_CKP/N=LP-11<br>Ta = 25deg | 50 | uA |
| | I_SLP_VDDI | | 180 | uA |
| Deep Standby Mode | I_DSTB_VCI | VDDI=VCC=1.8V<br>VCI=VDDA=VDDB=VDDR=2.8V<br>HSSI_D0P/N=HSSI_D1P/N=HSSI_CKP/N=0<br>Ta = 25deg | 4 | uA |
| | I_DSTB_VDDI | | 1 | uA |

## 7.5 MIPI Characteristics

### 7.5.1 High-Speed Receiver Specification

DC Specifications

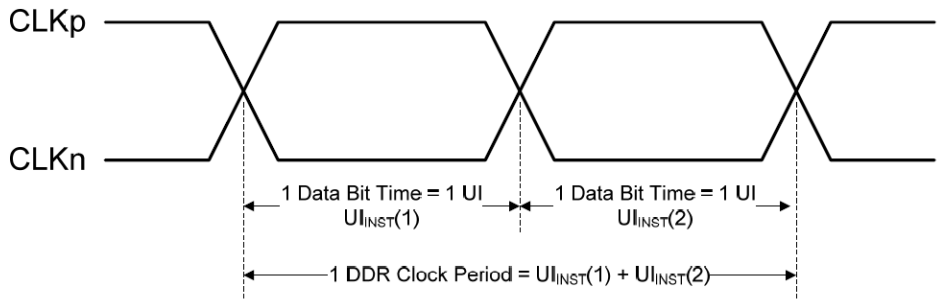



| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| VCMRX(DC) | Common-mode voltage HS receive mode | 70 | | 330 | mV | 1,2 |
| VIDTH | Differential input high threshold | | | 70 | mV | |
| VIDTL | Differential input low threshold | -70 | | | mV | |
| VIHHS | Single-ended input high voltage | | | 460 | mV | 1 |
| VILHS | Single-ended input low voltage | -40 | | | mV | 1 |
| ZID | Differential input impedance | 80 | 100 | 125 | Ω | |

Notes:
1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

### 7.5.2 Forward high speed transmissions

DDR Clock Definition




| Clock Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| UI instantaneous | $UI_{INST}$ | 2 | | 12.5 | ns | 1,2 |

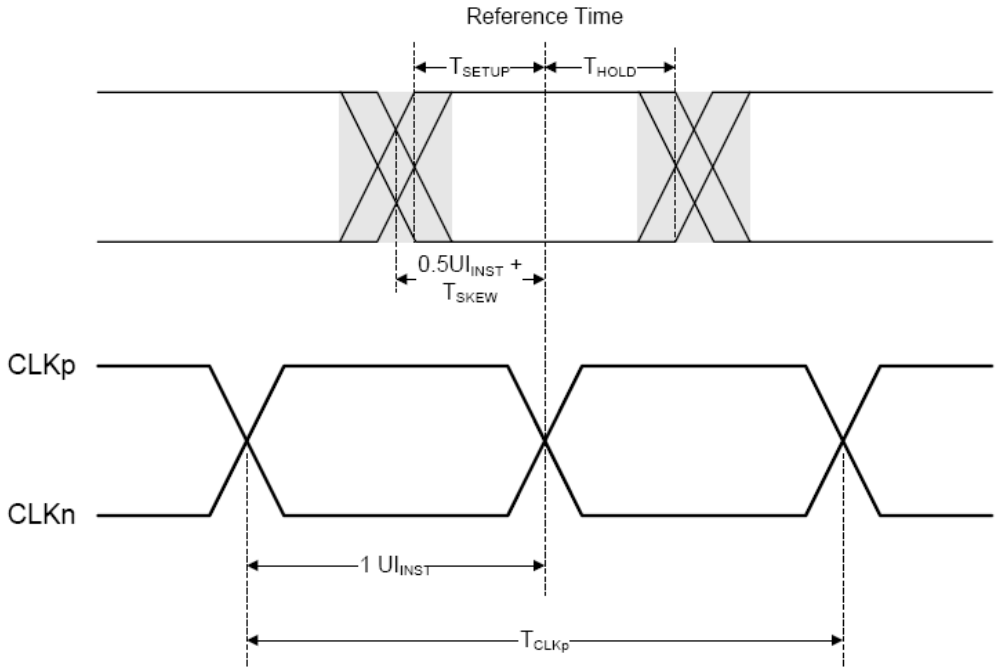
Notes:
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Data-Clock Timing Specifications

| Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Data to Clock Skew [measured at transmitter] | $T_{SKEW[TX]}$ | -0.15 | | 0.15 | $UI_{INST}$ | 1 |
| Data to Clock Setup Time [receiver] | $T_{SETUP[RX]}$ | 0.15 | | | $UI_{INST}$ | 2 |
| Clock to Data Hold Time [receiver] | $T_{HOLD[RX]}$ | 0.15 | | | $UI_{INST}$ | 2 |

Notes:
1. Total silicon and package delay budget of $0.3*UI_{INST}$
2. Total setup and hold window for receiver of 0.3*UIINST

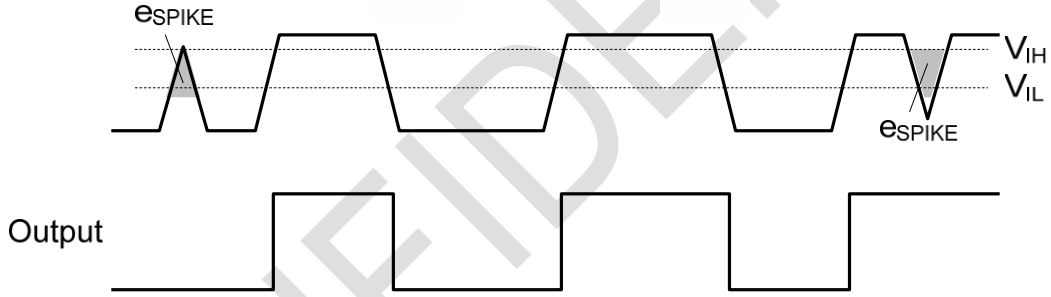
### 7.5.3 Data to Clock Timing Definitions



### 7.5.4 Low power transceiver specifications

| Parameters | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Logic high level input voltage | VIHCD | Contention Detection (Lane_D0) | 450 | | 1350 | mV |
| Logic low level input voltage | VILCD | Contention Detection (Lane_D0) | 0 | | 200 | mV |
| Logic high level input voltage | VIH-LPRX | LP-Rx (Lane_CK, Lane_D0, Lane_D1) | 880 | - | 1350 | mV |
| Logic low level input voltage | VIL-LPRX | LP-Rx (Lane_CK, Lane_D0, Lane_D1 | 0 | | 550 | mV |
| Logic low level input voltage | VIL-ULPS | LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1) | 0 | | 300 | mV |
| Logic high level input voltage | VOH-LPTX | Contention Detection (Lane_D0) | 1.1 | 1.2 | 1.3 | V |
| Logic low level input voltage | VOL-LPTX | Contention Detection (Lane_D0) | -50 | 0 | 50 | mV |
| eSPIKE[1.2.3] | Fig. 2 | Input pulse rejection | | | 300 | V.ps |

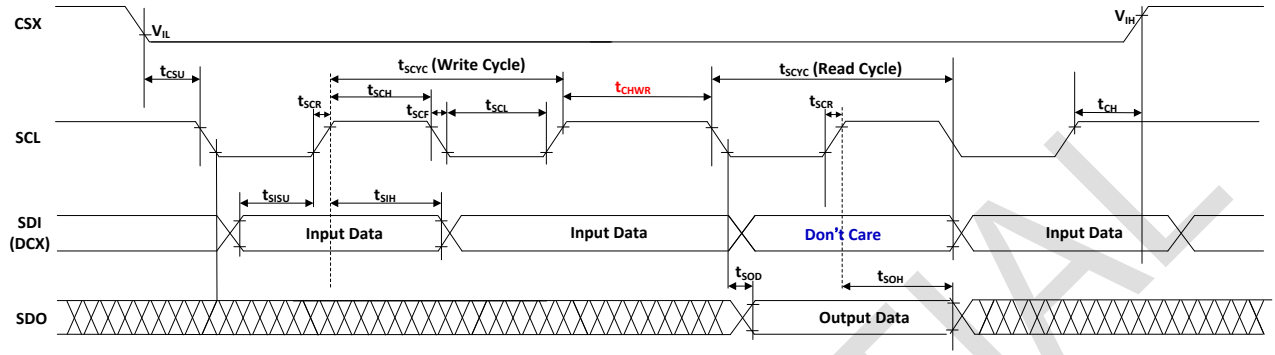
Notes:
Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State.
An impulse less than this will not change the receiver state.
In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
Input Glitch Rejection of Low Power Receivers as follow.



## 7.6 AC Characteristics

### 7.6.1 Serial Interface Characteristics

SPI Serial Interface Characteristics

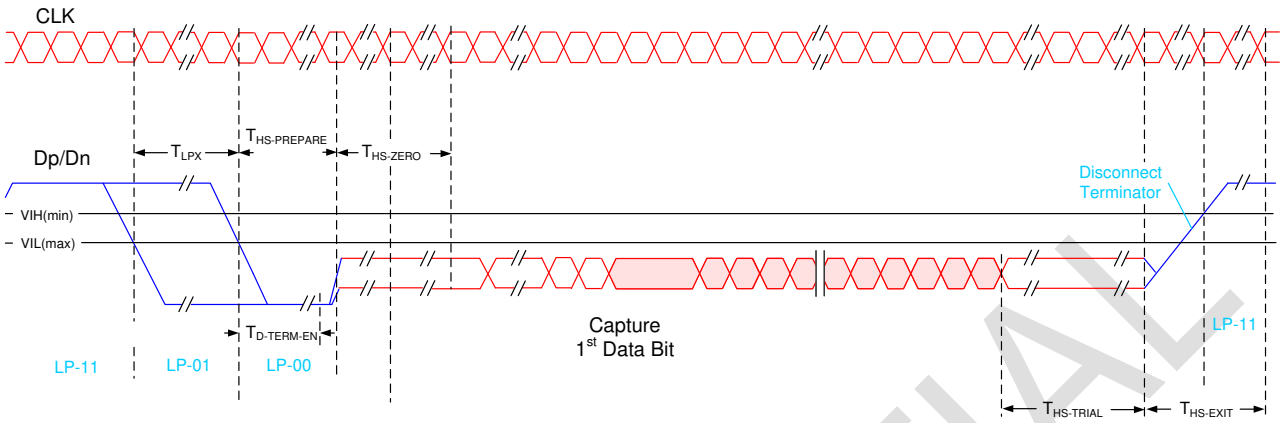



| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock cycle | $t_{SCYC}$ | Write | 20 | | | ns |
| | | Read | 300 | | | ns |
| Clock high pulse width | $t_{SCH}$ | Write | 9 | | | ns |
| | $t_{SCH}$ | Read | 140 | | | ns |
| Clock low pulse width | $t_{SCL}$ | Write | 9 | | | ns |
| | $t_{SCL}$ | Read | 140 | | | ns |
| Clock rise time | $t_{SCR}$ | 0.2*VDDI -> 0.8*VDDI | | | 2 | ns |
| Clock fall time | $t_{SCF}$ | 0.8*VDDI -> 0.2*VDDI | | | 2 | ns |
| Chip select setup time | $t_{CSU}$ | | 10 | | | ns |
| Chip select hold time | $t_{CH}$ | | 10 | | | ns |
| Data input setup time | $t_{SISU}$ | To $V_{IL}$ of SCL's rising edge | 5 | | | ns |
| Data input hold time | $t_{SIH}$ | | 5 | | | ns |
| Access time of output data | $t_{SOD}$ | From $V_{IL}$ of SCL's falling edge | | | 120 | ns |
| Hold time of output data | $t_{SOH}$ | From $V_{IH}$ of SCL's rising edge | 5 | | | ns |
| Transition time from Write cycle to Read cycle | $t_{CHWR}$ | From $V_{IH}$ of SCL's rising edge | 150 | | | ns |

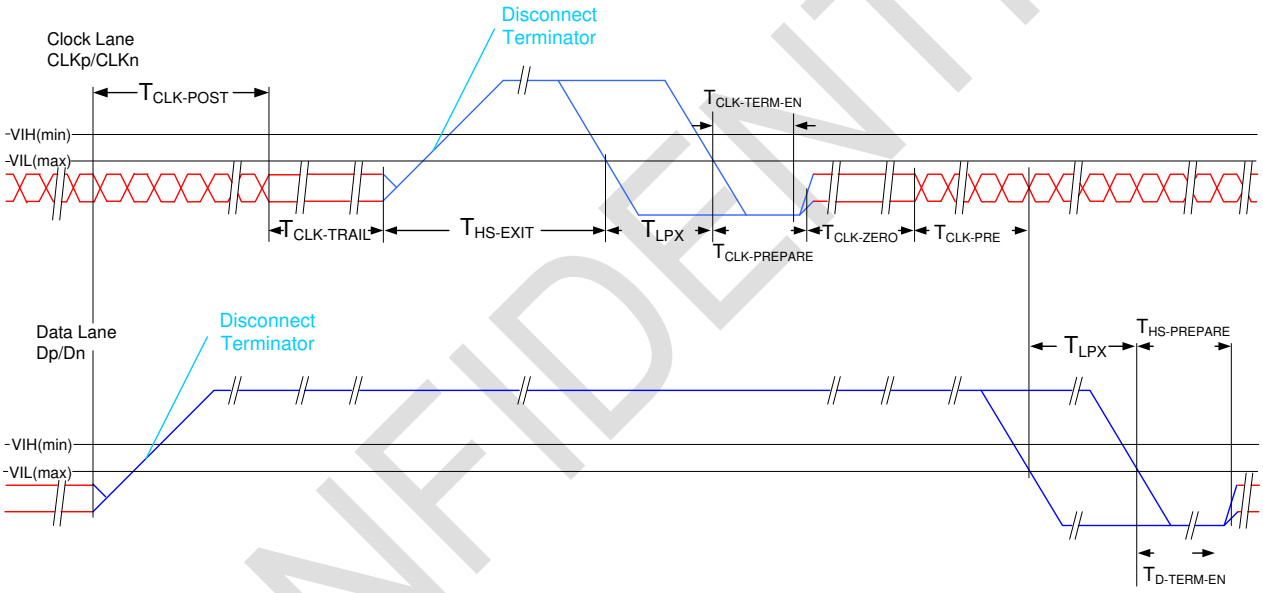
Notes:
(1) Logic high and low levels are specified as 80% and 20% of VDDI for Input signals.
(2) For the 4-wire SPI, the DCX's timing is the same as input data.
(3) Ta = -30°C to 70°C, VDDI=1.65V to 3.3V, VDD=2.7V to 3.6V, and VSS=0V

### 7.6.2 DSI Timing Characteristics

HS Data Transmission Burst



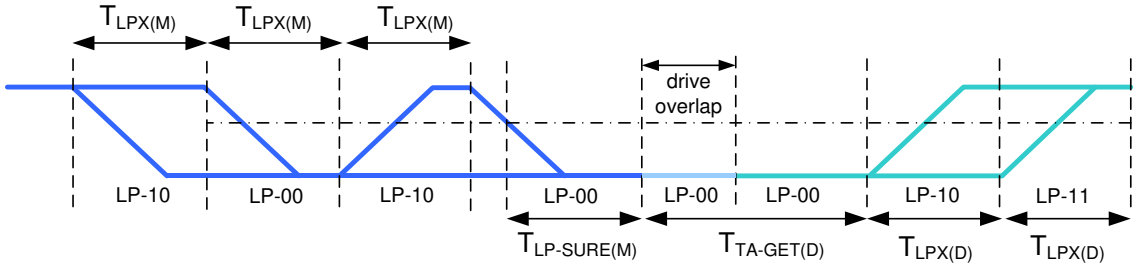

HS clock transmission



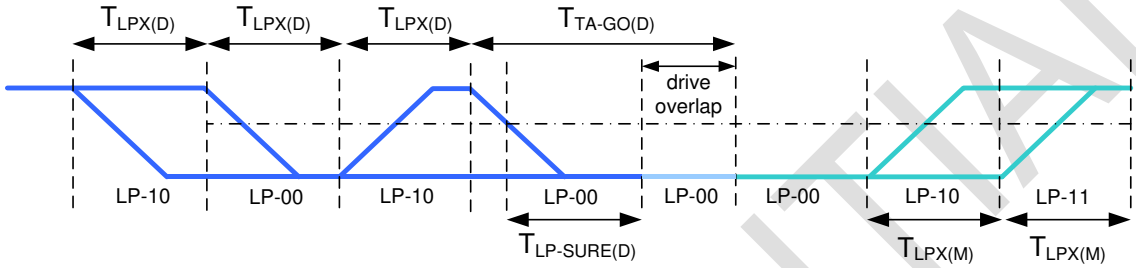
Timing Parameters:

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$ . | 60ns + 52*UI | | | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | | | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | **300** | | | ns |
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$ . | Time for Dn to reach $V_{TERM-EN}$ | | 38 | ns |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | | 95 | ns |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | | | UI |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | | | ns |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$ . | Time for Dn to reach $V_{TERM-EN}$ | | 35 ns +4*UI | |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40ns + 4*UI | | 85 ns + 6*UI | ns |
| **$T_{HS-PREPARE}$ + $T_{HS-ZERO}$** | **$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.** | **145ns + 10*UI** | | | **ns** |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | 60ns + 4*UI | | | ns |

Turnaround Procedure




Bus turnaround (BAT) from MPU to display module timing



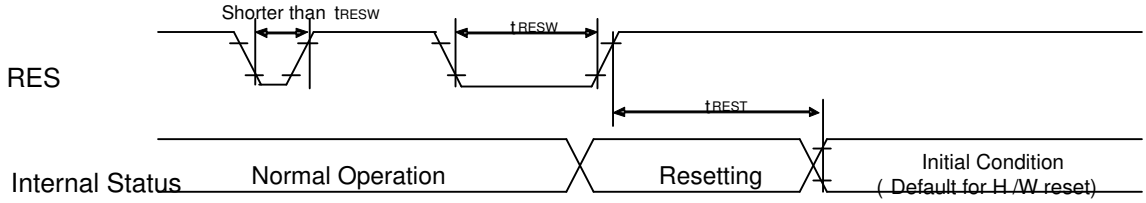

Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{LPX(M)}$ | Transmitted length of any Low-Power state period of MCU to display module | 50 | | **150** | ns | 1,2 |
| $T_{TA-SURE(M)}$ | Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX(M)}$ | | $2*T_{LPX(M)}$ | ns | 2 |
| $T_{LPX(D)}$ | Transmitted length of any Low-Power state period of display module to MCU | 50 | | **150** | ns | 1,2 |
| $T_{TA-GET(D)}$ | Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | | $5*T_{LPX(D)}$ | | ns | 2 |
| $T_{TA-GO(D)}$ | Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | | $4*T_{LPX(D)}$ | | ns | 2 |
| $T_{TA-SURE(D)}$ | Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX(D)}$ | | $2*T_{LPX(D)}$ | ns | 2 |

NOTE:
1. $T_{LPX}$ is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

### 7.6.3 Reset Timing



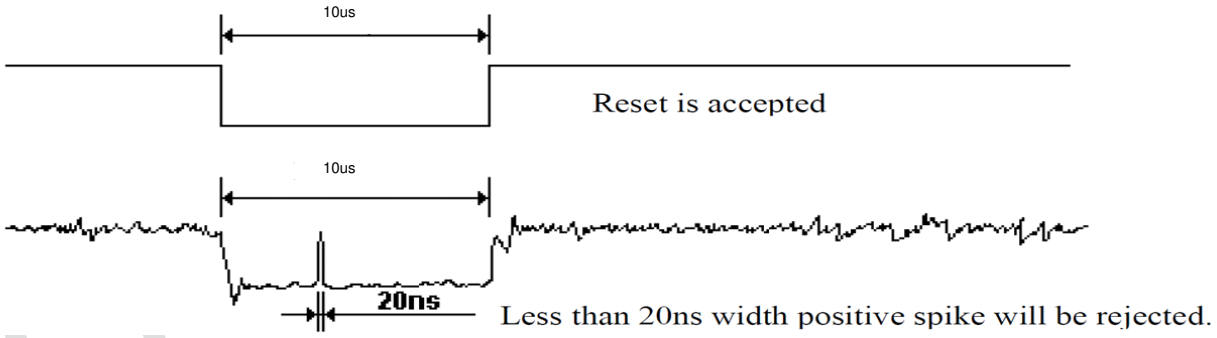

Reset input timing:
VDDI=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

| Symbol | Parameter | Related Pins | MIN | TYP | MAX | Note | Unit |
|---|---|---|---|---|---|---|---|
| $t_{RESW}$ | *1) Reset low pulse width | RESX | 10 | - | - | - | μs |
| $t_{REST}$ | *2) Reset complete time | - | - | - | 5 | When reset applied during Sleep in mode | ms |
| | | - | | - | 120 | When reset applied during Sleep out mode | ms |

*Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.*

| RESX Pulse | Action |
|---|---|
| Shorter than 5μs | Reset Rejected |
| Longer than 10μs | Reset |
| Between 5μs and 10μs | Reset starts<br>(It depends on voltage and temperature condition.) |

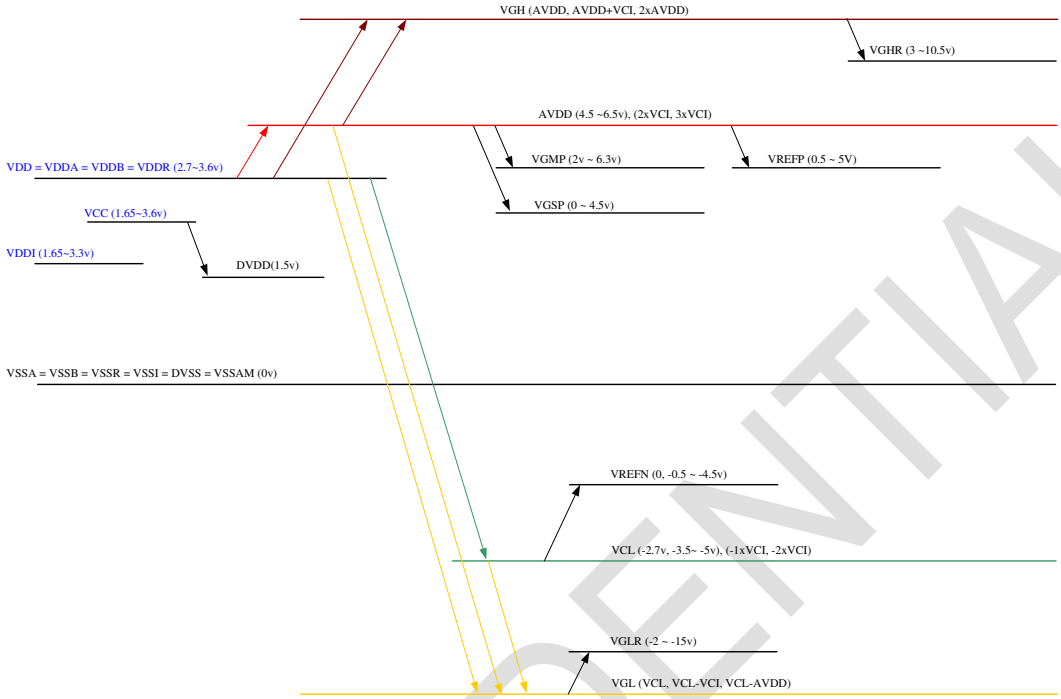
*Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.*
*Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.*
*Note 4. Spike Rejection also applies during a valid reset pulse as shown below:*




*Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.*

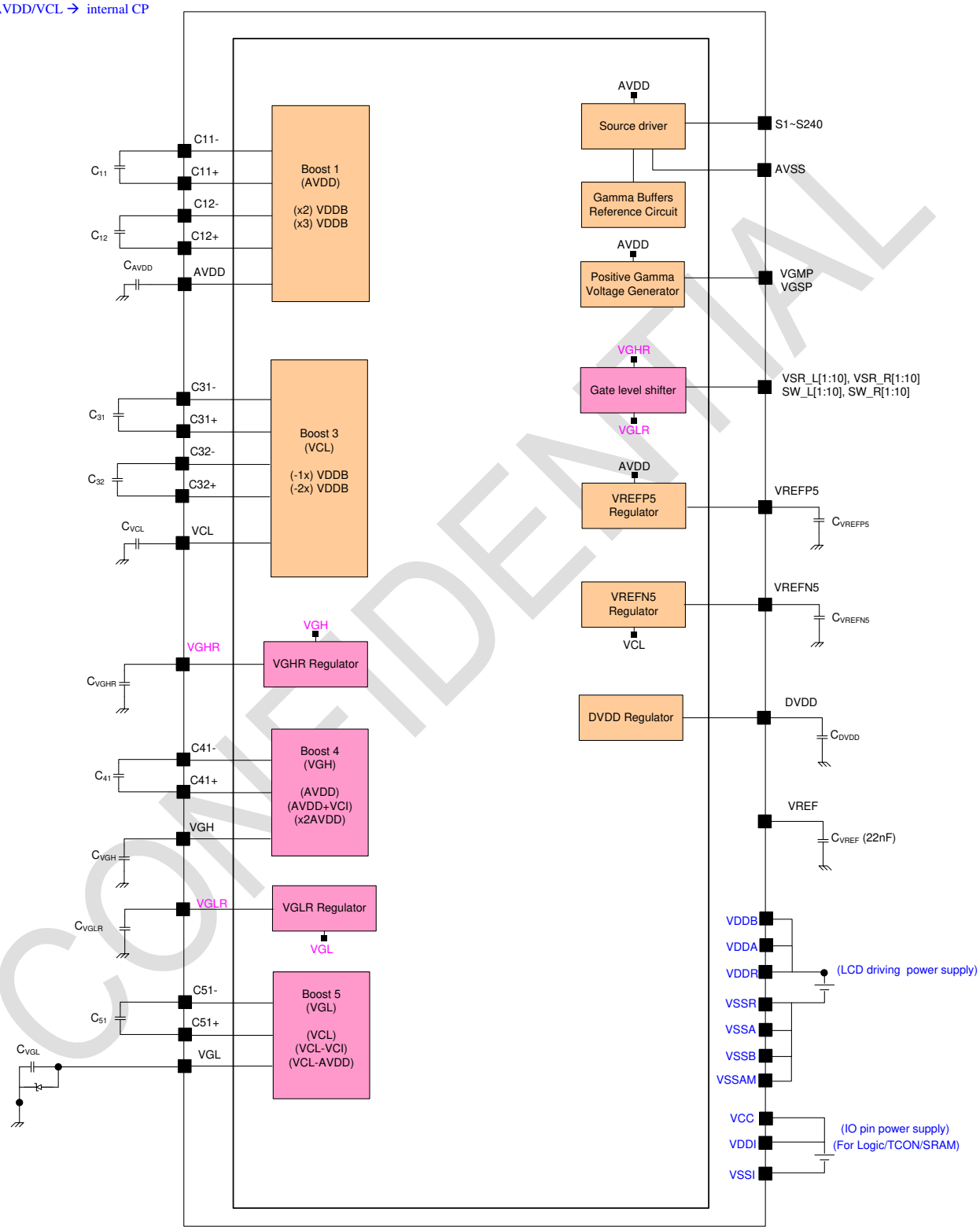
# 8. Power Generation

## 8.1 Two Supply Power ( VDDI / VDD )



## 8.2 DC/DC Converter Circuit

2PWR(VDDI, VDD)
VDD=VDDA=VDDR=VDDB
AVDD/VCL → internal CP

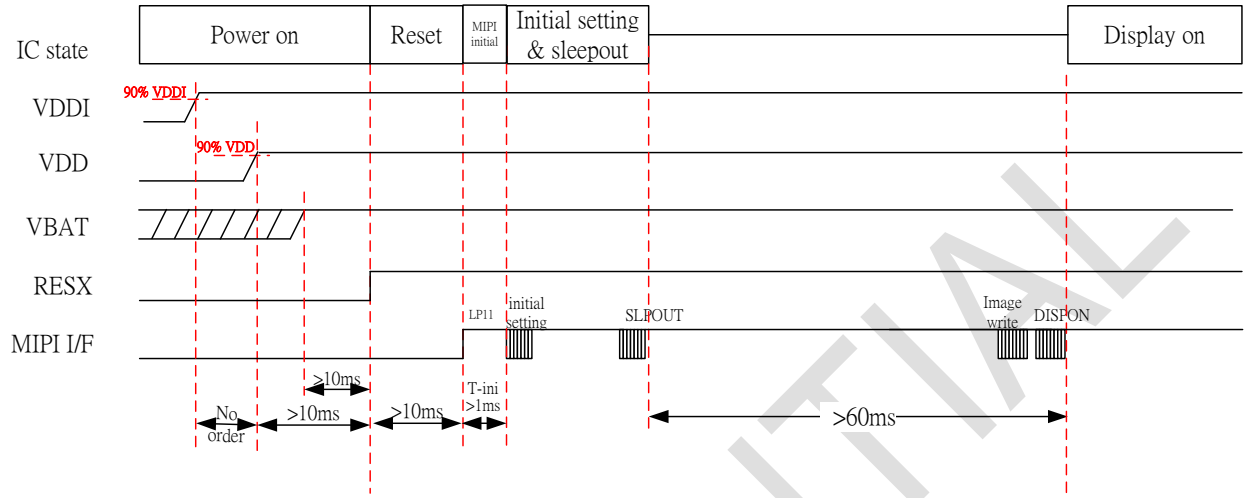


## 8.3 External Components

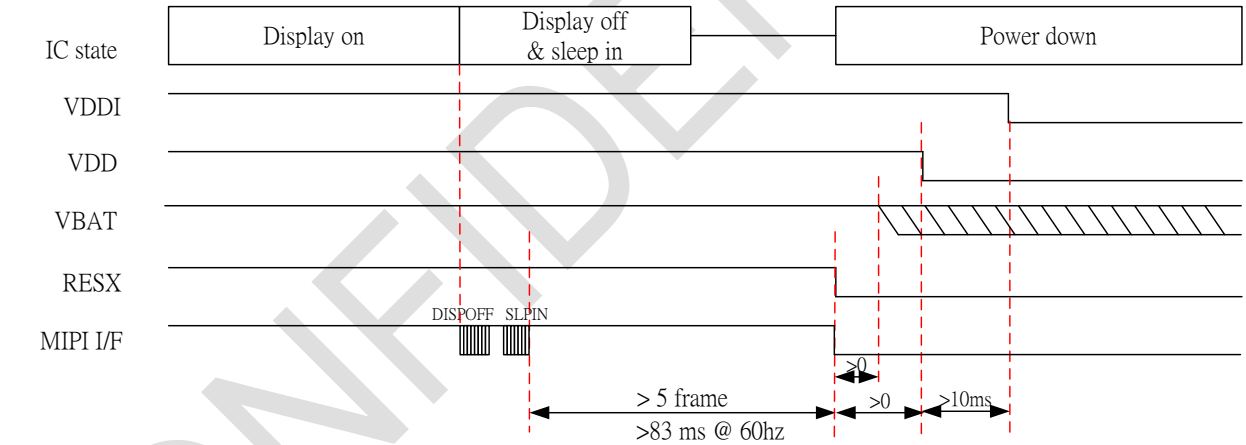
| No. | Signal name | Values | Max ability |
|---|---|---|---|
| 1 | VDDA, VDDR, VDDB | Cap , 2.2uF | 6.3V |
| 2 | VDDI, VCC | Cap , 2.2uF | 6.3V |
| 3 | VREF | Cap , 22nF | 6.3V |
| 4 | DVDD | Cap , 1.0uF | 6.3V |
| 5 | VREFN/VREFP | Cap , 1.0uF | 6.3V |
| 6 | VGHR | Cap , 2.2uF | 16V |
| 7 | VGLR | Cap , 2.2uF | 16V |
| 8 | BVP3D | Cap , 2.2uF | 10V |
| 9 | BVN3D | Cap , 2.2uF | 10V |
| 10 | C11P/C11N | Cap , 1.0uF | 6.3V |
| 11 | C12P/C12N | Cap , 1.0uF | 6.3V |
| 12 | AVDD | Cap , 2.2uF | 10V |
| 13 | C31P/C31N | Cap , 1.0uF | 6.3V |
| 14 | C32P/C32N | Cap , 1.0uF | 6.3V |
| 15 | VCL | Cap , 2.2uF | 6.3V |
| 16 | C41P/C41N | Cap , 1.0uF | 16V |
| 17 | VGH | Cap , 2.2uF | 25V |
| 18 | C51P/C51N | Cap , 1.0uF | 16V |
| 19 | VGL | Cap , 2.2uF | 25V |
| 20 | VGL (VGL-GND) | Schottky Diode | |

## 8.4 Power on/off sequence and timing

Power On sequence




Power Off sequence



## 8.5 Power Level Modes

*Normal display mode on = NORON*
*Partial mode on = PTLON*
*Idle mode off = IDMOFF*
*Idle mode on = IDMON*
*Sleep out = SLPOUT*
*Sleep in = SLPIN*
*Deep standby mode = DSTBON*

**Definition example:**

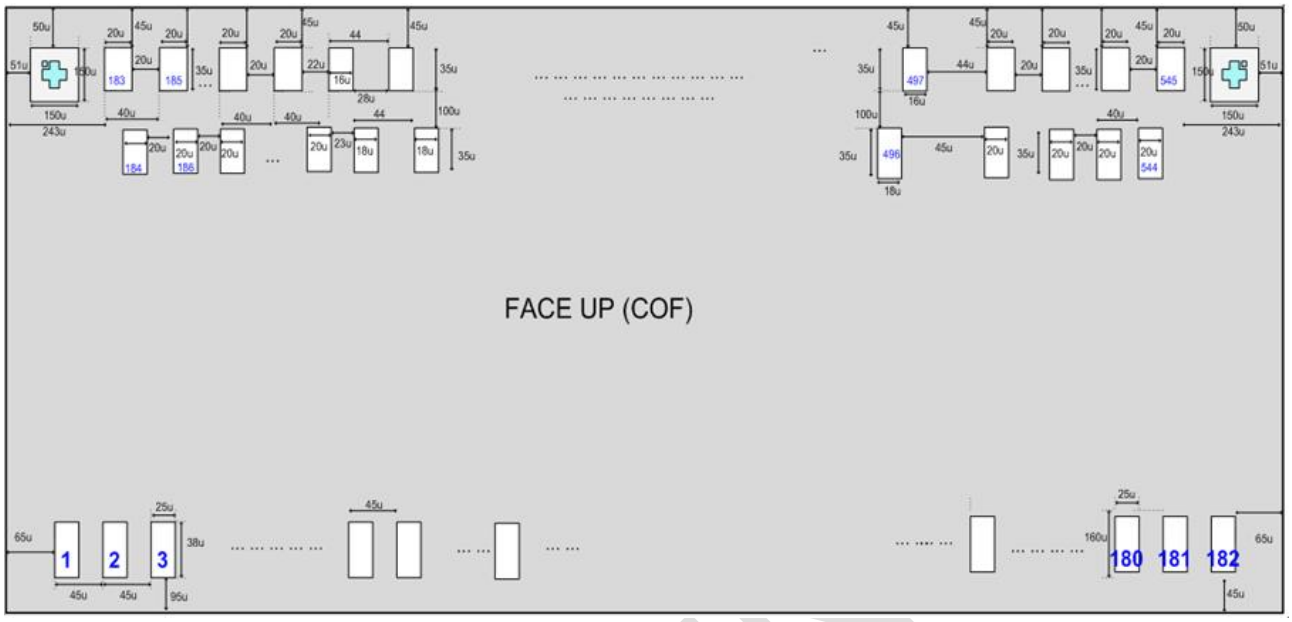
**1. Normal Mode On (full display), Idle Mode Off, Sleep Out.**
In this mode, the display is able to show maximum 16.7M colors.
**2. Partial Mode On, Idle Mode Off, Sleep Out**
In this mode, part of the display is used with maximum 16.7M colors.
**3. Normal Mode On (full display), Idle Mode On, Sleep Out.**
In this mode, the full display is used but with 8 colors.
**4. Partial Mode On, Idle Mode On, Sleep Out**
In this mode, part of the display is used but with 8 colors.
**5. Sleep In Mode.**
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.
**6. Deep Standby Mode.**
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory are random.
**7. Power Off Mode**
In this mode, VDDI and VDDA/VDDR/VDDB are removed.

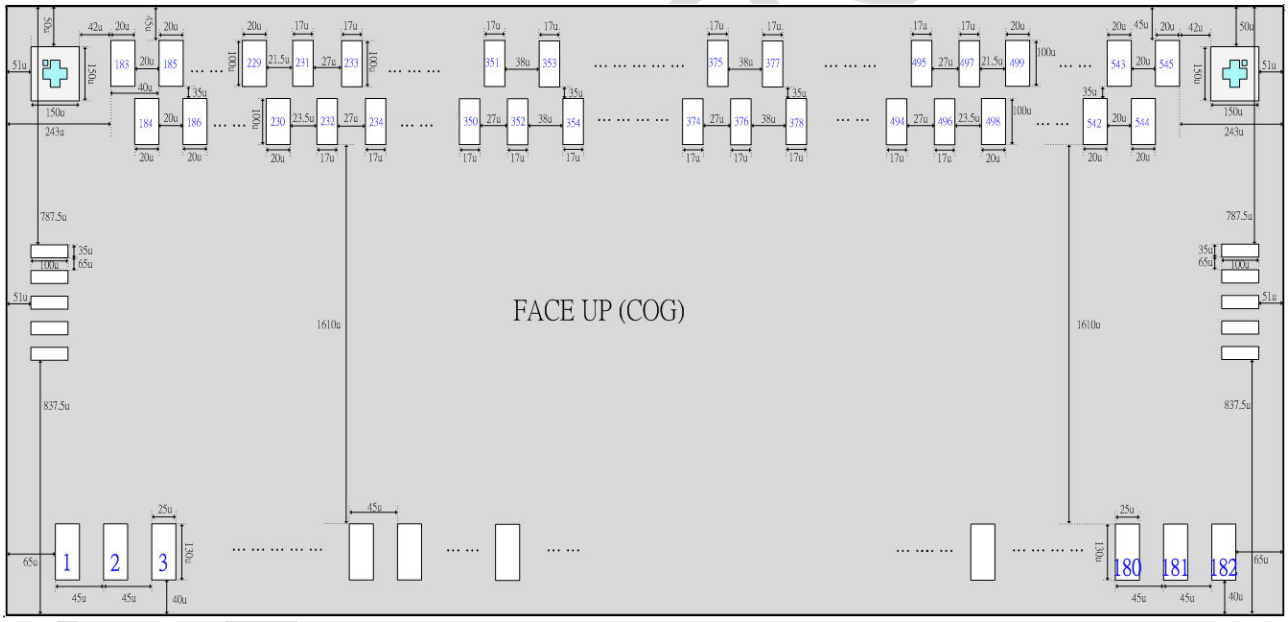
NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

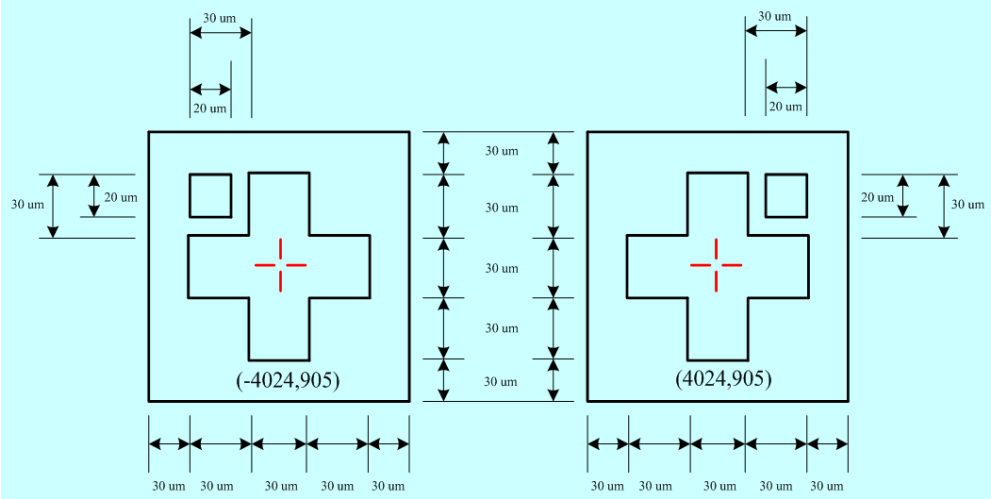
## 8.6 Maximum Series Resistance

| Pin Name | Type | Max Resistance | Unit |
|---|---|---|---|
| VDDA, VDDB, VDDR, VDDI, VCC, | Power Supply | 5 | Ω |
| AVSS, VSSAM, DVSS, VSSI, VSSA, VSSR, VSSB | Power Supply | 5 | Ω |
| AVDD | Power Input/Output | 5 | Ω |
| DVDD | Power Output | 5 | Ω |
| VCL | Power Output | 5 | Ω |
| VGH, VGL | Power Output | 10 | Ω |
| C11P/N~C12P/N | Capacitor Connection | 5 | Ω |
| C31P/N~C32P/N | Capacitor Connection | 5 | Ω |
| C41P/N | Capacitor Connection | 5 | Ω |
| C51P/N | Capacitor Connection | 5 | Ω |
| HSSI_CLK_P/N, HSSI_DATA0_P/N, HSSI_DATA1_P/N, | MIPI Interface I/O | 5 | Ω |
| TE, SWIRE, OLED_EN | Digital Output I/O | 20 | Ω |
| RESX, CSX, D/CX, SCL, SDI, SDO,D[0]~D[7] | Digital Interface I/O | 20 | Ω |
| IM[1 :0], DSWAP, PSWAP | Input I/O | 100 | Ω |
| MTP_PWR | Power Supply | 5 | Ω |
| S[1]~S[240] | Source output | 20 | Ω |
| VSR_L[1]~ VSR_L[10], VSR_R[1]~ VSR_R[10] SW_L[1]~ SW_L[10], SW_R[1]~ SW_R[10] | GOA,SWoutput | 20 | Ω |

# 9. Pad Diagram and Coordination






- Chip size: 8300 um x 2060um (Include sealing and scribe line)
- Chip thickness: 200/300 um
- PAD coordinates: PAD center
- PAD coordinates origin: Chip center
- Au bump size
  - COF:
    - 16um/18um x 35um: Source:S1~S240
    - 20um x 35um: gate control signal
    - 25um x 38um: Input Pads
  - COG:
    - 17um x 100um: Source:S1~S240
    - 20um x 100um: gate control signal
    - 25um x 130um: Input PadsAu bump pitch: See PAD coordinates table
- Au bump height: 12±2 um (typ.)
- No. in the figure corresponds to No. in the PAD coordinates table
- Alignment mark

| Alignment mark shape | X | Y |
|---|---|---|
| left | 4024 | 905 |
| right | -4024 | 905 |

◆ Pad Coordinate (Unit: um)

| NO | PAD NAME | NO | PAD NAME | NO | PAD NAME | NO | PAD NAME |
|---|---|---|---|---|---|---|---|
| 1 | ANALOG_TEST[1] | 51 | D[0] | 101 | VSSR | 151 | C32N |
| 2 | VGLR | 52 | VSSI | 102 | VSSR | 152 | C32N |
| 3 | VGLR | 53 | D[1] | 103 | VSSA | 153 | C41P |
| 4 | VGHR | 54 | D[2] | 104 | VSSA | 154 | C41P |
| 5 | VGHR | 55 | D[3] | 105 | VSSA | 155 | C41N |
| 6 | VREFP5 | 56 | D[4] | 106 | AVSS | 156 | C41N |
| 7 | VREFP5 | 57 | D[5] | 107 | AVSS | 157 | C51N |
| 8 | VREFP5 | 58 | VSSI | 108 | AVSS | 158 | C51N |
| 9 | VREFN5 | 59 | D[6] | 109 | VSSB | 159 | C51P |
| 10 | VREFN5 | 60 | D[7] | 110 | VSSB | 160 | C51P |
| 11 | VREFN5 | 61 | TEST[1] | 111 | VSSB | 161 | VGH |
| 12 | BVP3D | 62 | EXTCLK | 112 | VSSB | 162 | VGH |
| 13 | BVP3D | 63 | TEST[2] | 113 | VSSB | 163 | VGH |
| 14 | BVP3D | 64 | VSSI | 114 | C11P | 164 | VGHR |
| 15 | BVN3D | 65 | TEST[3] | 115 | C11P | 165 | VGHR |
| 16 | BVN3D | 66 | IM[1] | 116 | C11P | 166 | VGHR |
| 17 | BVN3D | 67 | IM[0] | 117 | C11N | 167 | VGLR |
| 18 | VCL | 68 | DSWAP | 118 | C11N | 168 | VGLR |
| 19 | VCL | 69 | TESTEN | 119 | C11N | 169 | VGLR |
| 20 | VCL | 70 | PSWAP | 120 | C12P | 170 | VGL |
| 21 | AVDD | 71 | BSTM | 121 | C12P | 171 | VGL |
| 22 | AVDD | 72 | VDDI | 122 | C12P | 172 | VGL |
| 23 | AVDD | 73 | VDDI | 123 | C12N | 173 | AVSS |
| 24 | VREF | 74 | VDDI | 124 | C12N | 174 | AVSS |
| 25 | VGSP | 75 | VCC | 125 | C12N | 175 | AVSS |
| 26 | VGMP | 76 | VCC | 126 | VDDB | 176 | MTP_PWR |
| 27 | ANALOG_TEST[2] | 77 | VCC | 127 | VDDB | 177 | MTP_PWR |
| 28 | VDDR | 78 | DVDD | 128 | VDDB | 178 | MTP_PWR |
| 29 | VDDR | 79 | DVDD | 129 | VDDB | 179 | MTP_PWR |
| 30 | VDDR | 80 | DVDD | 130 | VDDB | 180 | MTP_PWR |
| 31 | VDDA | 81 | DVDD | 131 | VDDR | 181 | MTP_PWR |
| 32 | VDDA | 82 | DVSS | 132 | VDDR | 182 | DUMMY |
| 33 | VDDA | 83 | DVSS | 133 | VDDR | 183 | VGLR |
| 34 | AVSS | 84 | DVSS | 134 | VDDR | 184 | VGLR |
| 35 | AVSS | 85 | DVSS | 135 | AVDD | 185 | VGHR |
| 36 | AVSS | 86 | HSSI_D1_P | 136 | AVDD | 186 | VGHR |
| 37 | VSSR | 87 | HSSI_D1_P | 137 | AVDD | 187 | VREFP5 |
| 38 | VSSR | 88 | HSSI_D1_N | 138 | C31P | 188 | VREFP5 |
| 39 | VSSR | 89 | HSSI_D1_N | 139 | C31P | 189 | VREFN5 |
| 40 | TE1 | 90 | VSSAM | 140 | C31P | 190 | VREFN5 |
| 41 | SWIRE | 91 | HSSI_CLK_P | 141 | C31N | 191 | VSR_L[10] |
| 42 | OLED_EN | 92 | HSSI_CLK_P | 142 | C31N | 192 | VSR_L[10] |
| 43 | TE | 93 | HSSI_CLK_N | 143 | C31N | 193 | VSR_L[9] |
| 44 | RESX | 94 | HSSI_CLK_N | 144 | VCL | 194 | VSR_L[9] |
| 45 | SDO | 95 | VSSAM | 145 | VCL | 195 | VSR_L[8] |
| 46 | VSSI | 96 | HSSI_D0_P | 146 | VCL | 196 | VSR_L[8] |
| 47 | SDI_RDX | 97 | HSSI_D0_P | 147 | C32P | 197 | VSR_L[7] |
| 48 | DCX | 98 | HSSI_D0_N | 148 | C32P | 198 | VSR_L[7] |
| 49 | WRX_SCL | 99 | HSSI_D0_N | 149 | C32P | 199 | VSR_L[6] |
| 50 | CSX | 100 | VSSR | 150 | C32N | 200 | VSR_L[6] |

| | |
|---|---|
| 201 | VSR_L[5] |
| 202 | VSR_L[5] |
| 203 | VSR_L[4] |
| 204 | VSR_L[4] |
| 205 | VSR_L[3] |
| 206 | VSR_L[3] |
| 207 | VSR_L[2] |
| 208 | VSR_L[2] |
| 209 | VSR_L[1] |
| 210 | VSR_L[1] |
| 211 | SW_L[1] |
| 212 | SW_L[1] |
| 213 | SW_L[2] |
| 214 | SW_L[2] |
| 215 | SW_L[3] |
| 216 | SW_L[3] |
| 217 | SW_L[4] |
| 218 | SW_L[4] |
| 219 | SW_L[5] |
| 220 | SW_L[5] |
| 221 | SW_L[6] |
| 222 | SW_L[6] |
| 223 | SW_L[7] |
| 224 | SW_L[7] |
| 225 | SW_L[8] |
| 226 | SW_L[8] |
| 227 | SW_L[9] |
| 228 | SW_L[9] |
| 229 | SW_L[10] |
| 230 | SW_L[10] |
| 231 | SDMY[21] |
| 232 | S[240] |
| 233 | S[239] |
| 234 | S[238] |
| 235 | S[237] |
| 236 | S[236] |
| 237 | S[235] |
| 238 | S[234] |
| 239 | S[233] |
| 240 | S[232] |
| 241 | S[231] |
| 242 | S[230] |
| 243 | S[229] |
| 244 | S[228] |
| 245 | S[227] |
| 246 | S[226] |
| 247 | S[225] |
| 248 | S[224] |
| 249 | S[223] |
| 250 | S[222] |

| | |
|---|---|
| 251 | S[221] |
| 252 | S[220] |
| 253 | S[219] |
| 254 | S[218] |
| 255 | S[217] |
| 256 | S[216] |
| 257 | S[215] |
| 258 | S[214] |
| 259 | S[213] |
| 260 | S[212] |
| 261 | S[211] |
| 262 | S[210] |
| 263 | S[209] |
| 264 | S[208] |
| 265 | S[207] |
| 266 | S[206] |
| 267 | S[205] |
| 268 | S[204] |
| 269 | S[203] |
| 270 | S[202] |
| 271 | S[201] |
| 272 | S[200] |
| 273 | S[199] |
| 274 | S[198] |
| 275 | S[197] |
| 276 | S[196] |
| 277 | S[195] |
| 278 | S[194] |
| 279 | S[193] |
| 280 | S[192] |
| 281 | S[191] |
| 282 | S[190] |
| 283 | S[189] |
| 284 | S[188] |
| 285 | S[187] |
| 286 | S[186] |
| 287 | S[185] |
| 288 | S[184] |
| 289 | S[183] |
| 290 | S[182] |
| 291 | S[181] |
| 292 | S[180] |
| 293 | S[179] |
| 294 | S[178] |
| 295 | S[177] |
| 296 | S[176] |
| 297 | S[175] |
| 298 | S[174] |
| 299 | S[173] |
| 300 | S[172] |

| | |
|---|---|
| 301 | S[171] |
| 302 | S[170] |
| 303 | S[169] |
| 304 | S[168] |
| 305 | S[167] |
| 306 | S[166] |
| 307 | S[165] |
| 308 | S[164] |
| 309 | S[163] |
| 310 | S[162] |
| 311 | S[161] |
| 312 | S[160] |
| 313 | S[159] |
| 314 | S[158] |
| 315 | S[157] |
| 316 | S[156] |
| 317 | S[155] |
| 318 | S[154] |
| 319 | S[153] |
| 320 | S[152] |
| 321 | S[151] |
| 322 | S[150] |
| 323 | S[149] |
| 324 | S[148] |
| 325 | S[147] |
| 326 | S[146] |
| 327 | S[145] |
| 328 | S[144] |
| 329 | S[143] |
| 330 | S[142] |
| 331 | S[141] |
| 332 | S[140] |
| 333 | S[139] |
| 334 | S[138] |
| 335 | S[137] |
| 336 | S[136] |
| 337 | S[135] |
| 338 | S[134] |
| 339 | S[133] |
| 340 | S[132] |
| 341 | S[131] |
| 342 | S[130] |
| 343 | S[129] |
| 344 | S[128] |
| 345 | S[127] |
| 346 | S[126] |
| 347 | S[125] |
| 348 | S[124] |
| 349 | S[123] |
| 350 | S[122] |

| | |
|---|---|
| 351 | S[121] |
| 352 | VGHR |
| 353 | VGLR |
| 354 | VREFN5 |
| 355 | SDMY[1] |
| 356 | SDMY[2] |
| 357 | SDMY[3] |
| 358 | SDMY[4] |
| 359 | SDMY[5] |
| 360 | SDMY[6] |
| 361 | SDMY[7] |
| 362 | SDMY[8] |
| 363 | SDMY[9] |
| 364 | SDMY[10] |
| 365 | SDMY[11] |
| 366 | SDMY[12] |
| 367 | SDMY[13] |
| 368 | SDMY[14] |
| 369 | SDMY[15] |
| 370 | SDMY[16] |
| 371 | SDMY[17] |
| 372 | SDMY[18] |
| 373 | SDMY[19] |
| 374 | SDMY[20] |
| 375 | VREFP5 |
| 376 | VGLR |
| 377 | VGHR |
| 378 | S[120] |
| 379 | S[119] |
| 380 | S[118] |
| 381 | S[117] |
| 382 | S[116] |
| 383 | S[115] |
| 384 | S[114] |
| 385 | S[113] |
| 386 | S[112] |
| 387 | S[111] |
| 388 | S[110] |
| 389 | S[109] |
| 390 | S[108] |
| 391 | S[107] |
| 392 | S[106] |
| 393 | S[105] |
| 394 | S[104] |
| 395 | S[103] |
| 396 | S[102] |
| 397 | S[101] |
| 398 | S[100] |
| 399 | S[99] |
| 400 | S[98] |

| | |
|---|---|
| 401 | S[97] |
| 402 | S[96] |
| 403 | S[95] |
| 404 | S[94] |
| 405 | S[93] |
| 406 | S[92] |
| 407 | S[91] |
| 408 | S[90] |
| 409 | S[89] |
| 410 | S[88] |
| 411 | S[87] |
| 412 | S[86] |
| 413 | S[85] |
| 414 | S[84] |
| 415 | S[83] |
| 416 | S[82] |
| 417 | S[81] |
| 418 | S[80] |
| 419 | S[79] |
| 420 | S[78] |
| 421 | S[77] |
| 422 | S[76] |
| 423 | S[75] |
| 424 | S[74] |
| 425 | S[73] |
| 426 | S[72] |
| 427 | S[71] |
| 428 | S[70] |
| 429 | S[69] |
| 430 | S[68] |
| 431 | S[67] |
| 432 | S[66] |
| 433 | S[65] |
| 434 | S[64] |
| 435 | S[63] |
| 436 | S[62] |
| 437 | S[61] |
| 438 | S[60] |
| 439 | S[59] |
| 440 | S[58] |
| 441 | S[57] |
| 442 | S[56] |
| 443 | S[55] |
| 444 | S[54] |
| 445 | S[53] |
| 446 | S[52] |
| 447 | S[51] |
| 448 | S[50] |
| 449 | S[49] |
| 450 | S[48] |

| | |
|---|---|
| 451 | S[47] |
| 452 | S[46] |
| 453 | S[45] |
| 454 | S[44] |
| 455 | S[43] |
| 456 | S[42] |
| 457 | S[41] |
| 458 | S[40] |
| 459 | S[39] |
| 460 | S[38] |
| 461 | S[37] |
| 462 | S[36] |
| 463 | S[35] |
| 464 | S[34] |
| 465 | S[33] |
| 466 | S[32] |
| 467 | S[31] |
| 468 | S[30] |
| 469 | S[29] |
| 470 | S[28] |
| 471 | S[27] |
| 472 | S[26] |
| 473 | S[25] |
| 474 | S[24] |
| 475 | S[23] |
| 476 | S[22] |
| 477 | S[21] |
| 478 | S[20] |
| 479 | S[19] |
| 480 | S[18] |
| 481 | S[17] |
| 482 | S[16] |
| 483 | S[15] |
| 484 | S[14] |
| 485 | S[13] |
| 486 | S[12] |
| 487 | S[11] |
| 488 | S[10] |
| 489 | S[9] |
| 490 | S[8] |
| 491 | S[7] |
| 492 | S[6] |
| 493 | S[5] |
| 494 | S[4] |
| 495 | S[3] |
| 496 | S[2] |
| 497 | S[1] |
| 498 | SW_R[10] |
| 499 | SW_R[10] |
| 500 | SW_R[9] |

| | |
|---|---|
| 501 | SW_R[9] |
| 502 | SW_R[8] |
| 503 | SW_R[8] |
| 504 | SW_R[7] |
| 505 | SW_R[7] |
| 506 | SW_R[6] |
| 507 | SW_R[6] |
| 508 | SW_R[5] |
| 509 | SW_R[5] |
| 510 | SW_R[4] |
| 511 | SW_R[4] |
| 512 | SW_R[3] |
| 513 | SW_R[3] |
| 514 | SW_R[2] |
| 515 | SW_R[2] |
| 516 | SW_R[1] |
| 517 | SW_R[1] |
| 518 | VSR_R[1] |
| 519 | VSR_R[1] |
| 520 | VSR_R[2] |
| 521 | VSR_R[2] |
| 522 | VSR_R[3] |
| 523 | VSR_R[3] |
| 524 | VSR_R[4] |
| 525 | VSR_R[4] |
| 526 | VSR_R[5] |
| 527 | VSR_R[5] |
| 528 | VSR_R[6] |
| 529 | VSR_R[6] |
| 530 | VSR_R[7] |
| 531 | VSR_R[7] |
| 532 | VSR_R[8] |
| 533 | VSR_R[8] |
| 534 | VSR_R[9] |
| 535 | VSR_R[9] |
| 536 | VSR_R[10] |
| 537 | VSR_R[10] |
| 538 | VREFN5 |
| 539 | VREFN5 |
| 540 | VREFP5 |
| 541 | VREFP5 |
| 542 | VGHR |
| 543 | VGHR |
| 544 | VGLR |
| 545 | VGLR |
| | |
| | |
| | |
| | |
| | |