Raytheon

RMDA1840

18-40 GHz Broad Band Driver Amplifier MMIC

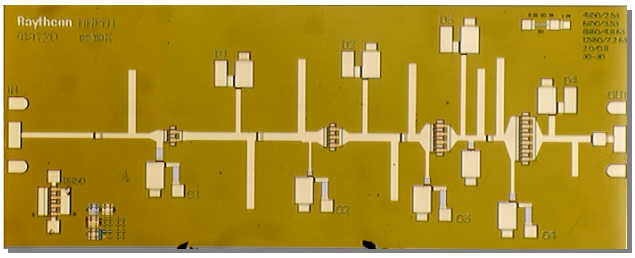
PRODUCT INFORMATION

Description

The RMDA1840 is a 4-stage GaAs MMIC amplifier designed as a 18 to 40 GHz broad band amplifier for use in point to point radios, point to multi-point communications, LMDS, and other millimeter wave applications. The RMDA1840 utilizes Raytheon's 0.25µm power PHEMT process and is sufficiently versatile to serve in a variety of applications, such as a driver amplifier or a frequency multiplier.

Features

- 4 mil substrate
- Small-signal gain 22 dB (typ.)
- Pout 1 dB comp 23 dBm (typ.)
- Chip size 4.67 mm x 2.00 mm



Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Positive DC voltage (+5 V Typical)	Vd	+6	Volts
Negative DC voltage	Vg	-2	Volts
Simultaneous (Vd - Vg)	Vdg	+8	Volts
Positive DC Current	I_D	442	mA
RF Input Power (from 50 Ω source)	P_{IN}	+15	dBm
Operating Baseplate Temperature	T_C	-30 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Thermal Resistance (Channel to Backside)	R_{JC}	53	°C/W

Electrical Characteristics

(At 25°C), 50 Ω system, Vd = +5 V, Quiescent Current Idq = 400 mA

Parameter	Min	Typ	Max	Unit
Frequency Range	18		40	GHz
Gate Supply Voltage (Vg)[1]		-0.2		V
Gain Small Signal at Pin = -5 dBm	20	22		dB
Gain Variation vs Frequency		+/-2.5		dB
Gain at 1dB Compression		21		dB
Power Output at 1 dB Compression		23		dBm

Parameter	Min	Typ	Max	Unit
Power Output Saturated: Pin = +3 dBm	21	24		dBm
Power Added Efficiency (PAE): at P1dB		15		%
Input Return Loss (Pin = -5 dBm)		8		dB
Output Return Loss (Pin = -5 dBm)		10		dB

Notes:

1. Typical range of gate voltage is -1.0 to 0 V to set Idq of 400 mA.

Characteristic performance data and specifications are subject to change without notice.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typically 2 mil between the chip and the substrate material.

Recommended Procedure for Biasing and Operation

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

CAUTION: LOSS OF GATE VOLTAGES (Vg) WHILE DRAIN VOLTAGES (Vd) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier.

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the grounds of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5 V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +5 V to Vd.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq = 400 mA.

Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

(i) Turn off RF input power,

(ii) Turn down and off drain voltage (Vd),

(iii) Turn down and off gate bias voltage (Vg).

Figure 1 Functional Block Diagram

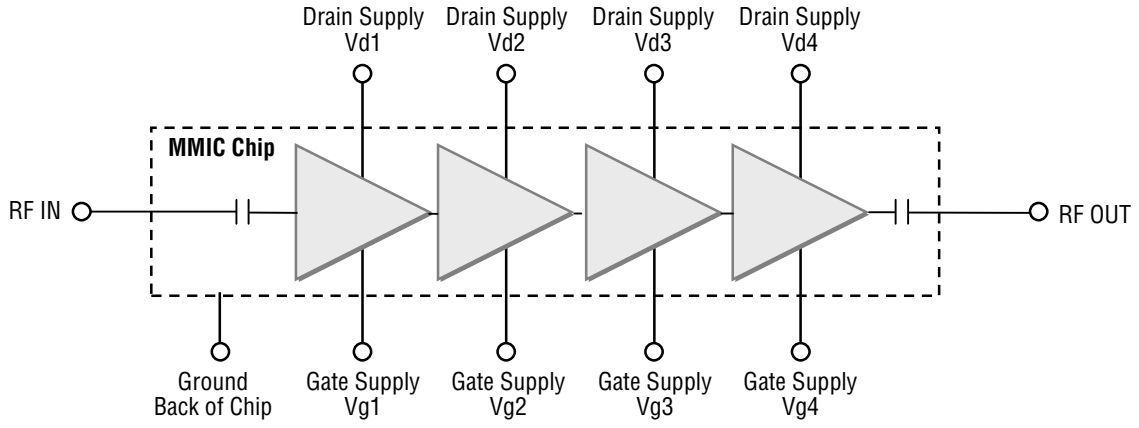

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Figure 2
Chip Layout and Bond Pad Locations

Chip Size is 4.67 mm x 2.0 mm x 100 µm. Back of chip is RF and DC ground

Dimensions in mm

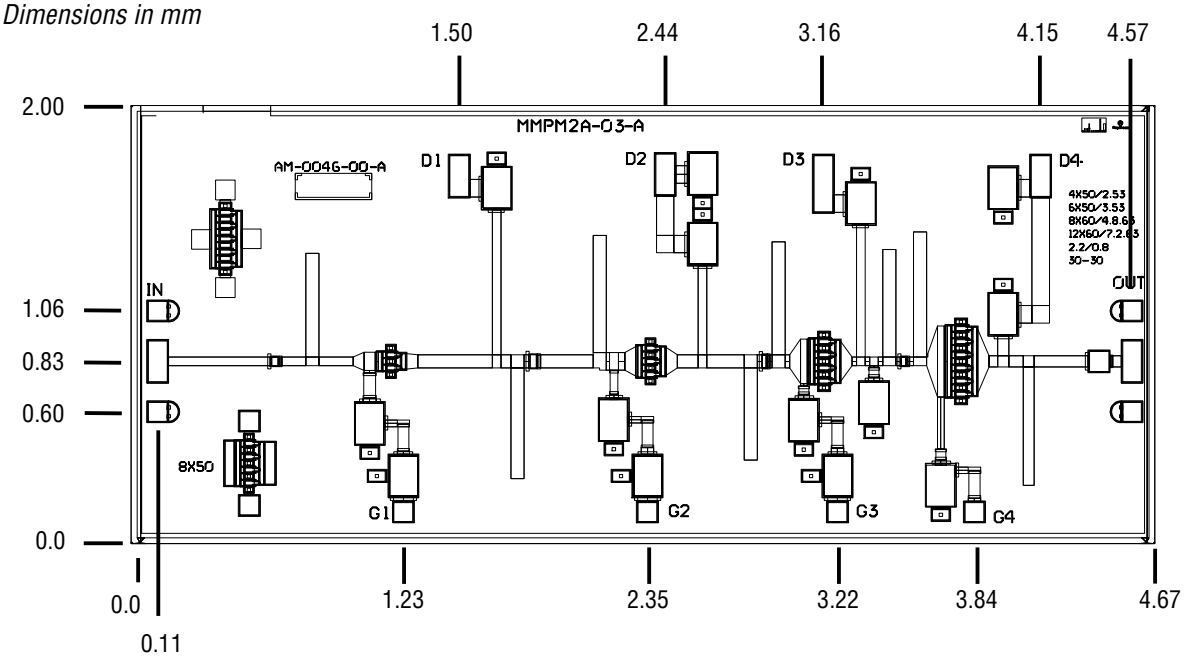
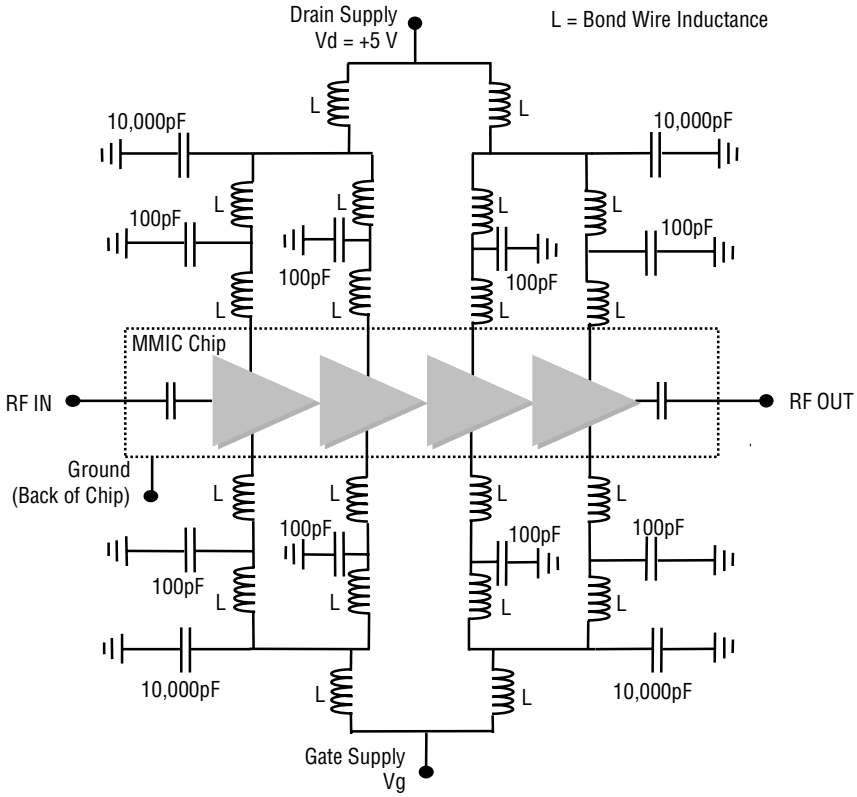


Figure 3
Recommended Application Schematic Circuit Diagram



Note: For output power level detection, bias both detector and reference diodes. DC voltage difference between detector and reference can be used to measure output power after calibration. If output power level detection is not desired, do not make connection to detector bond pad.

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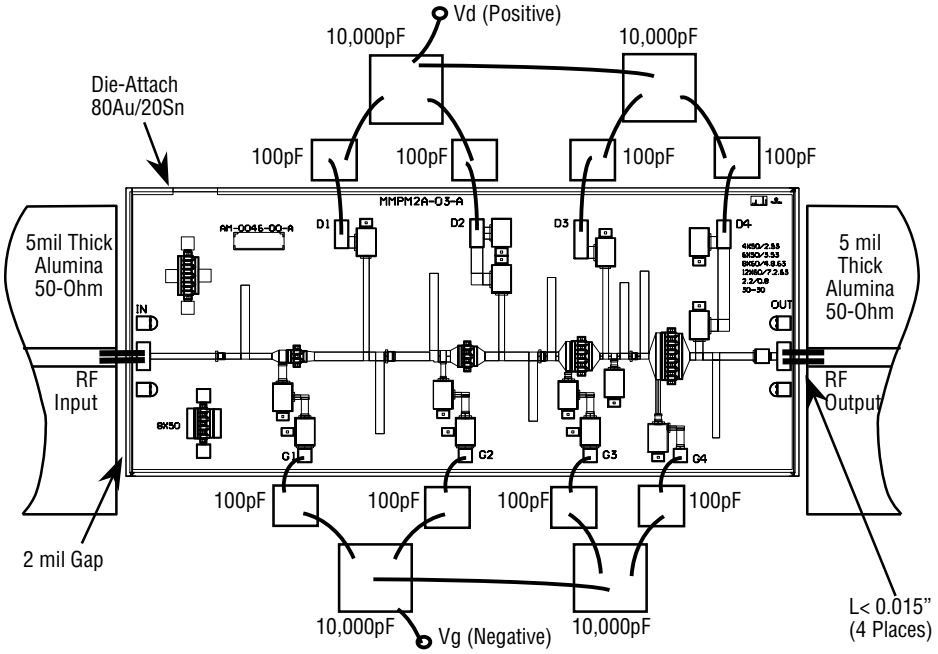
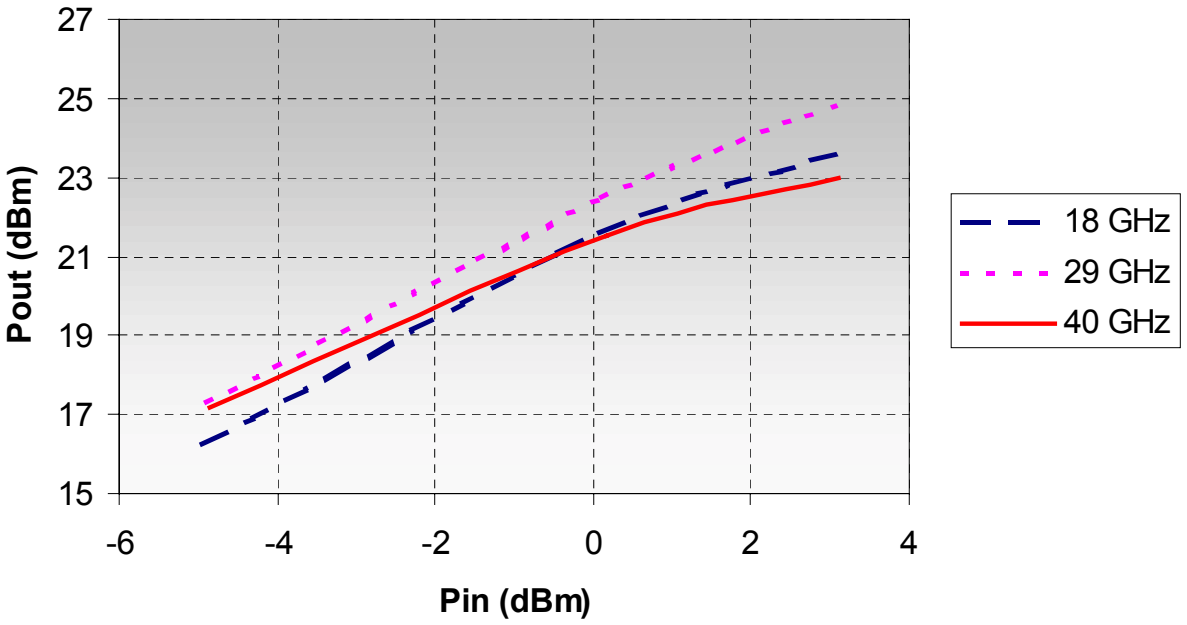
Figure 4
Recommended
Assembly Diagram



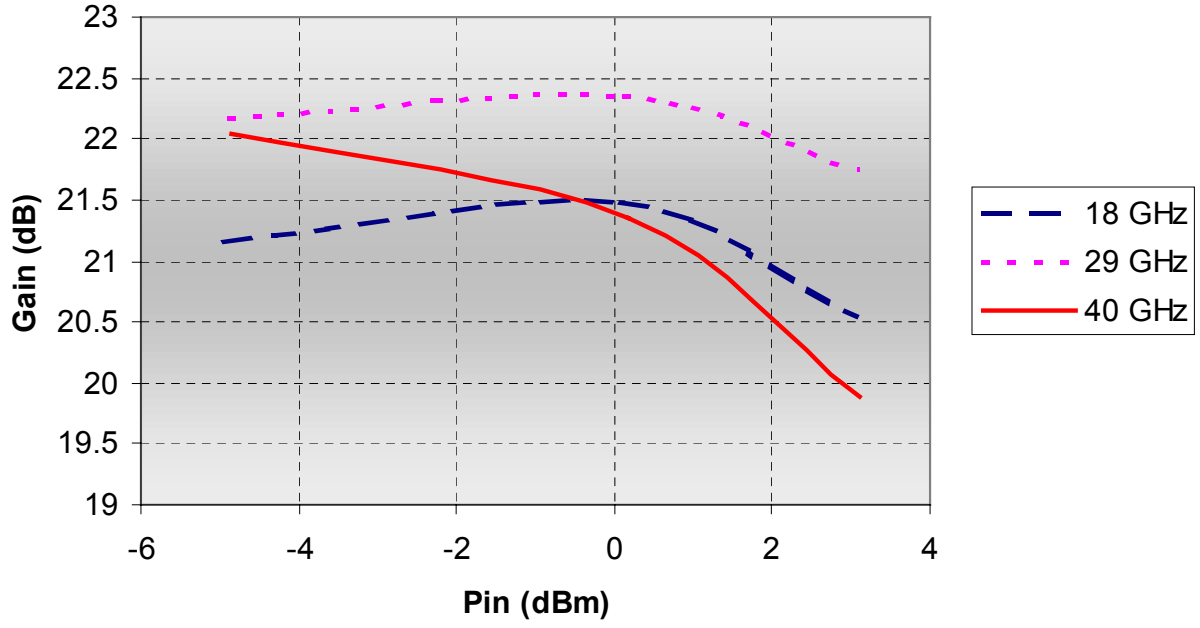
Note Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief. If output power level detection is not desired, do not make connection to detector bond pad.

Performance Data

Pout vs. Pin
Vd = 5V, Id = 400mA



Gain vs. Pin
Vd = 5V, Id = 400mA



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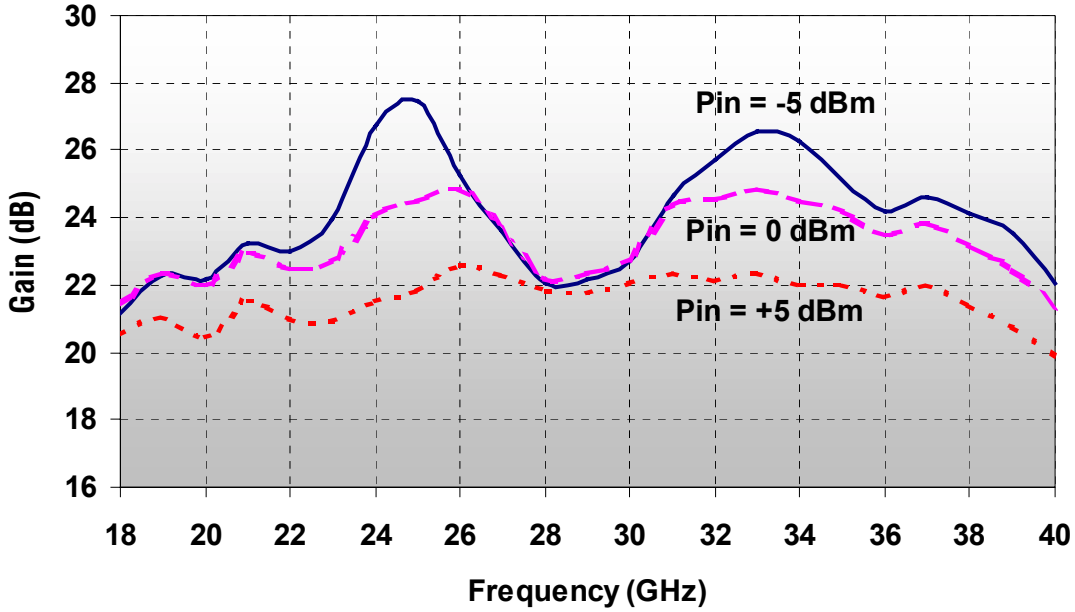
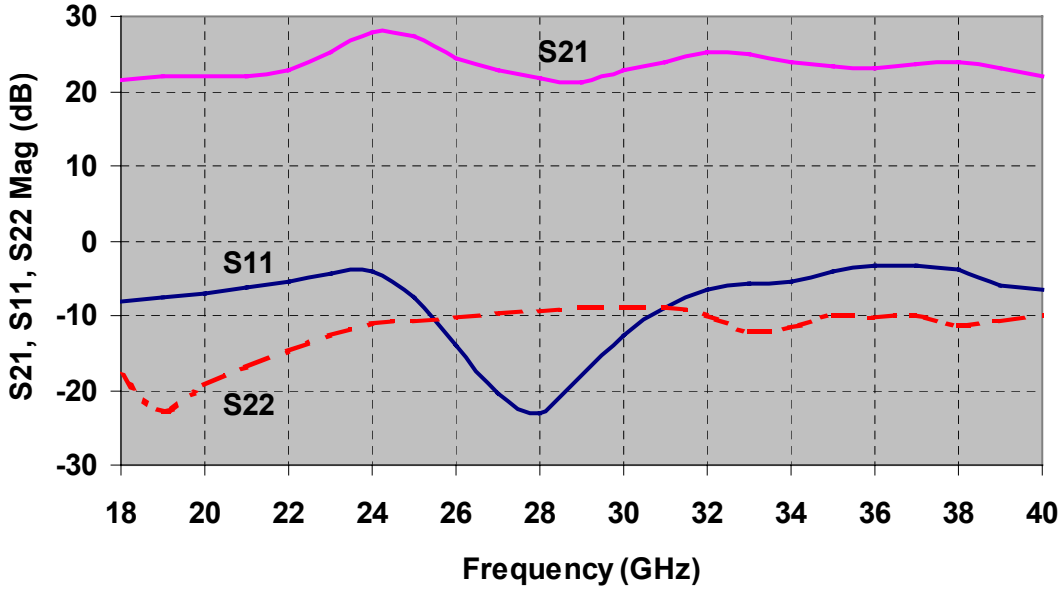
Performance Data

Gain vs. Frequency
Power In = -5, 0, +5 dBm Vd = 5V, Id = 400mA



S21, S11, S22 Mag
vs. Frequency Vd = 5V, Id = 400mA



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