FAIRCHILD SEMICONDUCTOR®

May 2004

RMPA2450

2.4–2.5 GHz GaAs MMIC Power Amplifier

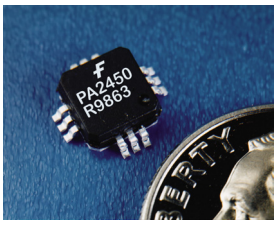
General Description

The Fairchild RMPA2450 is a fully monolithic power amplifier in a surface mount package for use in wireless applications in the 2.4 to 2.5GHz ISM frequency band. The amplifier may be biased for linear, class AB or class F for high efficiency applications. On-chip matching components allow operation in a 50Ω system with no external matching components. The MMIC chip design utilizes our 0.25µm power PHEMT process.

Features

- 35% Power Added Efficiency
- 31dBm Output Power (P1dB) at Vd = +7V
- 28dBm Output Power (P1dB) at Vd = +5V
- No external RF matching components
- Small Package Outline: 0.28" x 0.28" x 0.07"
- Thermal Resistance (Channel to Case): 33°C/W

Device



Absolute Ratings

Symbol	Parameter	Rating	Units
Vd1, Vd2	Positive Drain DC Voltage	+8	V
Vg1, Vg2	Negative Gate DC Voltage	-5	V
Vd–Vg	Simultaneous Drain to Gate Voltage	+10	V
P_{IN}	RF Input Power (from 50Ω source)	+10	dBm
Ids	Drain to Source Current	575	mA
Ig	Gate Current	5	mA
Tch	Channel Temperature	150	°C
T_{CASE}	Operating Case Temperature	-40 to 100	°C
T_{STG}	Storage Temperature Range	-40 to 125	°C

Electrical Characteristics (Note 4, At 25°C, Z_O = 50Ω, Unless Otherwise Noted)

Parameter	Min	Typ	Max	Units
Frequency Range	2400	2450	2500	MHz
Gain[1, 2, 4]		30		dB
Output Power, P1dB[1,4]		28		dBm
Assoc. Power Added Efficiency		35		%
Output Power, P1dB[3]		31		dBm
Assoc. Power Added Efficiency		33		%
Drain Current (Idd1 + Idd2)			550	mA
Gate Current (Igg1 + Igg2)			5	mA
Input Return Loss (50Ω)	7.5			dB

Notes:
1: Idq = 360mA, Vd1 = Vd2 = 5.0V
2: Pin = -3dBm,
3: Vd1 = Vd2 = +7V
4: Production Testing includes Gain, Output Power (P1dB) and Input Return Loss at Vd1 = Vd2 = 5.0V, Vg1 = Vg2 = -0.5V (nominal) , adjusted for Idq = 360mA, Pin = -3 dBm and at F = 2.45 GHz. Other Parameters are guaranteed by Design Validation Testing.

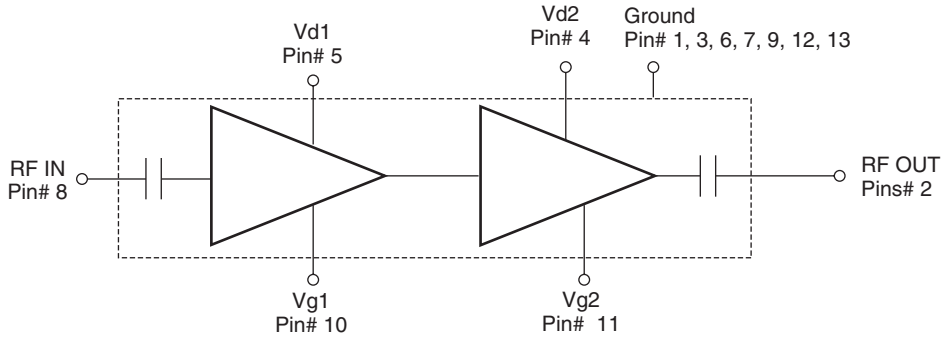
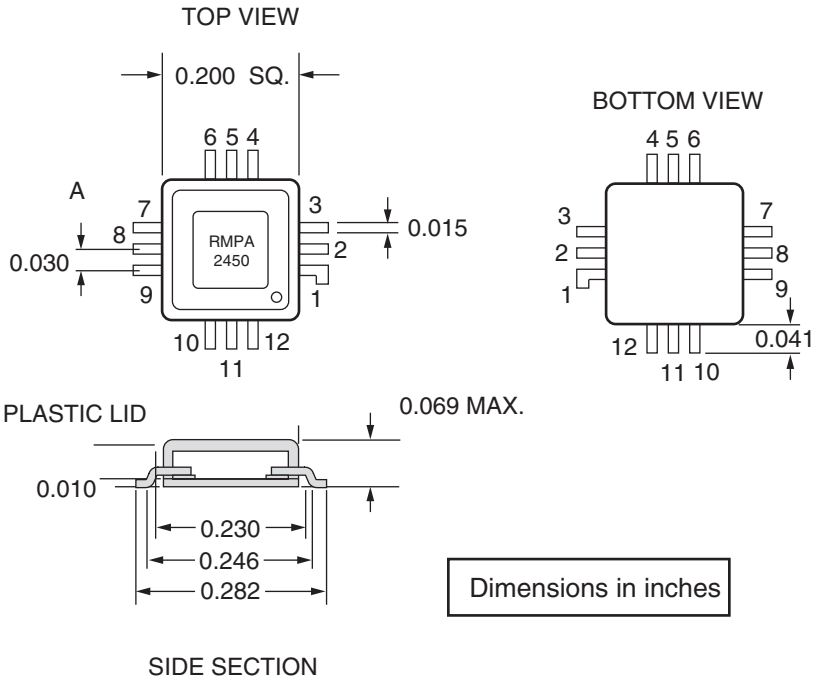


Figure 1. Functional Block Diagram (RMPA2450)



Pin#	Description
1	GND
2	RF Out
3	GND
4	Vd2
5	Vd1
6	GND
7	GND
8	RF
9	GND
10	Vg1
11	Vg2
12	GND
13	GND (PACKAGE BASE)

Figure 2. Outline Dimensions (RMPA2450)

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

The following briefly describes a procedure for evaluating the high efficiency PHEMT amplifier packaged in a surface mount package. It may be noted that the chip is a fully monolithic amplifier for ISM band applications. Figure 1 shows the functional block diagram of the packaged product.

Test Fixture

Figure 2 shows the outline and pin-out descriptions for the packaged device. A typical test fixture schematic showing external bias components is shown in Figure 3. Figure 4 shows typical layout of an evaluation board corresponding to the schematic diagram. The following should be noted:

(1) Package pin designations are as shown in Figure 2.

(2) Vg1, Vg2 are the Gate Voltages (negative) applied at the pins of the package

(3) Vgg1 = Vgg2 = Vgg is the negative supply voltage at the evaluation board terminal

(4) Vd1, Vd2 are the Drain Voltages (positive) applied at the pins of the package

(5) Vdd1 = Vdd2 = Vdd is the positive supply voltage at the evaluation board terminal

Test Procedure for the Evaluation Board (RMPA2450-TB)

The following sequence of procedure must be followed to properly test the power amplifier:

CAUTION: LOSS OF GATE VOLTAGES (VG1, VG2) WHILE DRAIN VOLTAGES (VD1,VD2) ARE PRESENT MAY DAMAGE THE AMPLIFIER.

Step 1: Turn off RF input power.

Step 2: Use GND terminal of the evaluation board for DC supplies.
Apply gate supply voltages of typical -0.5V to evaluation board terminals Vgg.

Step 3: Apply drain supply voltages of +5.0V to evaluation board terminals Vdd.
Adjust gate supply voltage, if needed, to set the desired quiescent bias currents Idq (or to the values as shown on the data summary accompanying the product samples).

Step 4: After the bias condition is established, RF input signal may now be applied.

Step 5: Follow turn-off sequence of:
(i) Turn off RF Input Power (ii) Turn down and off Vdd (iii) Turn down and off Vgg

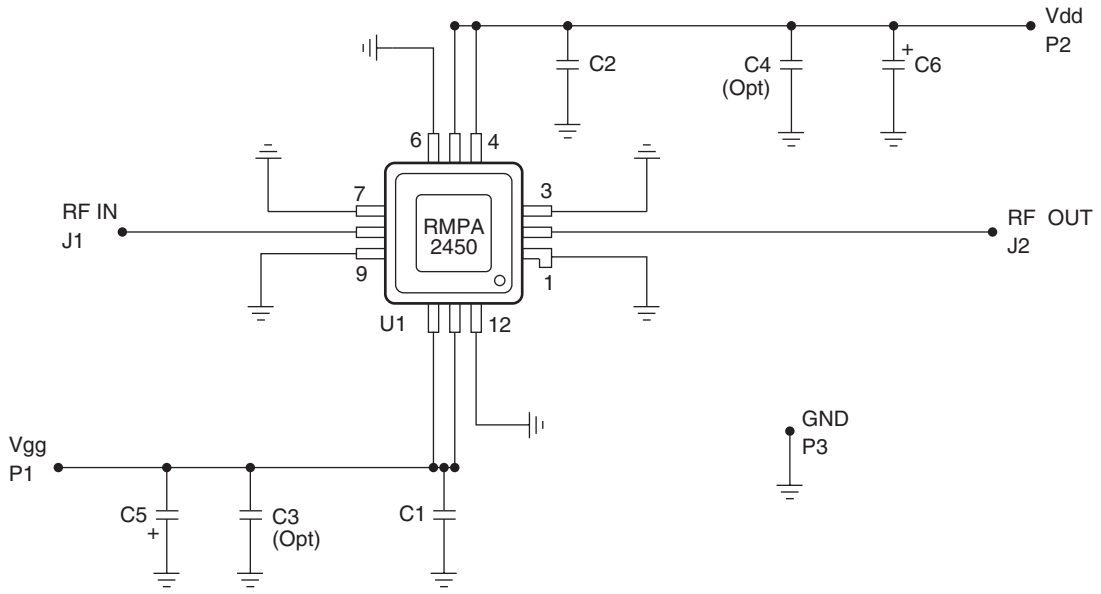


Figure 3. Schematic for a Typical Test Evaluation Board (RMPA2450-TB)

Parts List for Test Evaluation Board (RMPA2450-TB), G654220

Part	Rating	Size (L" X W")	Vendors
C1, C2	330pF	.04" X .02"	AVX, Murata, Novacap
C3, C4	1000pF	.04" X .02"	AVX, Murata, Novacap
C5, C6	4.75µF	.14" X .11"	Sprague, ATC, AVX, Murata
U1	RMPA2550	.28" X .28" X .07	
P1, P2, P3	Terminals		Sametec
J1, J2	SMA Connectors		E.F. Johnson
Board	FR4		

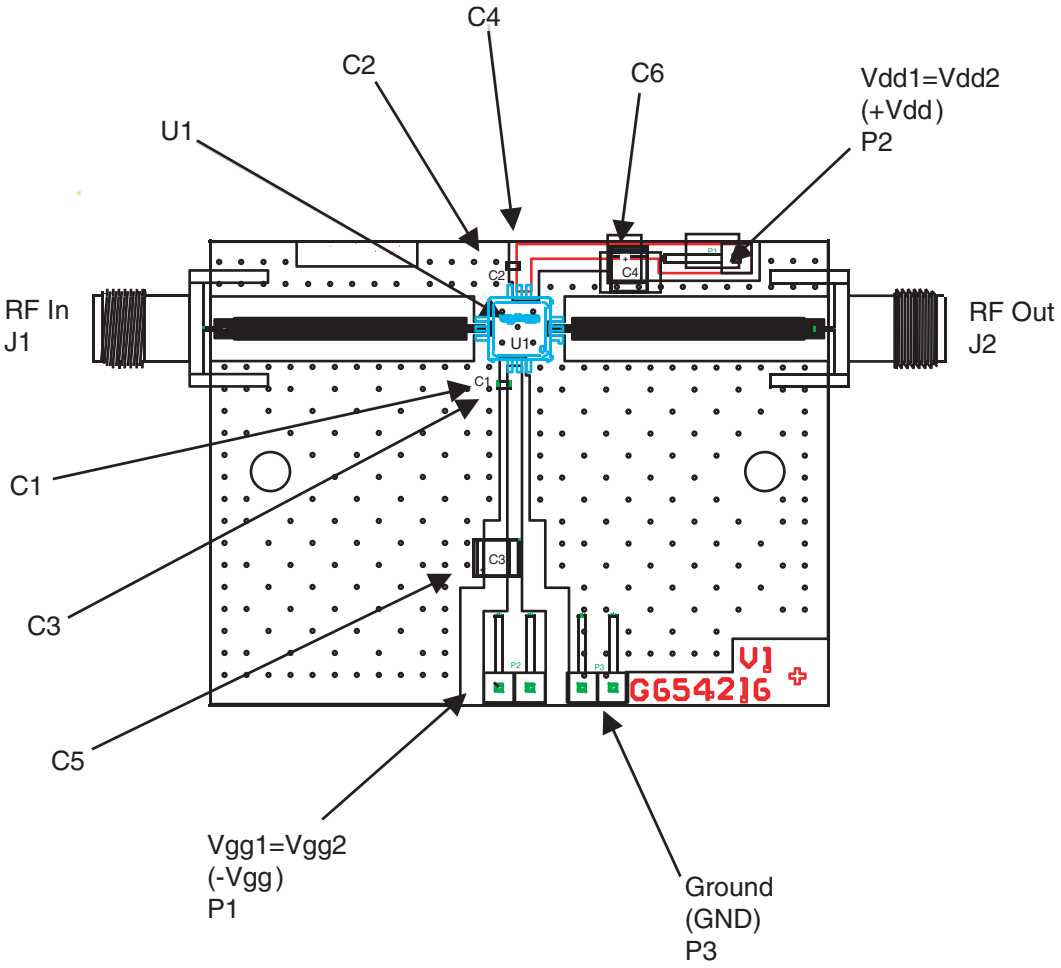


Figure 4. Layout and Assembly of Test Evaluation Board (RMPA2450-TB)

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CoolFET™	FRFET™	MicroFET™	QFET®	SuperSOT™-8
CROSSVOLT™	GlobalOptoisolator™	MicroPak™	QS™	SyncFET™
DOME™	GTO™	MICROWIRE™	QT Optoelectronics™	TinyLogic®
EcoSPARK™	HiSeC™	MSX™	Quiet Series™	TINYOPTO™
E^2CMOS™	I^2C™	MSXPro™	RapidConfigure™	TruTranslation™
EnSigna™	*i-Lo*™	OCX™	RapidConnect™	UHC™
FACT™	ImpliedDisconnect™	OCXPro™	µSerDes™	UltraFET®
FACT Quiet Series™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
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Programmable Active Droop™		POP™	Stealth™	

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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