FAIRCHILD
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RMWD38001

37–40 GHz Driver Amplifier MMIC

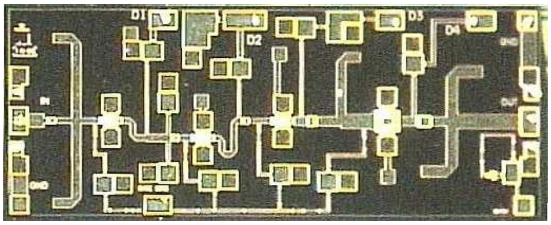
General Description

The RMWD38001 is a 4-stage GaAs MMIC amplifier designed as a 37 to 40 GHz Driver Amplifier for use in point to point and point to multi-point radios, and various communications applications. In conjunction with other Fairchild Semiconductor amplifiers, multipliers and mixers it forms part of a complete 38 GHz transmit/receive chipset. The RMWD38001 utilizes our 0.25µm power PHEMT process and is sufficiently versatile to serve in a variety of applications, such as a driver amplifier or a frequency multiplier.

Features

- 4 mil substrate
- Small-signal gain 25dB (typ.)
- 1dB compressed Pout 18dBm (typ.)
- Voltage detector included to monitor Pout
- Chip size 3.0mm x 1.2mm

Device



Absolute Ratings

Symbol	Parameter	Ratings	Units
Vd	Positive DC Voltage (+4V Typical)	+6	V
Vg	Negative DC Voltage	-2	V
Vdg	Simultaneous (Vd–Vg)	8	V
I_D	Positive DC Current	173	mA
P_{IN}	RF Input Power (from 50Ω source)	+8	dBm
T_C	Operating Baseplate Temperature	-30 to +85	°C
T_{STG}	Storage Temperature Range	-55 to +125	°C
R_{JC}	Thermal Resistance (Channel to Backside)	126	°C/W

Electrical Characteristics (At 25°C), 50Ω system, Vd = +4V, Quiescent Current (Idq) = 105mA

Parameter	Min	Typ	Max	Units
Frequency Range	37		40	GHz
Gate Supply Voltage[1] (Vg)		-0.4		V
Gain Small Signal at Pin = -10dBm	21	25		dB
Gain Variation vs. Frequency		2		dB
Gain at 1dB Compression		24		dB
Power Output at 1dBm Compression		18		dBm
Power Output Saturated: Pin = -5.5dBm	15.5	19		dBm
Drain Current at Pin = -10dBm		105		mA
Drain Current at 1dB Compression		120		mA
Drain Current at Saturated: Pin = -5.5dBm		120		mA
Power Added Efficiency (PAE): at P1dB		13		%
Input Return Loss (Pin = -10dBm)		15		dB
Output Return Loss (Pin = -10dBm)		9		dB
OIP3		28		dBm
Noise Figure		6		dB
Detector Voltage (Pout = +17dBm)		0.1		V

Note:
1: Typical range of negative gate voltages is -0.7 to -0.1V to set typical Idq of 105mA.

Application Information

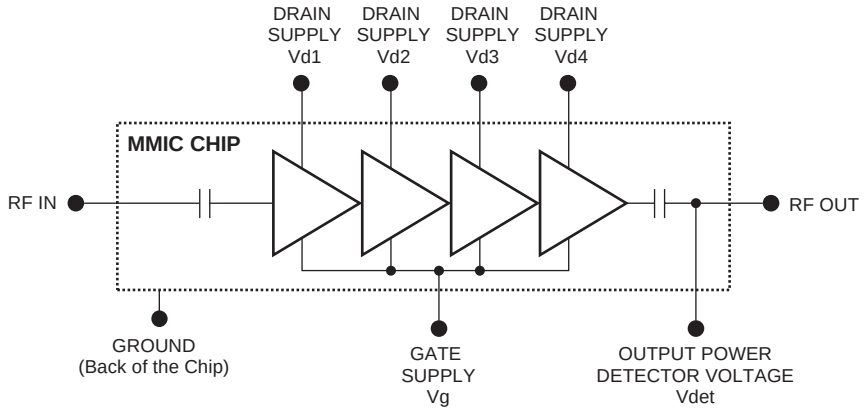
CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF ground.

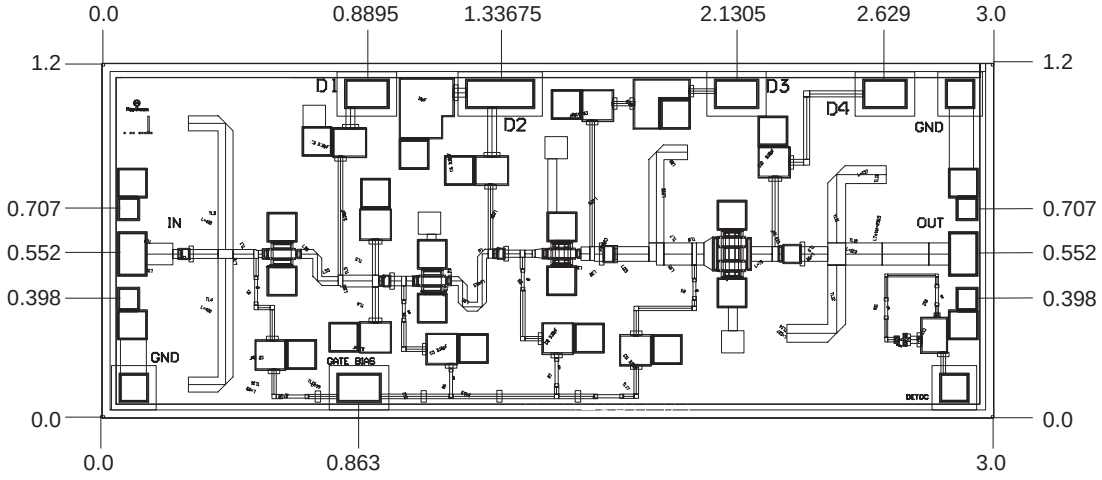
These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typical 2 mil gap between the chip and the substrate material.



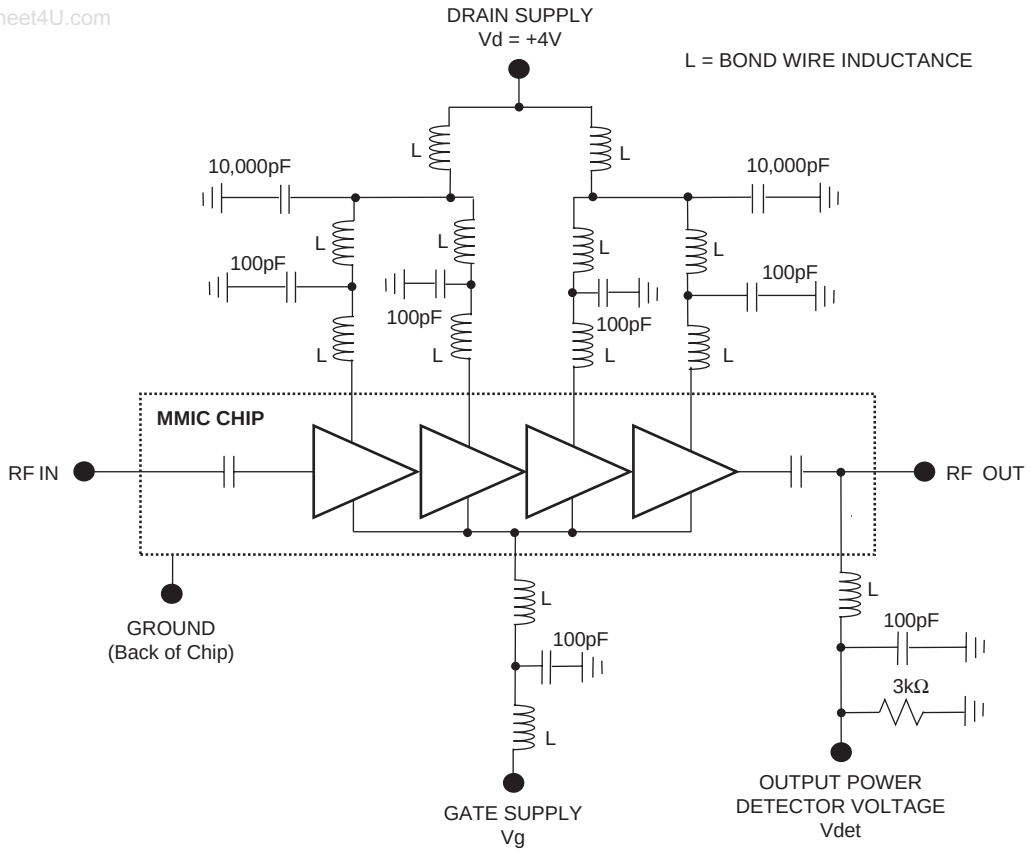
Note:
Detector delivers 0.1V DC into 3kΩ load resistor for > +17dBm output power. If output power level detection is not desired, do not make connection to detector bond pad.

Figure 1. Functional Block Diagram



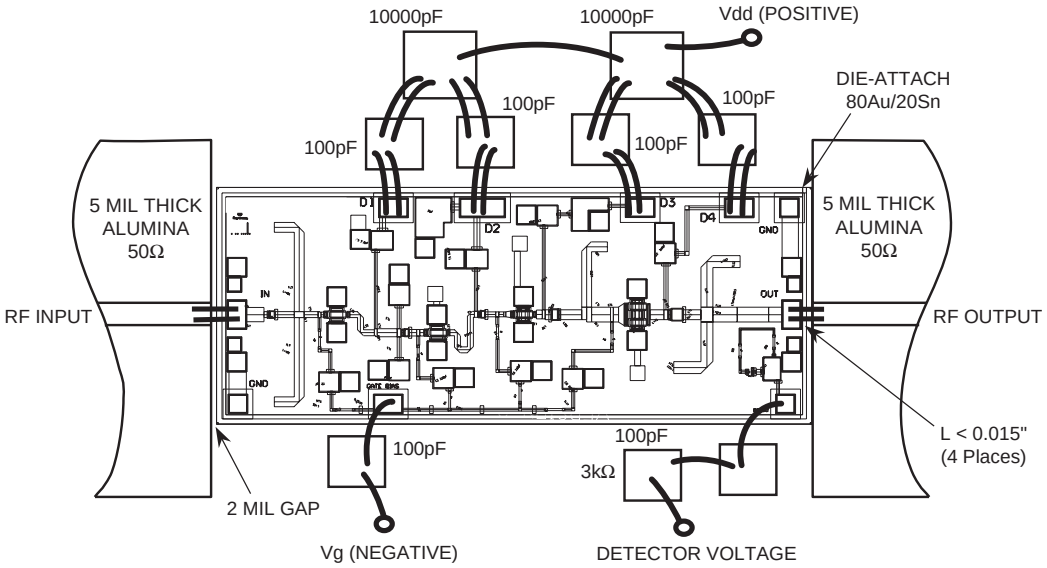
Dimensions in mm

Figure 2. Chip Layout and Bond Pad Locations
(Chip Size is 3.0mm x 1.2mm x 1.2mm. Back of chip is RF and DC Ground)



Note:
Detector delivers 0.1 V DC into 3kΩ load resistor for >+17 dBm output power. If output power level detection is not desired, do not make connection to detector bond pad.

Figure 3. Recommended Application Schematic Circuit Diagram



Note:
Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief. Detector delivers 0.1V DC into 3kΩ load resistor for >+17dBm output power. If output power level detection is not desired, do not make connection to detector bond pad

Figure 4. Recommended Assembly Diagram

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (Vg) WHILE DRAIN VOLTAGE (Vd) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5V to Vgs.

Step 3: Slowly apply positive drain bias supply voltages of +4V to Vd.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq = 105mA.

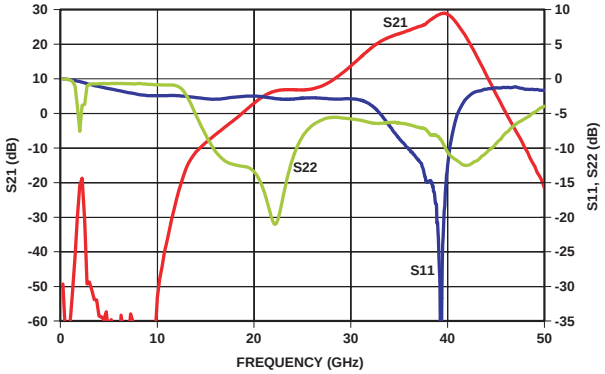
Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

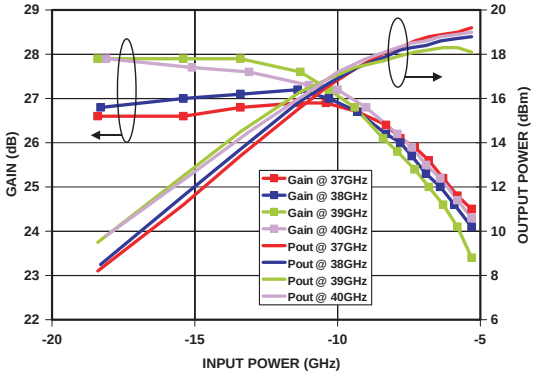
(i) Turn off RF input power,
(ii) Turn down and off drain voltage (Vd),
(iii) Turn down and off gate bias voltage (Vg).

Typical Characteristics

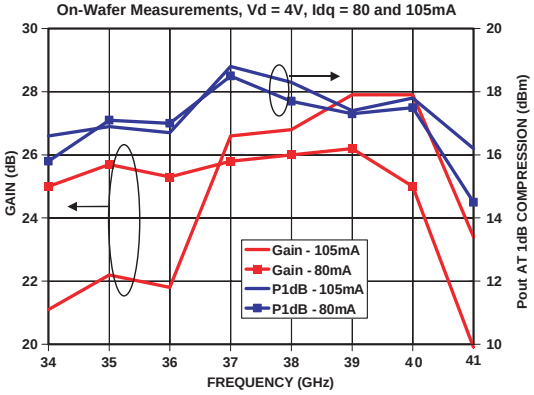
RMWD38001, 37–40GHz Driver Amplifier, Typical Performance,
Vd = 4V, Idq = 105mA, Chip Bonded into 50Ω Test Fixture



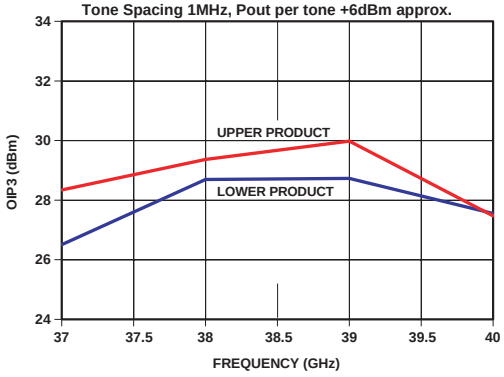
RMWD38001, 37–40GHz Driver Amplifier, Typical Performance,
On-Wafer Measurements, Vd = 4V, Idq = 105mA



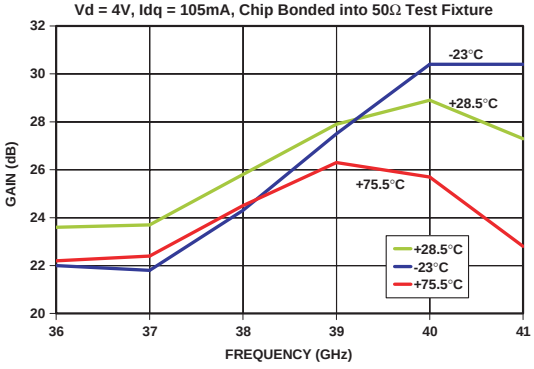
RMWD38001, 37–40GHz Driver Amplifier, Typical Performance,
On-Wafer Measurements, Vd = 4V, Idq = 80 and 105mA



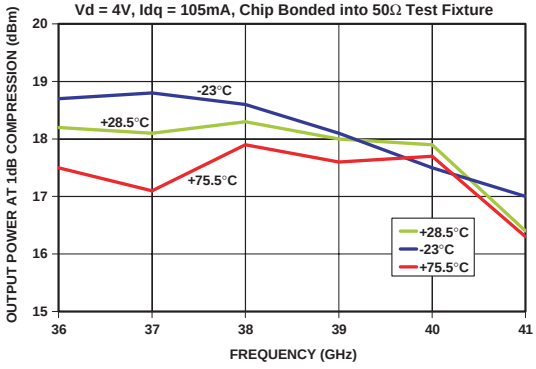
RMWD38001, 37–40GHz Driver Amplifier,
Typical Intermodulation Performance,
Vd = 4V, Idq = 105mA, Chip Bonded into 50Ω Test Fixture
Tone Spacing 1MHz, Pout per tone +6dBm approx.



RMWD38001, Typical Performance over Temperature,
Vd = 4V, Idq = 105mA, Chip Bonded into 50Ω Test Fixture



RMWD38001, Typical Performance over Temperature,
Vd = 4V, Idq = 105mA, Chip Bonded into 50Ω Test Fixture



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