

RMWP38001

37–40 GHz Power Amplifier MMIC

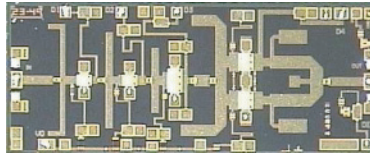
General Description

The RMWP38001 is a 4-stage GaAs MMIC amplifier designed as a 37 to 40 GHz Power Amplifier for use in point to point and point to multi-point radios, and various communications applications. In conjunction with other Fairchild Semiconductor amplifiers, multipliers and mixers it forms part of a complete 38 GHz transmit/receive chipset. The RMWP38001 utilizes our 0.25 μ m power PHEMT process and is sufficiently versatile to serve in a variety of power amplifier applications.

Features

- 4mil substrate
- Small-signal gain 22dB (typ.)
- 1dB compressed Pout 22dBm (typ.)
- Chip size 3.4mm x 1.4mm

Device



Absolute Ratings

Symbol	Parameter	Ratings	Units
V _d	Positive DC Voltage (+4V Typical)	+6	V
V _{dg}	Simultaneous (V _d –V _g)	8	V
I _D	Positive DC Current	483	mA
P _{IN}	RF Input Power (from 50 Ω source)	+8	dBm
T _C	Operating Baseplate Temperature	-30 to +85	°C
T _{STG}	Storage Temperature Range	-55 to +125	°C
R _{JC}	Thermal Resistance (Channel to Backside)	46	°C/W

Electrical Characteristics (At 25°C), 50Ω system, Vd = +4V, Quiescent Current Idq = 250mA

Parameter	Min	Typ	Max	Units
Frequency Range	37		40	GHz
Gate Supply Voltage (Vg) ¹		-0.5		V
Gain Small Signal at Pin = -10dBm	18	22		dB
Gain Variation vs. Frequency		4		dB
Gain at 1dB Compression		21		dB
Power Output at 1dB Compression		22		dBm
Power Output Saturated: Pin = +5dBm	21	23.5		dBm
Drain Current at Pin = -10dBm		250		mA
Drain Current at 1dB Compression		280		mA
Drain Current at Saturated: Pin = +5dBm		270		mA
Power Added Efficiency (PAE): at P1dB		15		%
Input Return Loss (Pin = -10dBm)		12		dB
Output Return Loss (Pin = -10dBm)		7		dB
OIP3		30		dBm
Noise Figure		6		dB
Detector Voltage (Pout = +15dBm) (Bias Current = 0.02–0.05mA)		0.15		V

Note:

1. Typical range of gate voltage is -2.0 to 0V to set Idq of 250mA.

Application Information

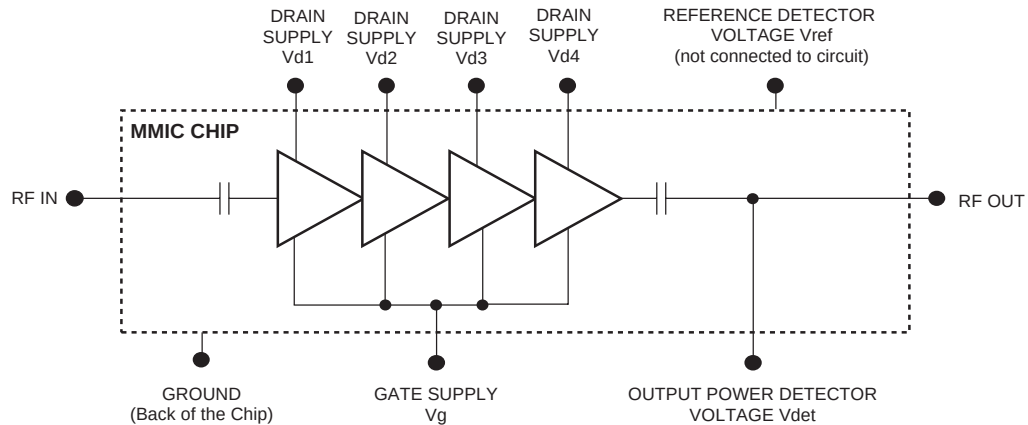
CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typical 2 mil gap between the chip and the substrate material.



Note:

For output power level detection, bias both detector and reference diodes. DC voltage difference between detector and reference can be used to measure output power after calibration. If output power level detection is not desired, do not make connection to detector bond pad.

Figure 1. Functional Block Diagram

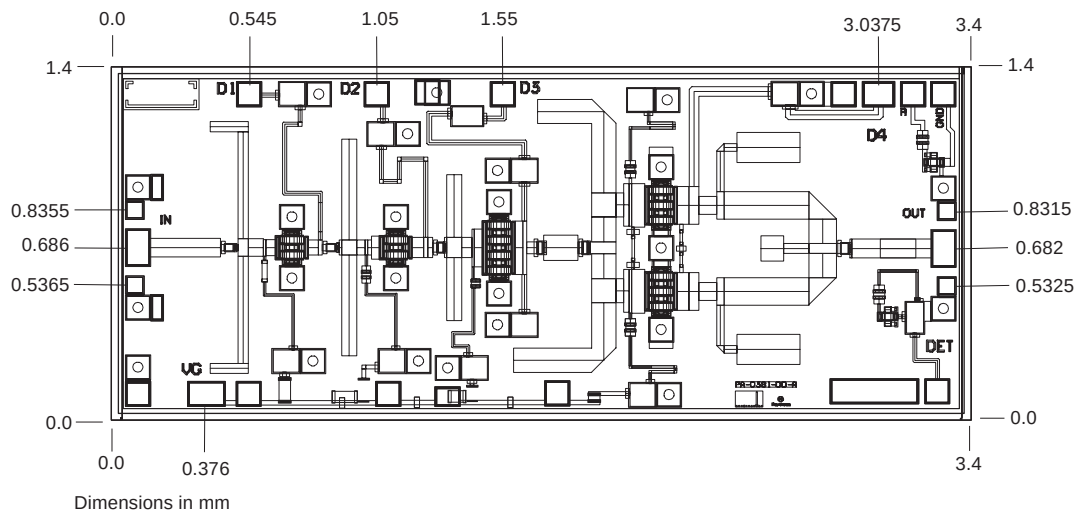


Figure 2. Chip Layout and Bond Pad Locations
(Chip Size is 3.4mm x 1.4mm. Back of chip is RF and DC Ground)

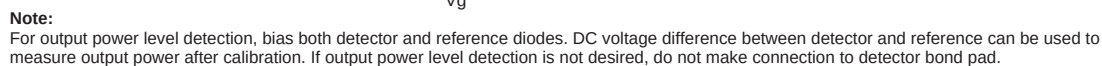


Figure 3. Recommended Application Schematic Circuit Diagram

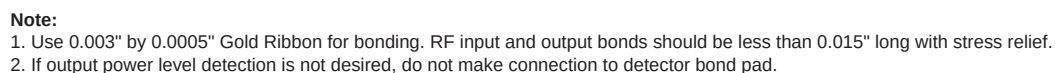


Figure 4. Recommended Assembly Diagram

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (V_g) WHILE DRAIN VOLTAGE (V_d) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5V to V_g .

Step 3: Slowly apply positive drain bias supply voltage of +4V to V_d .

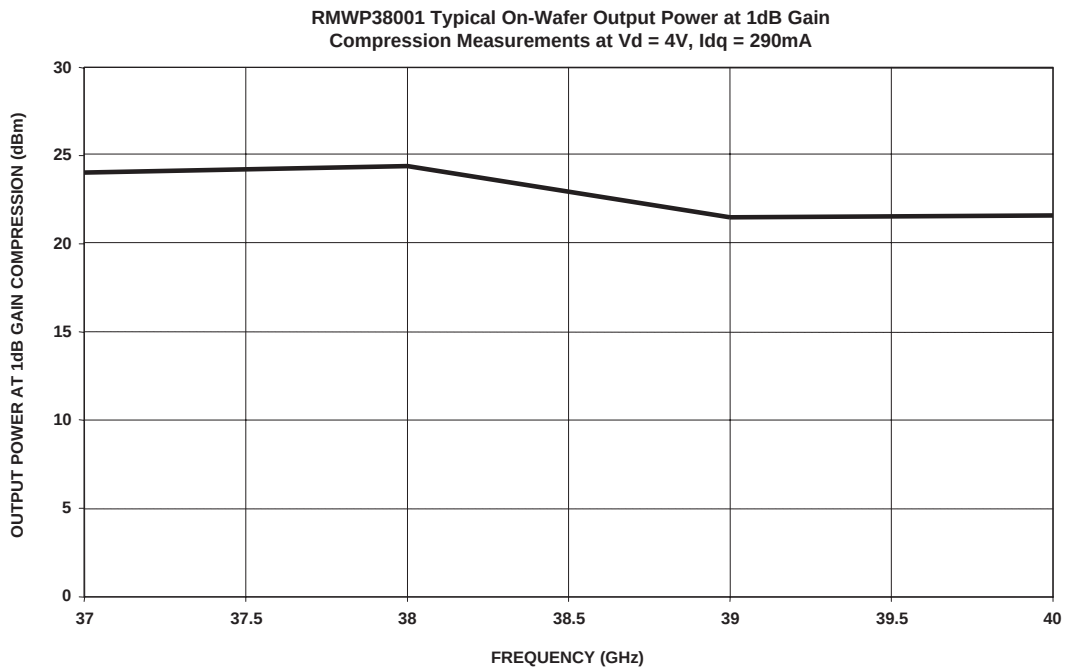
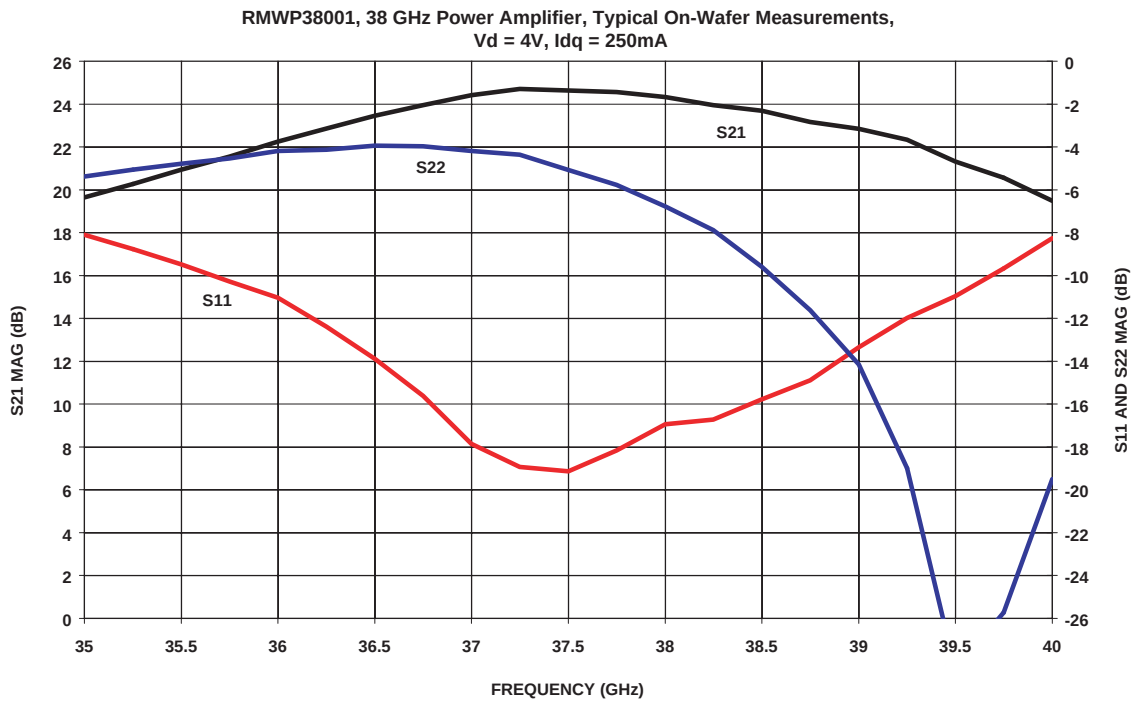
Step 4: Adjust gate bias voltage to set the quiescent current of $I_{dq} = 250\text{mA}$.

Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

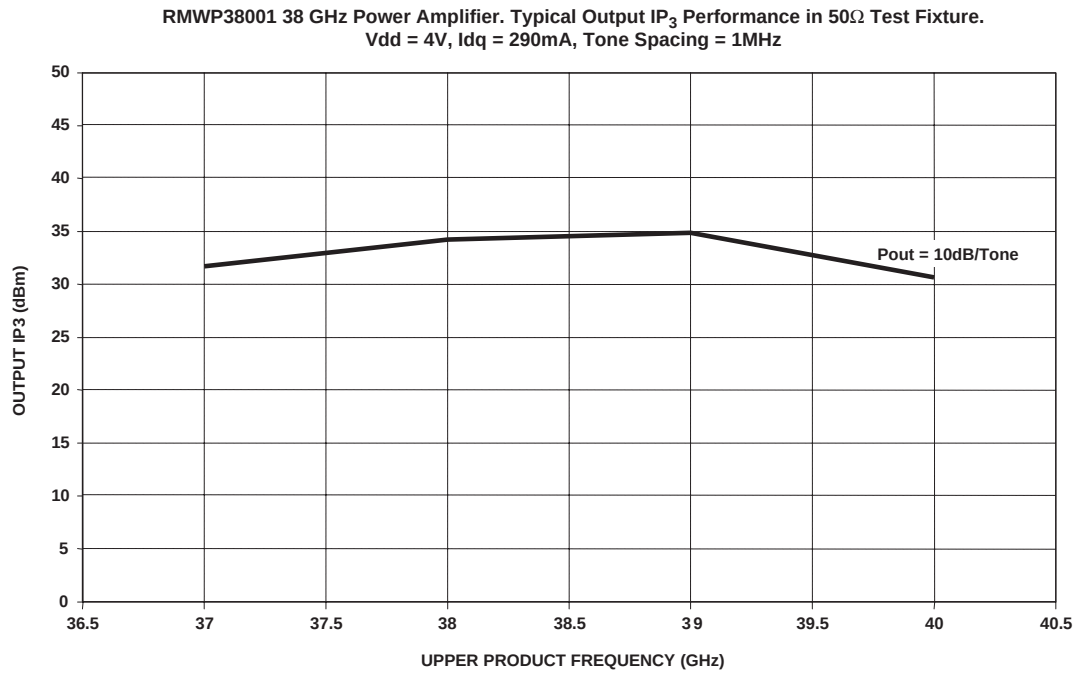
Step 6: Follow turn-off sequence of:

- (i) Turn off RF input power,
- (ii) Turn down and off drain voltage (V_d),
- (iii) Turn down and off gate bias voltage (V_g).

Typical Characteristics



www.DataSheet4U.com Typical Characteristics (Continued)



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Rev. 111